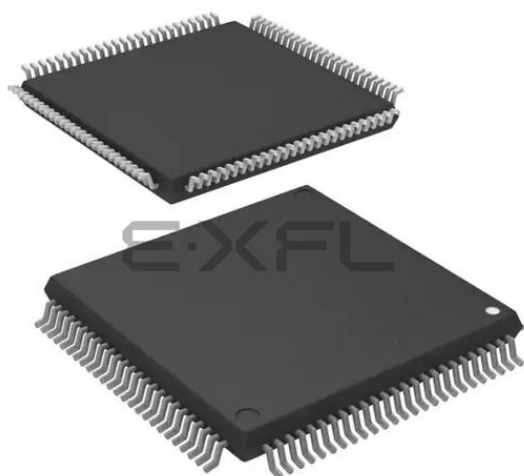




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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                                 |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Discontinued at Digi-Key                                                                                                                                                        |
| Core Processor             | RX                                                                                                                                                                              |
| Core Size                  | 32-Bit Single-Core                                                                                                                                                              |
| Speed                      | 100MHz                                                                                                                                                                          |
| Connectivity               | CANbus, I <sup>2</sup> C, LINbus, SCI, SPI                                                                                                                                      |
| Peripherals                | DMA, LVD, POR, PWM, WDT                                                                                                                                                         |
| Number of I/O              | 55                                                                                                                                                                              |
| Program Memory Size        | 256KB (256K x 8)                                                                                                                                                                |
| Program Memory Type        | FLASH                                                                                                                                                                           |
| EEPROM Size                | -                                                                                                                                                                               |
| RAM Size                   | 16K x 8                                                                                                                                                                         |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V                                                                                                                                                                     |
| Data Converters            | A/D 12x10b, 8x12b                                                                                                                                                               |
| Oscillator Type            | Internal                                                                                                                                                                        |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                               |
| Mounting Type              | Surface Mount                                                                                                                                                                   |
| Package / Case             | 100-LQFP                                                                                                                                                                        |
| Supplier Device Package    | 100-LFQFP (14x14)                                                                                                                                                               |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562tabdfp-v3">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562tabdfp-v3</a> |

**Table 1.1 Outline of Specifications (4 / 5)**

| Classification | Module/Function                               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------------|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Communications | CAN module (CAN)<br>(as an optional function) | <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• 32 mailboxes</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                | Serial peripheral interface (RSPI)            | <ul style="list-style-type: none"> <li>• 1 unit</li> <li>• RSPI transfer facility<br/>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br/>Capable of handling serial transfer as a master or slave</li> <li>• Data formats<br/>Switching between MSB first and LSB first<br/>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.<br/>128-bit buffers for transmission and reception<br/>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)</li> <li>• Buffered structure</li> <li>• Double buffers for both transmission and reception</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                | LIN module (LIN)                              | <ul style="list-style-type: none"> <li>• 1 channel (LIN master)</li> <li>• Supports revisions 1.3, 2.0, and 2.1 of the LIN protocol</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| A/D converter  | 12-bit A/D converter (S12ADA)                 | <ul style="list-style-type: none"> <li>• 12 bits (2 units x 4 channels)</li> <li>• 12-bit resolution</li> <li>• Conversion time:<br/>1.0 <math>\mu</math>s per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC = 4.0 to 5.5 V<br/>2.0 <math>\mu</math>s per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC0 = 3.0 to 3.6 V</li> <li>• Two basic operating modes<br/>Single mode and scan mode</li> <li>• Scan mode<br/>One-cycle scan mode<br/>Continuous scan mode<br/>2-channel scan mode (Input ports of the A/D unit are divided into two groups in this mode, and the activation sources are separately selectable for each group.)</li> <li>• Sample-and-hold function<br/>A common sample-and-hold circuit for both units is included.<br/>Additionally, sample-and-hold circuit for each unit is included. (three channels per unit)</li> <li>• A/D-conversion register settings for each input pin.</li> <li>• Two registers for the result of conversion are provided for a single analog input pin of each unit (AN000 and AN100).</li> <li>• Three ways to start A/D conversion<br/>Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal.</li> <li>• Functionality for 8- or 10-bit precision output<br/>Right-shifting of the results of conversion for output by two or four bits is selectable.</li> <li>• Self-diagnostic function<br/>The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0).</li> <li>• Amplification of input signals by a programmable gain amplifier (three channels per unit)<br/>Amplification rate: 2.0-, 2.5-, 3.077-, 3.636-, 4.0-, 4.444-, 5.0-, 5.714-, 6.667-, 10.0-, or 13.333-times amplification (a total of 11 steps)</li> <li>• Window comparators (three channels per unit)</li> </ul> |

**Table 1.7** List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (3 / 3)

| Pin No.<br>(80-Pin<br>LQFP) | Power Supply<br>Clock<br>System Control | I/O Port | Analog | Timer    | Communication | Interrupt | POE | Debugging |
|-----------------------------|-----------------------------------------|----------|--------|----------|---------------|-----------|-----|-----------|
| 76                          | AVSS0                                   |          |        |          |               |           |     |           |
| 77                          |                                         | P82      |        | MTIC5U   | SCK2-B        |           |     |           |
| 78                          |                                         | P81      |        | MTIC5V   | TXD2-B        |           |     |           |
| 79                          |                                         | P80      |        | MTIC5W   | RXD2-B        |           |     |           |
| 80                          |                                         | P10      |        | MTCLKD-B |               | IRQ0-A    |     |           |

## 2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

## 2.2 Control Registers

### (1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

### (2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts. Set INTB to a multiple of four.

### (3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

### (4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

### (5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

### (6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

### (7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

### (8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

**Table 4.1 List of I/O Registers (Address Order) (6 / 25)**

| Address    | Module Abbreviation | Register Name                          | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------------|----------------------------------------|-----------------------|----------------|-------------|-------------------------|
| 0008 71BEh | ICU                 | DTC activation enable register 190     | DTCER190              | 8              | 8           | 2 ICLK                  |
| 0008 71C0h | ICU                 | DTC activation enable register 192     | DTCER192              | 8              | 8           | 2 ICLK                  |
| 0008 71C1h | ICU                 | DTC activation enable register 193     | DTCER193              | 8              | 8           | 2 ICLK                  |
| 0008 71C2h | ICU                 | DTC activation enable register 194     | DTCER194              | 8              | 8           | 2 ICLK                  |
| 0008 71C3h | ICU                 | DTC activation enable register 195     | DTCER195              | 8              | 8           | 2 ICLK                  |
| 0008 71C4h | ICU                 | DTC activation enable register 196     | DTCER196              | 8              | 8           | 2 ICLK                  |
| 0008 71D7h | ICU                 | DTC activation enable register 215     | DTCER215              | 8              | 8           | 2 ICLK                  |
| 0008 71D8h | ICU                 | DTC activation enable register 216     | DTCER216              | 8              | 8           | 2 ICLK                  |
| 0008 71DBh | ICU                 | DTC activation enable register 219     | DTCER219              | 8              | 8           | 2 ICLK                  |
| 0008 71DCh | ICU                 | DTC activation enable register 220     | DTCER220              | 8              | 8           | 2 ICLK                  |
| 0008 71DFh | ICU                 | DTC activation enable register 223     | DTCER223              | 8              | 8           | 2 ICLK                  |
| 0008 71E0h | ICU                 | DTC activation enable register 224     | DTCER224              | 8              | 8           | 2 ICLK                  |
| 0008 71F7h | ICU                 | DTC activation enable register 247     | DTCER247              | 8              | 8           | 2 ICLK                  |
| 0008 71F8h | ICU                 | DTC activation enable register 248     | DTCER248              | 8              | 8           | 2 ICLK                  |
| 0008 71FEh | ICU                 | DTC activation enable register 254     | DTCER254              | 8              | 8           | 2 ICLK                  |
| 0008 7202h | ICU                 | Interrupt request enable register 02   | IER02                 | 8              | 8           | 2 ICLK                  |
| 0008 7203h | ICU                 | Interrupt request enable register 03   | IER03                 | 8              | 8           | 2 ICLK                  |
| 0008 7205h | ICU                 | Interrupt request enable register 05   | IER05                 | 8              | 8           | 2 ICLK                  |
| 0008 7207h | ICU                 | Interrupt request enable register 07   | IER07                 | 8              | 8           | 2 ICLK                  |
| 0008 7208h | ICU                 | Interrupt request enable register 08   | IER08                 | 8              | 8           | 2 ICLK                  |
| 0008 720Ch | ICU                 | Interrupt request enable register 0C   | IER0C                 | 8              | 8           | 2 ICLK                  |
| 0008 720Dh | ICU                 | Interrupt request enable register 0D   | IER0D                 | 8              | 8           | 2 ICLK                  |
| 0008 720Eh | ICU                 | Interrupt request enable register 0E   | IER0E                 | 8              | 8           | 2 ICLK                  |
| 0008 720Fh | ICU                 | Interrupt request enable register 0F   | IER0F                 | 8              | 8           | 2 ICLK                  |
| 0008 7210h | ICU                 | Interrupt request enable register 10   | IER10                 | 8              | 8           | 2 ICLK                  |
| 0008 7211h | ICU                 | Interrupt request enable register 11   | IER11                 | 8              | 8           | 2 ICLK                  |
| 0008 7212h | ICU                 | Interrupt request enable register 12   | IER12                 | 8              | 8           | 2 ICLK                  |
| 0008 7213h | ICU                 | Interrupt request enable register 13   | IER13                 | 8              | 8           | 2 ICLK                  |
| 0008 7215h | ICU                 | Interrupt request enable register 15   | IER15                 | 8              | 8           | 2 ICLK                  |
| 0008 7216h | ICU                 | Interrupt request enable register 16   | IER16                 | 8              | 8           | 2 ICLK                  |
| 0008 7217h | ICU                 | Interrupt request enable register 17   | IER17                 | 8              | 8           | 2 ICLK                  |
| 0008 7218h | ICU                 | Interrupt request enable register 18   | IER18                 | 8              | 8           | 2 ICLK                  |
| 0008 721Ah | ICU                 | Interrupt request enable register 1A   | IER1A                 | 8              | 8           | 2 ICLK                  |
| 0008 721Bh | ICU                 | Interrupt request enable register 1B   | IER1B                 | 8              | 8           | 2 ICLK                  |
| 0008 721Ch | ICU                 | Interrupt request enable register 1C   | IER1C                 | 8              | 8           | 2 ICLK                  |
| 0008 721Eh | ICU                 | Interrupt request enable register 1E   | IER1E                 | 8              | 8           | 2 ICLK                  |
| 0008 721Fh | ICU                 | Interrupt request enable register 1F   | IER1F                 | 8              | 8           | 2 ICLK                  |
| 0008 72E0h | ICU                 | Software interrupt activation register | SWINTR                | 8              | 8           | 2 ICLK                  |
| 0008 72F0h | ICU                 | Fast interrupt set register            | FIR                   | 16             | 16          | 2 ICLK                  |
| 0008 7300h | ICU                 | Interrupt source priority register 00  | IPR00                 | 8              | 8           | 2 ICLK                  |
| 0008 7301h | ICU                 | Interrupt source priority register 01  | IPR01                 | 8              | 8           | 2 ICLK                  |
| 0008 7302h | ICU                 | Interrupt source priority register 02  | IPR02                 | 8              | 8           | 2 ICLK                  |
| 0008 7303h | ICU                 | Interrupt source priority register 03  | IPR03                 | 8              | 8           | 2 ICLK                  |
| 0008 7304h | ICU                 | Interrupt source priority register 04  | IPR04                 | 8              | 8           | 2 ICLK                  |

**Table 4.1 List of I/O Registers (Address Order) (7 / 25)**

| Address    | Module Abbreviation | Register Name                         | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------------|---------------------------------------|-----------------------|----------------|-------------|-------------------------|
| 0008 7305h | ICU                 | Interrupt source priority register 05 | IPR05                 | 8              | 8           | 2 ICLK                  |
| 0008 7306h | ICU                 | Interrupt source priority register 06 | IPR06                 | 8              | 8           | 2 ICLK                  |
| 0008 7307h | ICU                 | Interrupt source priority register 07 | IPR07                 | 8              | 8           | 2 ICLK                  |
| 0008 7314h | ICU                 | Interrupt source priority register 14 | IPR14                 | 8              | 8           | 2 ICLK                  |
| 0008 7318h | ICU                 | Interrupt source priority register 18 | IPR18                 | 8              | 8           | 2 ICLK                  |
| 0008 7320h | ICU                 | Interrupt source priority register 20 | IPR20                 | 8              | 8           | 2 ICLK                  |
| 0008 7321h | ICU                 | Interrupt source priority register 21 | IPR21                 | 8              | 8           | 2 ICLK                  |
| 0008 7322h | ICU                 | Interrupt source priority register 22 | IPR22                 | 8              | 8           | 2 ICLK                  |
| 0008 7323h | ICU                 | Interrupt source priority register 23 | IPR23                 | 8              | 8           | 2 ICLK                  |
| 0008 7324h | ICU                 | Interrupt source priority register 24 | IPR24                 | 8              | 8           | 2 ICLK                  |
| 0008 7325h | ICU                 | Interrupt source priority register 25 | IPR25                 | 8              | 8           | 2 ICLK                  |
| 0008 7326h | ICU                 | Interrupt source priority register 26 | IPR26                 | 8              | 8           | 2 ICLK                  |
| 0008 7327h | ICU                 | Interrupt source priority register 27 | IPR27                 | 8              | 8           | 2 ICLK                  |
| 0008 7340h | ICU                 | Interrupt source priority register 40 | IPR40                 | 8              | 8           | 2 ICLK                  |
| 0008 7344h | ICU                 | Interrupt source priority register 44 | IPR44                 | 8              | 8           | 2 ICLK                  |
| 0008 7348h | ICU                 | Interrupt source priority register 48 | IPR48                 | 8              | 8           | 2 ICLK                  |
| 0008 7349h | ICU                 | Interrupt source priority register 49 | IPR49                 | 8              | 8           | 2 ICLK                  |
| 0008 7351h | ICU                 | Interrupt source priority register 51 | IPR51                 | 8              | 8           | 2 ICLK                  |
| 0008 7352h | ICU                 | Interrupt source priority register 52 | IPR52                 | 8              | 8           | 2 ICLK                  |
| 0008 7353h | ICU                 | Interrupt source priority register 53 | IPR53                 | 8              | 8           | 2 ICLK                  |
| 0008 7354h | ICU                 | Interrupt source priority register 54 | IPR54                 | 8              | 8           | 2 ICLK                  |
| 0008 7355h | ICU                 | Interrupt source priority register 55 | IPR55                 | 8              | 8           | 2 ICLK                  |
| 0008 7356h | ICU                 | Interrupt source priority register 56 | IPR56                 | 8              | 8           | 2 ICLK                  |
| 0008 7357h | ICU                 | Interrupt source priority register 57 | IPR57                 | 8              | 8           | 2 ICLK                  |
| 0008 7358h | ICU                 | Interrupt source priority register 58 | IPR58                 | 8              | 8           | 2 ICLK                  |
| 0008 7359h | ICU                 | Interrupt source priority register 59 | IPR59                 | 8              | 8           | 2 ICLK                  |
| 0008 735Ah | ICU                 | Interrupt source priority register 5A | IPR5A                 | 8              | 8           | 2 ICLK                  |
| 0008 735Bh | ICU                 | Interrupt source priority register 5B | IPR5B                 | 8              | 8           | 2 ICLK                  |
| 0008 735Ch | ICU                 | Interrupt source priority register 5C | IPR5C                 | 8              | 8           | 2 ICLK                  |
| 0008 735Dh | ICU                 | Interrupt source priority register 5D | IPR5D                 | 8              | 8           | 2 ICLK                  |
| 0008 735Eh | ICU                 | Interrupt source priority register 5E | IPR5E                 | 8              | 8           | 2 ICLK                  |
| 0008 735Fh | ICU                 | Interrupt source priority register 5F | IPR5F                 | 8              | 8           | 2 ICLK                  |
| 0008 7360h | ICU                 | Interrupt source priority register 60 | IPR60                 | 8              | 8           | 2 ICLK                  |
| 0008 7367h | ICU                 | Interrupt source priority register 67 | IPR67                 | 8              | 8           | 2 ICLK                  |
| 0008 7368h | ICU                 | Interrupt source priority register 68 | IPR68                 | 8              | 8           | 2 ICLK                  |
| 0008 7369h | ICU                 | Interrupt source priority register 69 | IPR69                 | 8              | 8           | 2 ICLK                  |
| 0008 736Ah | ICU                 | Interrupt source priority register 6A | IPR6A                 | 8              | 8           | 2 ICLK                  |
| 0008 736Bh | ICU                 | Interrupt source priority register 6B | IPR6B                 | 8              | 8           | 2 ICLK                  |
| 0008 736Ch | ICU                 | Interrupt source priority register 6C | IPR6C                 | 8              | 8           | 2 ICLK                  |
| 0008 736Dh | ICU                 | Interrupt source priority register 6D | IPR6D                 | 8              | 8           | 2 ICLK                  |
| 0008 736Eh | ICU                 | Interrupt source priority register 6E | IPR6E                 | 8              | 8           | 2 ICLK                  |
| 0008 736Fh | ICU                 | Interrupt source priority register 6F | IPR6F                 | 8              | 8           | 2 ICLK                  |
| 0008 7380h | ICU                 | Interrupt source priority register 80 | IPR80                 | 8              | 8           | 2 ICLK                  |
| 0008 7381h | ICU                 | Interrupt source priority register 81 | IPR81                 | 8              | 8           | 2 ICLK                  |

**Table 4.1 List of I/O Registers (Address Order) (10 / 25)**

| Address    | Module Abbreviation | Register Name                                     | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|------------|---------------------|---------------------------------------------------|-----------------------|----------------|-------------|-------------------------|
| 0008 8250h | SCI2                | Serial mode register                              | SMR <sup>*1</sup>     | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8251h | SCI2                | Bit rate register                                 | BRR                   | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8252h | SCI2                | Serial control register                           | SCR <sup>*1</sup>     | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8253h | SCI2                | Transmit data register                            | TDR                   | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8254h | SCI2                | Serial status register                            | SSR <sup>*1</sup>     | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8255h | SCI2                | Receive data register                             | RDR                   | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8256h | SCI2                | Smart card mode register                          | SCMR                  | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8257h | SCI2                | Serial extended mode register                     | SEMR                  | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8250h | SMCI2               | Serial mode register                              | SMR <sup>*1</sup>     | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8251h | SMCI2               | Bit rate register                                 | BRR                   | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8252h | SMCI2               | Serial control register                           | SCR <sup>*1</sup>     | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8253h | SMCI2               | Transmit data register                            | TDR                   | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8254h | SMCI2               | Serial status register                            | SSR <sup>*1</sup>     | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8255h | SMCI2               | Receive data register                             | RDR                   | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8256h | SMCI2               | Smart card mode register                          | SCMR                  | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8280h | CRC                 | CRC control register                              | CRCCR                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8281h | CRC                 | CRC data input register                           | CRCDIR                | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8282h | CRC                 | CRC data output register                          | CRCDOR                | 16             | 16          | 2, 3 PCLK <sup>*3</sup> |
| 0008 8300h | RIIC                | I <sup>2</sup> C bus control register 1           | ICCR1                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8301h | RIIC                | I <sup>2</sup> C bus control register 2           | ICCR2                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8302h | RIIC                | I <sup>2</sup> C bus mode register 1              | ICMR1                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8303h | RIIC                | I <sup>2</sup> C bus mode register 2              | ICMR2                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8304h | RIIC                | I <sup>2</sup> C bus mode register 3              | ICMR3                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8305h | RIIC                | I <sup>2</sup> C bus function enable register     | ICFER                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8306h | RIIC                | I <sup>2</sup> C bus status enable register       | ICSER                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8307h | RIIC                | I <sup>2</sup> C bus interrupt enable register    | ICIER                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8308h | RIIC                | I <sup>2</sup> C bus status register 1            | ICSR1                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8309h | RIIC                | I <sup>2</sup> C bus status register 2            | ICSR2                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 830Ah | RIIC                | Slave address register L0                         | SARL0                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 830Ah | RIIC                | Internal counter L for timeout                    | TMOCNTL               | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 830Bh | RIIC                | Slave address register U0                         | SARU0                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 830Bh | RIIC                | Internal counter U for timeout                    | TMOCNTU               | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 830Bh | RIIC                | Slave address register U0                         | SARU0                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 830Ch | RIIC                | Slave address register L1                         | SARL1                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 830Dh | RIIC                | Slave address register U1                         | SARU1                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 830Eh | RIIC                | Slave address register L2                         | SARL2                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 830Fh | RIIC                | Slave address register U2                         | SARU2                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8310h | RIIC                | I <sup>2</sup> C bus bit rate low-level register  | ICBRL                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8311h | RIIC                | I <sup>2</sup> C bus bit rate high-level register | ICBRH                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8312h | RIIC                | I <sup>2</sup> C bus transmit data register       | ICDRT                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8313h | RIIC                | I <sup>2</sup> C bus receive data register        | ICDRR                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8380h | RSPI                | RSPI control register                             | SPCR                  | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8381h | RSPI                | RSPI slave select polarity register               | SSLP                  | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |
| 0008 8382h | RSPI                | RSPI pin control register                         | SPPCR                 | 8              | 8           | 2, 3 PCLK <sup>*3</sup> |

**Table 4.1 List of I/O Registers (Address Order) (21 / 25)**

| Address    | Module Abbreviation | Register Name                                                                         | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles   |
|------------|---------------------|---------------------------------------------------------------------------------------|-----------------------|----------------|-------------|---------------------------|
| 000C 2116h | GPT0                | General PWM timer compare capture register D                                          | GTCCRD                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2118h | GPT0                | General PWM timer compare capture register E                                          | GTCCRE                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 211Ah | GPT0                | General PWM timer compare capture register F                                          | GTCCRF                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 211Ch | GPT0                | General PWM timer cycle setting register                                              | GTPR                  | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 211Eh | GPT0                | General PWM timer cycle setting buffer register                                       | GTPBR                 | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2120h | GPT0                | General PWM timer cycle setting double-buffer register                                | GTPDBR                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2124h | GPT0                | A/D converter start request timing register A                                         | GTADTRA               | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2126h | GPT0                | A/D converter start request timing buffer register A                                  | GTADTBRA              | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2128h | GPT0                | A/D converter start request timing double-buffer register A                           | GTADTBRA              | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 212Ch | GPT0                | A/D converter start request timing register B                                         | GTADTRB               | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 212Eh | GPT0                | A/D converter start request timing buffer register B                                  | GTADTRB               | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2130h | GPT0                | A/D converter start request timing double-buffer register B                           | GTADTRB               | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2134h | GPT0                | General PWM timer output negate control register                                      | GTONCR                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2136h | GPT0                | General PWM timer dead time control register                                          | GTDTCR                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2138h | GPT0                | General PWM timer dead time value register                                            | GTDVU                 | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 213Ah | GPT0                | General PWM timer dead time value register                                            | GTDVD                 | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 213Ch | GPT0                | General PWM timer dead time buffer register                                           | GTDBU                 | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 213Eh | GPT0                | General PWM timer dead time buffer register                                           | GTDBD                 | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2140h | GPT0                | General PWM timer output protection function status register                          | GTSOS                 | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2142h | GPT0                | General PWM timer output protection function temporary release register               | GTSOTR                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2180h | GPT1                | General PWM timer I/O control register                                                | GTIOR                 | 16             | 8, 16, 32   | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2182h | GPT1                | General PWM timer interrupt output setting register                                   | GTINTAD               | 16             | 8, 16, 32   | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2184h | GPT1                | General PWM timer control register                                                    | GTCR                  | 16             | 8, 16, 32   | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2186h | GPT1                | General PWM timer buffer enable register                                              | GTBER                 | 16             | 8, 16, 32   | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2188h | GPT1                | General PWM timer count direction register                                            | GTUDC                 | 16             | 8, 16, 32   | 3 to 5 ICLK <sup>*4</sup> |
| 000C 218Ah | GPT1                | General PWM timer interrupt and A/D converter start request skipping setting register | GTITC                 | 16             | 8, 16, 32   | 3 to 5 ICLK <sup>*4</sup> |
| 000C 218Ch | GPT1                | General PWM timer status register                                                     | GTST                  | 16             | 8, 16, 32   | 3 to 5 ICLK <sup>*4</sup> |
| 000C 218Eh | GPT1                | General PWM timer counter                                                             | GTCNT                 | 16             | 16          | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2190h | GPT1                | General PWM timer compare capture register A                                          | GTCCRA                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2192h | GPT1                | General PWM timer compare capture register B                                          | GTCCRB                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2194h | GPT1                | General PWM timer compare capture register C                                          | GTCCRC                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2196h | GPT1                | General PWM timer compare capture register D                                          | GTCCRD                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 2198h | GPT1                | General PWM timer compare capture register E                                          | GTCCRE                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 219Ah | GPT1                | General PWM timer compare capture register F                                          | GTCCRF                | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 219Ch | GPT1                | General PWM timer cycle setting register                                              | GTPR                  | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |
| 000C 219Eh | GPT1                | General PWM timer cycle setting buffer register                                       | GTPBR                 | 16             | 16, 32      | 3 to 5 ICLK <sup>*4</sup> |



**Table 4.1 List of I/O Registers (Address Order) (25 / 25)**

| Address    | Module<br>Abbreviation | Register Name                           | Register<br>Abbreviation | Number<br>of Bits | Access<br>Size | Number of<br>Access<br>Cycles |
|------------|------------------------|-----------------------------------------|--------------------------|-------------------|----------------|-------------------------------|
| 007F FFBAh | FLASH                  | FCU command register                    | FCMDR                    | 16                | 16             | 2, 3 PCLK <sup>*3</sup>       |
| 007F FFC8h | FLASH                  | FCU processing switching register       | FCPSR                    | 16                | 16             | 2, 3 PCLK <sup>*3</sup>       |
| 007F FFCAh | FLASH                  | Data flash blank check control register | DFLBCCNT                 | 16                | 16             | 2, 3 PCLK <sup>*3</sup>       |
| 007F FFCCh | FLASH                  | Flash P/E status register               | FPESTAT                  | 16                | 16             | 2, 3 PCLK <sup>*3</sup>       |
| 007F FFCEh | FLASH                  | Data flash blank check status register  | DFLBCSTAT                | 16                | 16             | 2, 3 PCLK <sup>*3</sup>       |
| 007F FFE8h | FLASH                  | Peripheral clock notification register  | PCKAR                    | 16                | 16             | 2, 3 PCLK <sup>*3</sup>       |

Note 1. This register is not supported by the 100-pin LQFP version.

Note 2. This register is not supported by the product without the CAN function.

Note 3. The number of access states depends on the number of divided cycles for clock synchronization (0 to 1 PCLK).

Note 4. Reading the registers takes 3 cycles of ICLK and writing to the registers takes 5 cycles of ICLK.

**Table 4.2 List of I/O Registers (Bit Order) (3 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---------------------|-----------------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| MPU                 | RSPAGE7               |                |                |                |                | RSPN[27:0]     |                |               |               |
|                     |                       |                |                |                |                | RSPN[27:0]     |                |               |               |
|                     |                       |                |                |                |                | RSPN[27:0]     |                |               |               |
|                     |                       |                |                | RSPN[27:0]     |                | —              | —              | —             | —             |
| MPU                 | REPAGE7               |                |                |                |                | REPN[27:0]     |                |               |               |
|                     |                       |                |                |                |                | REPN[27:0]     |                |               |               |
|                     |                       |                |                |                |                | REPN[27:0]     |                |               |               |
|                     |                       |                |                | REPN[27:0]     |                |                | UAC[2:0]       |               | V             |
| MPU                 | MPEN                  | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | MPEN          |
| MPU                 | MPBAC                 | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              |                | UBAC[2:0]      |               | —             |
| MPU                 | MPECLR                | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | CLR           |
| MPU                 | MPESTS                | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DRW            | DA            | IA            |
| MPU                 | MPDEA                 |                |                |                |                | DEA[31:0]      |                |               |               |
|                     |                       |                |                |                |                | DEA[31:0]      |                |               |               |
|                     |                       |                |                |                |                | DEA[31:0]      |                |               |               |
|                     |                       |                |                |                |                | DEA[31:0]      |                |               |               |
| MPU                 | MPSA                  |                |                |                |                | SA[31:0]       |                |               |               |
|                     |                       |                |                |                |                | SA[31:0]       |                |               |               |
|                     |                       |                |                |                |                | SA[31:0]       |                |               |               |
|                     |                       |                |                |                |                | SA[31:0]       |                |               |               |
| MPU                 | MPOPS                 | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | S             |
| MPU                 | MPOPI                 | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | INV           |
| MPU                 | MHITI                 | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       |                |                |                |                | HITI[7:0]      |                |               |               |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              |                | UHACI[2:0]     |               | —             |
| MPU                 | MHITD                 | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       |                |                |                |                | HITD[7:0]      |                |               |               |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              |                | UHACD[2:0]     |               | —             |
| ICU                 | IR016                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR021                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR023                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR027                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR028                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR029                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR030                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR031                 | —              | —              | —              | —              | —              | —              | —             | IR            |

**Table 4.2 List of I/O Registers (Bit Order) (4 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---------------------|-----------------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| ICU                 | IR044                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR045                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR046                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR047                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR056                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR057                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR058                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR059                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR060                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR064                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR065                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR066                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR067                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR068                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR069                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR070                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR071                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR096                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR098                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR102                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR103                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR106                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR114                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR115                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR116                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR117                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR118                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR119                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR120                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR121                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR122                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR123                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR124                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR125                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR126                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR127                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR128                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR129                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR130                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR131                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR132                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR133                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR134                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR135                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR136                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR137                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR138                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR139                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR140                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR141                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR142                 | —              | —              | —              | —              | —              | —              | —             | IR            |
| ICU                 | IR143                 | —              | —              | —              | —              | —              | —              | —             | IR            |

**Table 4.2 List of I/O Registers (Bit Order) (29 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---------------------|-----------------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| GPT2                | GTDLYCR               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLYEN          | DLYRST        | DLEN          |
| GPT3                | GTDLYCR               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLYEN          | DLYRST        | DLEN          |
| GPT0                | GTDLYRA               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT0                | GTDLYRB               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT1                | GTDLYRA               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT1                | GTDLYRB               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT2                | GTDLYRA               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT2                | GTDLYRB               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT3                | GTDLYRA               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT3                | GTDLYRB               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT0                | GTDLYFA               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT0                | GTDLYFB               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT1                | GTDLYFA               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT1                | GTDLYFB               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT2                | GTDLYRA               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT2                | GTDLYFB               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT3                | GTDLYFA               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| GPT3                | GTDLYFB               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | DLY[4:0]       | —             | —             |
| FLASH               | FMODR                 | —              | —              | —              | FRDMD          | —              | —              | —             | —             |
| FLASH               | FASTAT                | ROMAE          | —              | —              | CMDLK          | DFLAE          | —              | DFLRPE        | DFLWPE        |
| FLASH               | FAEINT                | ROMAEIE        | —              | —              | CMDLKIE        | DFLAEIE        | —              | DFLRPEIE      | DFLWPEIE      |
| FLASH               | FRDYIE                | —              | —              | —              | —              | —              | —              | —             | FRDYIE        |
| FLASH               | DFLRE0                | KEY[7:0]       |                |                |                |                |                |               |               |
|                     |                       | DBRE07         | DBRE06         | DBRE05         | DBRE04         | DBRE03         | DBRE02         | DBRE01        | DBRE00        |
| FLASH               | DFLRE1                | KEY[7:0]       |                |                |                |                |                |               |               |
|                     |                       | DBRE15         | DBRE14         | DBRE13         | DBRE12         | DBRE11         | DBRE10         | DBRE09        | DBRE08        |
| FLASH               | DFLWE0                | KEY[7:0]       |                |                |                |                |                |               |               |
|                     |                       | DBWE07         | DBWE06         | DBWE05         | DBWE04         | DBWE03         | DBWE02         | DBWE01        | DBWE00        |
| FLASH               | DFLWE1                | KEY[7:0]       |                |                |                |                |                |               |               |
|                     |                       | DBWE15         | DBWE14         | DBWE13         | DBWE12         | DBWE11         | DBWE10         | DBWE09        | DBWE08        |
| FLASH               | FCURAME               | KEY[7:0]       |                |                |                |                |                |               |               |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | FCRME         |

**Table 4.2 List of I/O Registers (Bit Order) (30 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---------------------|-----------------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| FLASH               | FSTATR0               | FRDY           | ILGLERR        | ERSERR         | PRGERR         | SUSRDY         | —              | ERSSPD        | PRGSPD        |
| FLASH               | FSTATR1               | FCUERR         | —              | —              | FLOCKST        | —              | —              | —             | —             |
| FLASH               | FENTRYR               | FEKEY[7:0]     |                |                |                |                |                |               |               |
|                     |                       | FENTRYD        | —              | —              | —              | —              | —              | —             | FENTRY0       |
| FLASH               | FPROTR                | FPKEY[7:0]     |                |                |                |                |                |               |               |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | FPROTCN       |
| FLASH               | FRESETR               | FRKEY[7:0]     |                |                |                |                |                |               |               |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | FRESET        |
| FLASH               | FCMDR                 | CMDR[7:0]      |                |                |                |                |                |               |               |
|                     |                       | PCMDR[7:0]     |                |                |                |                |                |               |               |
| FLASH               | FCPSR                 | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | ESUSPMD       |
| FLASH               | DFLBCCNT              | BCADR[7:0]     |                |                |                |                |                |               |               |
|                     |                       | BCADR[7:0]     |                |                |                |                |                |               |               |
| FLASH               | FPESTAT               | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | PEERRST[7:0]   |                |                |                |                |                |               |               |
| FLASH               | DFLBCSTAT             | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | —              | —              | —              | —              | —              | —              | —             | BCST          |
| FLASH               | PCKAR                 | —              | —              | —              | —              | —              | —              | —             | —             |
|                     |                       | PCKA[7:0]      |                |                |                |                |                |               |               |

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.

## 5. Electrical Characteristics

### 5.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Ratings**

| Item                                    | Symbol                    | Value             | Unit        |
|-----------------------------------------|---------------------------|-------------------|-------------|
| Power supply voltage                    | VCC<br>PLLVCC             | -0.3 to +6.5      | V           |
| Input voltage (except for ports 4 to 6) | V <sub>IN</sub>           | -0.3 to VCC+0.3   | V           |
| Input voltage (port 4)                  | V <sub>IN</sub>           | -0.3 to AVCC0+0.3 | V           |
| Input voltage (ports 5 and 6)           | V <sub>IN</sub>           | -0.3 to AVCC+0.3  | V           |
| Analog power supply voltage             | AVCC0, AVCC* <sup>1</sup> | -0.3 to +6.5      | V           |
| Reference power supply voltage          | VREFH0* <sup>1</sup>      | -0.3 to AVCC0+0.3 | V           |
|                                         | VREF* <sup>1</sup>        | -0.3 to AVCC+0.3  |             |
| Analog input voltage (port 4)           | V <sub>AN</sub>           | -0.3 to AVCC0+0.3 | V           |
| Analog input voltage (ports 5 and 6)    | V <sub>AN</sub>           | -0.3 to AVCC+0.3  | V           |
| Operating temperature                   | D version                 | T <sub>opr</sub>  | -40 to +85  |
|                                         | G version                 | T <sub>opr</sub>  | -40 to +105 |
| Storage temperature                     | T <sub>stg</sub>          | -55 to +125       | °C          |

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open circuit even if the A/D converter is not to be used.

- When the 12-bit converter is not in use:  
Connect the AVCC0 pin to AVCC (or VCC for a 64-pin product), the VREFH0 pin to VREF (or AVCC or VCC for an 80- or 64-pin product, respectively), and the AVSS0 and VREFL0 pins to VSS.
- When the 10-bit converter is not in use:  
Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0.
- When neither the 10- nor the 12-bit converter is in use:  
Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS.

### 5.3.2 Control Signal Timing

**Table 5.8 Control Signal Timing**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC  
Ta = Topr. Ta is the same under conditions 1 to 3.

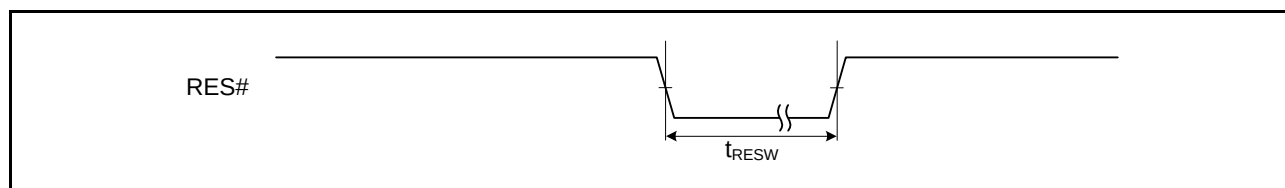
| Item                                                                                                                                 | Symbol          | Min. | Max. | Unit           | Test Conditions |
|--------------------------------------------------------------------------------------------------------------------------------------|-----------------|------|------|----------------|-----------------|
| RES# pulse width<br>(except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory*1) | $t_{RESW}^{*2}$ | 20   | -    | $t_{cyc}^{*4}$ | Figure 5.5      |
|                                                                                                                                      |                 | 1.5  | -    | $\mu\text{s}$  |                 |
| Internal reset time*3                                                                                                                | $t_{RESW2}$     | 35   | -    | $\mu\text{s}$  |                 |
| NMI pulse width                                                                                                                      | $t_{NMIW}$      | 200  | -    | ns             | Figure 5.6      |
| IRQ pulse width                                                                                                                      | $t_{IRQW}$      | 200  | -    | ns             | Figure 5.7      |

Note 1. For a reset by the signal on the RES# pin during programming or erasure of the ROM or data-flash memory or during blank checking of the data-flash memory, see section 31.12, Usage Notes in section 31, ROM (Flash Memory for Code Storage) in the User's manual: Hardware.

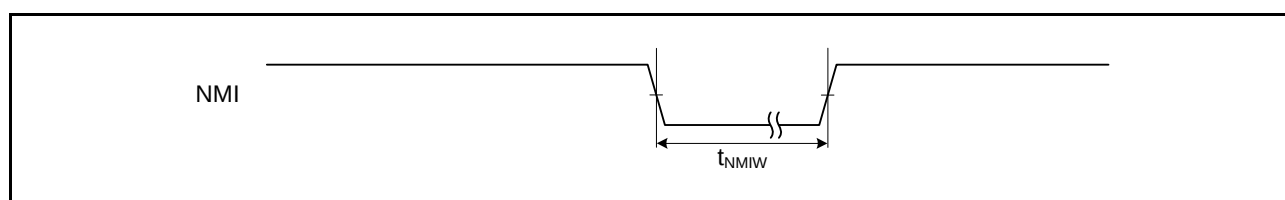
Note 2. Both the time and the number of cycles should satisfy the specifications.

Note 3. This is to specify the FCU reset.

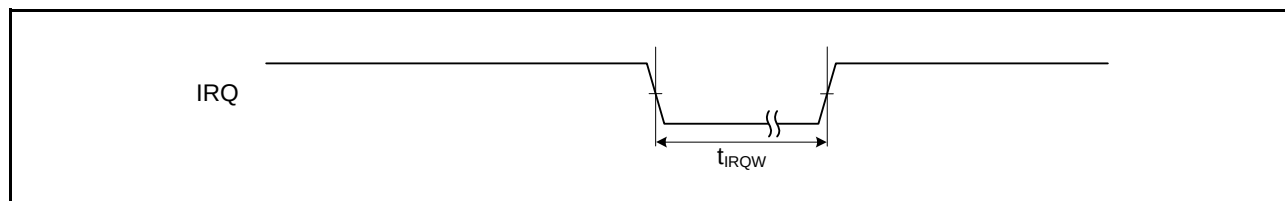
Note 4. ICLK cycles.



**Figure 5.5 Reset Input Timing**



**Figure 5.6 NMI Interrupt Input Timing**



**Figure 5.7 IRQ Interrupt Input Timing**

**Table 5.17 Characteristics of the Programmable Gain Amplifier**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC  
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item                      |               | Symbol | Min.         | Typ. | Max.         | Unit | Test Conditions |
|---------------------------|---------------|--------|--------------|------|--------------|------|-----------------|
| Analog input capacitance  |               | Cin    | -            | -    | 6            | pF   |                 |
| Input offset voltage      |               | Voff   | -            | -    | 8            | mV   |                 |
| Input voltage range (Vin) | Gain × 2.000  | Vin    | 0.050 × AVcc | -    | 0.450 × AVcc | V    |                 |
|                           | Gain × 2.500  |        | 0.047 × AVcc | -    | 0.360 × AVcc |      |                 |
|                           | Gain × 3.077  |        | 0.045 × AVcc | -    | 0.292 × AVcc |      |                 |
|                           | Gain × 3.636  |        | 0.042 × AVcc | -    | 0.247 × AVcc |      |                 |
|                           | Gain × 4.000  |        | 0.040 × AVcc | -    | 0.212 × AVcc |      |                 |
|                           | Gain × 4.444  |        | 0.036 × AVcc | -    | 0.191 × AVcc |      |                 |
|                           | Gain × 5.000  |        | 0.033 × AVcc | -    | 0.170 × AVcc |      |                 |
|                           | Gain × 5.714  |        | 0.031 × AVcc | -    | 0.148 × AVcc |      |                 |
|                           | Gain × 6.667  |        | 0.029 × AVcc | -    | 0.127 × AVcc |      |                 |
|                           | Gain × 10.000 |        | 0.025 × AVcc | -    | 0.08 × AVcc  |      |                 |
|                           | Gain × 13.333 |        | 0.023 × AVcc | -    | 0.06 × AVcc  |      |                 |
| Slew rate                 |               | SR     | 10           | -    | -            | V/μs |                 |
| Gain error                | Gain × 2.000  | -      | -            | -    | 1            | %    |                 |
|                           | Gain × 2.500  |        | -            | -    | 1            |      |                 |
|                           | Gain × 3.077  |        | -            | -    | 1            |      |                 |
|                           | Gain × 3.636  |        | -            | -    | 1.5          |      |                 |
|                           | Gain × 4.000  |        | -            | -    | 1.5          |      |                 |
|                           | Gain × 4.444  |        | -            | -    | 2            |      |                 |
|                           | Gain × 5.000  |        | -            | -    | 2            |      |                 |
|                           | Gain × 5.714  |        | -            | -    | 2            |      |                 |
|                           | Gain × 6.667  |        | -            | -    | 3            |      |                 |
|                           | Gain × 10.000 |        | -            | -    | 4            |      |                 |
|                           | Gain × 13.333 |        | -            | -    | 4            |      |                 |



## 5.5 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

**Table 5.19 Power-on Reset Circuit, Voltage Detection Circuit Characteristics**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

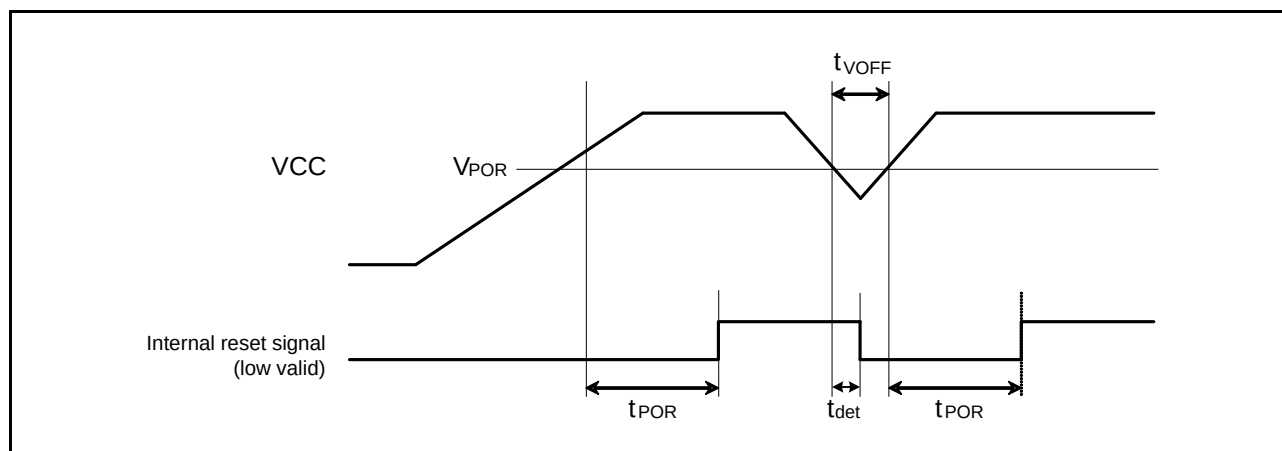
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC  
Ta = Topr. Ta is the same under conditions 1 and 2.

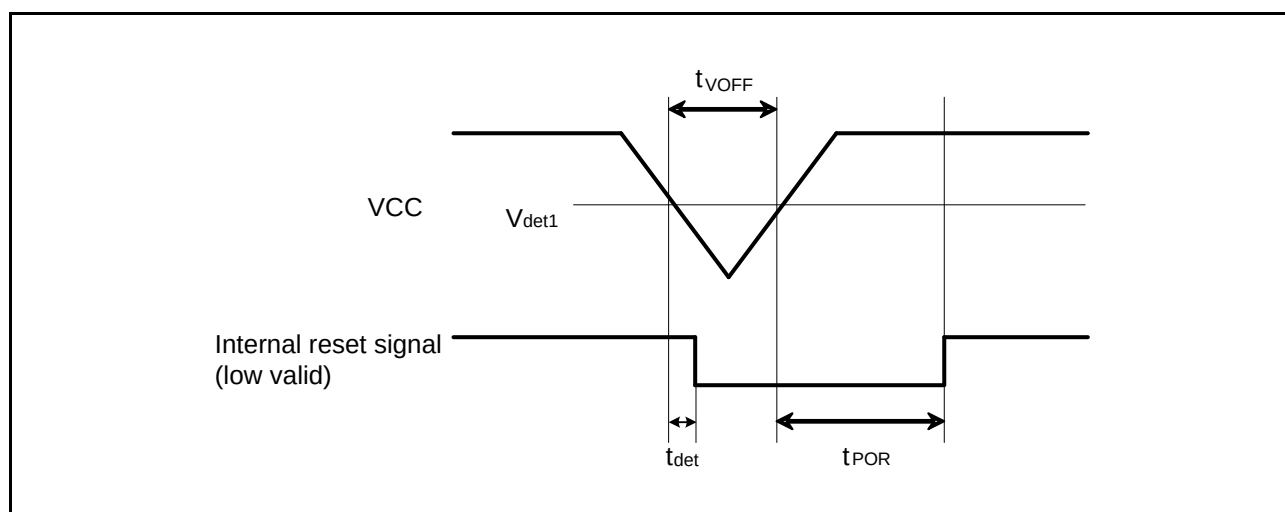
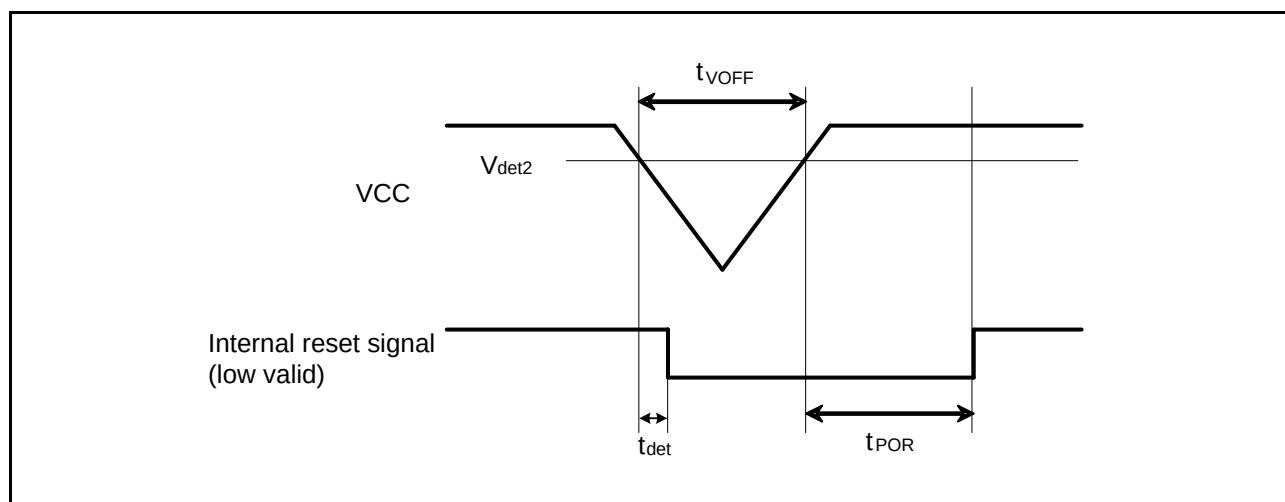
| Item                             |                                 | Symbol            | Min. | Typ. | Max. | Unit | Test Conditions             |
|----------------------------------|---------------------------------|-------------------|------|------|------|------|-----------------------------|
| Voltage detection level          | Power-on reset (POR)            | V <sub>POR</sub>  | 2.48 | 2.60 | 2.72 | V    | Figure 5.20                 |
|                                  | Voltage detection circuit (LVD) | V <sub>det1</sub> | 2.68 | 2.80 | 2.92 |      | Figure 5.21                 |
|                                  |                                 | V <sub>det2</sub> | 2.98 | 3.10 | 3.22 |      | Figure 5.22                 |
| Internal reset time              |                                 | t <sub>POR</sub>  | 20   | 35   | 50   | ms   | Figure 5.21 and Figure 5.22 |
| Min. VCC down time* <sup>1</sup> |                                 | t <sub>VOFF</sub> | 200  | -    | -    | us   | Figure 5.20 to Figure 5.22  |
| Reply delay time                 |                                 | t <sub>det</sub>  | -    | -    | 200  | us   |                             |

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC  
Ta = Topr

| Item                    |                                 | Symbol            | Min. | Typ. | Max. | Unit | Test Conditions             |
|-------------------------|---------------------------------|-------------------|------|------|------|------|-----------------------------|
| Voltage detection level | Power-on reset (POR)            | V <sub>POR</sub>  | 3.70 | 3.90 | 4.10 | V    | Figure 5.20                 |
|                         | Voltage detection circuit (LVD) | V <sub>det1</sub> | 3.95 | 4.15 | 4.35 |      | Figure 5.21                 |
|                         |                                 | V <sub>det2</sub> | 4.40 | 4.60 | 4.80 |      | Figure 5.22                 |
| Internal reset time     |                                 | t <sub>POR</sub>  | 20   | 35   | 50   | ms   | Figure 5.21 and Figure 5.22 |
| Min. VCC down time*1    |                                 | t <sub>VOFF</sub> | 200  | -    | -    | us   | Figure 5.20 to Figure 5.22  |
| Reply delay time        |                                 | t <sub>det</sub>  | -    | -    | 200  | us   |                             |

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels V<sub>POR</sub>, V<sub>det1</sub>, and V<sub>det2</sub> for the POR/ LVD.


**Figure 5.20 Power-on Reset Timing**

**Figure 5.21** Voltage Detection Circuit Timing ( $V_{det1}$ )**Figure 5.22** Voltage Detection Circuit Timing ( $V_{det2}$ )

## 5.6 Oscillation Stop Detection Timing

**Table 5.20 Oscillation Stop Detection Circuit Characteristics**

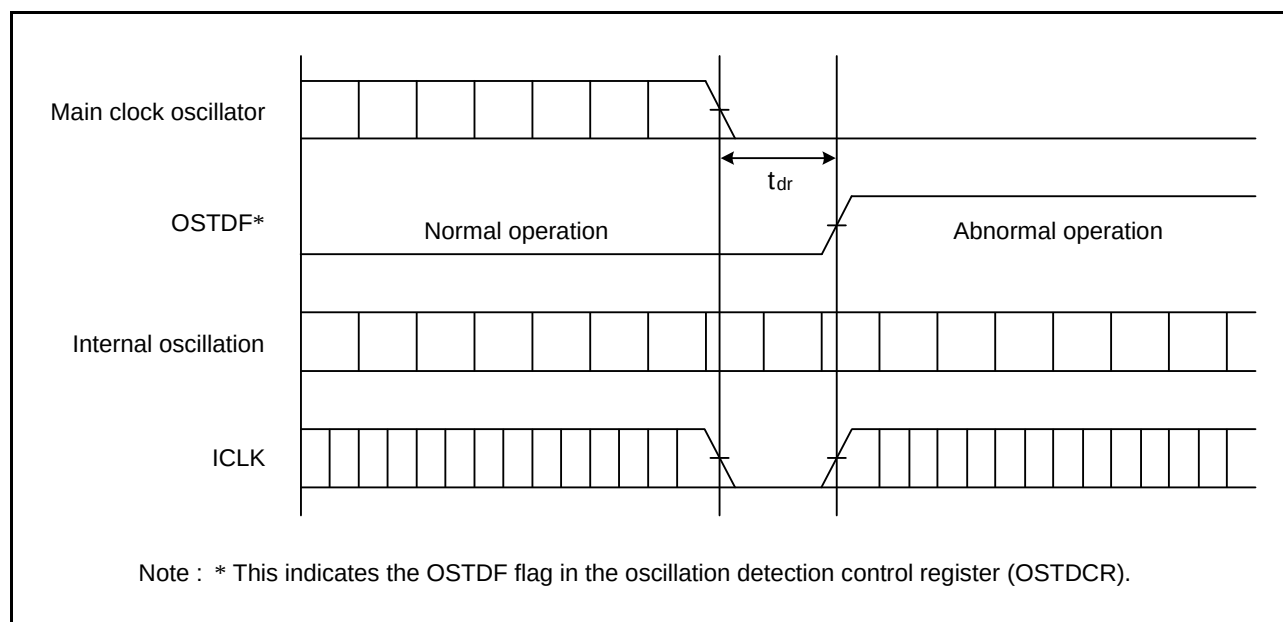
Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC  
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item                                                             | Symbol            | Min. | Typ. | Max. | Unit | Test Conditions |
|------------------------------------------------------------------|-------------------|------|------|------|------|-----------------|
| Detection time                                                   | t <sub>dr</sub>   | -    | -    | 1.0  | ms   | Figure 5.23     |
| Internal oscillation frequency when oscillation stop is detected | f <sub>MAIN</sub> | 0.5  | -    | 7.0  | MHz  |                 |



**Figure 5.23 Oscillation Stop Detection Timing**

## 5.7 ROM (Flash Memory for Code Storage) Characteristics

**Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1)**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:  
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item                              | Symbol           | Min.             | Typ. | Max. | Unit  | Test Conditions |
|-----------------------------------|------------------|------------------|------|------|-------|-----------------|
| Rewrite/erase cycle <sup>*1</sup> | N <sub>PEC</sub> | 1000             | —    | —    | Times |                 |
| Data hold time                    | t <sub>DRP</sub> | 30 <sup>*2</sup> | —    | —    | Year  | Ta = +85C°      |

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

**Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2)**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V  
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:  
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item                                                                |           | Symbol             | Min. | Typ. | Max. | Unit | Test Conditions                         |
|---------------------------------------------------------------------|-----------|--------------------|------|------|------|------|-----------------------------------------|
| Programming time                                                    | 256 bytes | t <sub>P256</sub>  | —    | 2    | 12   | ms   | PCLK = 50 MHz<br>N <sub>PEC</sub> ≤ 100 |
|                                                                     | 4 Kbytes  | t <sub>P4K</sub>   | —    | 23   | 50   | ms   |                                         |
|                                                                     | 16 Kbytes | t <sub>P16K</sub>  | —    | 90   | 200  | ms   |                                         |
|                                                                     | 256 byte  | t <sub>P256</sub>  | —    | 2.4  | 14.4 | ms   | PCLK = 50 MHz<br>N <sub>PEC</sub> > 100 |
|                                                                     | 4 Kbytes  | t <sub>P4K</sub>   | —    | 27.6 | 60   | ms   |                                         |
|                                                                     | 16 Kbytes | t <sub>P16K</sub>  | —    | 108  | 240  | ms   |                                         |
| Erasure time                                                        | 4 Kbytes  | t <sub>E4K</sub>   | —    | 25   | 60   | ms   | PCLK = 50 MHz<br>N <sub>PEC</sub> ≤ 100 |
|                                                                     | 16 Kbytes | t <sub>E16K</sub>  | —    | 100  | 240  | ms   |                                         |
|                                                                     | 4 Kbytes  | t <sub>E4K</sub>   | —    | 30   | 72   | ms   | PCLK = 50 MHz<br>N <sub>PEC</sub> > 100 |
|                                                                     | 16 Kbytes | t <sub>E16K</sub>  | —    | 120  | 288  | ms   |                                         |
| Suspend delay time during writing                                   |           | t <sub>SPD</sub>   | —    | —    | 120  | μs   | Figure 5.24<br>PCLK = 50 MHz            |
| First suspend delay time during erasing (in suspend priority mode)  |           | t <sub>SESD1</sub> | —    | —    | 120  | μs   |                                         |
| Second suspend delay time during erasing (in suspend priority mode) |           | t <sub>SESD2</sub> | —    | —    | 1.7  | ms   |                                         |
| Suspend delay time during erasing (in erasure priority mode)        |           | t <sub>SEED</sub>  | —    | —    | 1.7  | ms   |                                         |

## Notice

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