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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562taddff-v3

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range									
RX62T	R5F562TAADFH	R5F562TAADFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support- ed	-40 to +85°C (D version)									
	R5F562TAADFP	R5F562TAADFP#V3	PLQP0100KB-A															
	R5F562TAADFF	R5F562TAADFF#V3	PLQP0080JA-A															
	R5F562TAGDFF	R5F562TAGDFF#V3	PLQP0080JA-A															
	R5F562TAADFM	R5F562TAADFM#V3	PLQP0064KB-A															
	R5F562TAADFK	R5F562TAADFK#V3	PLQP0064GA-A															
	R5F562T7ADFH	R5F562T7ADFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes												
	R5F562T7ADFP	R5F562T7ADFP#V3	PLQP0100KB-A															
	R5F562T7ADFF	R5F562T7ADFF#V3	PLQP0080JA-A															
	R5F562T7GDFF	R5F562T7GDFF#V3	PLQP0080JA-A															
	R5F562T7ADFM	R5F562T7ADFM#V3	PLQP0064KB-A															
	R5F562T7ADFK	R5F562T7ADFK#V3	PLQP0064GA-A															
	R5F562T6ADFF	R5F562T6ADFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes													
	R5F562T6ADFM	R5F562T6ADFM#V3	PLQP0064KB-A															
	R5F562T6ADFK	R5F562T6ADFK#V3	PLQP0064GA-A															
	R5F562TABDFH	R5F562TABDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V											
	R5F562TABDFP	R5F562TABDFP#V3	PLQP0100KB-A															
	R5F562TABDFF	R5F562TABDFF#V3	PLQP0080JA-A															
	R5F562TABDFM	R5F562TABDFM#V3	PLQP0064KB-A															
	R5F562TABDFK	R5F562TABDFK#V3	PLQP0064GA-A															
	R5F562T7BDFH	R5F562T7BDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes												
	R5F562T7BDFP	R5F562T7BDFP#V3	PLQP0100KB-A															
	R5F562T7BDFF	R5F562T7BDFF#V3	PLQP0080JA-A															
	R5F562T7BDFM	R5F562T7BDFM#V3	PLQP0064KB-A															
	R5F562T7BDFK	R5F562T7BDFK#V3	PLQP0064GA-A															
	R5F562T6BDFF	R5F562T6BDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes													
	R5F562T6BDFM	R5F562T6BDFM#V3	PLQP0064KB-A															
	R5F562T6BDFK	R5F562T6BDFK#V3	PLQP0064GA-A															
	R5F562TADDFH	R5F562TADDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	4.0 to 5.5 V	Not Support- ed										
	R5F562TADDFP	R5F562TADDFP#V3	PLQP0100KB-A															
	R5F562TADDDFF	R5F562TADDDFF#V3	PLQP0080JA-A															
	R5F562TADDDFM	R5F562TADDDFM#V3	PLQP0064KB-A															
	R5F562TADDDFK	R5F562TADDDFK#V3	PLQP0064GA-A															
	R5F562T7DDFH	R5F562T7DDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes												
	R5F562T7DDFP	R5F562T7DDFP#V3	PLQP0100KB-A															
	R5F562T7DDFF	R5F562T7DDFF#V3	PLQP0080JA-A															
	R5F562T7DDFM	R5F562T7DDFM#V3	PLQP0064KB-A															
	R5F562T7DDFK	R5F562T7DDFK#V3	PLQP0064GA-A															
	R5F562T6DDFF	R5F562T6DDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes													
	R5F562T6DDFM	R5F562T6DDFM#V3	PLQP0064KB-A															
	R5F562T6DDFK	R5F562T6DDFK#V3	PLQP0064GA-A															
	R5F562TAEDFH	R5F562TAEDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	2.7 to 3.6 V											
	R5F562TAEDFP	R5F562TAEDFP#V3	PLQP0100KB-A															
	R5F562TAEDFF	R5F562TAEDFF#V3	PLQP0080JA-A															
	R5F562TAEDFM	R5F562TAEDFM#V3	PLQP0064KB-A															
	R5F562TAEDFK	R5F562TAEDFK#V3	PLQP0064GA-A															

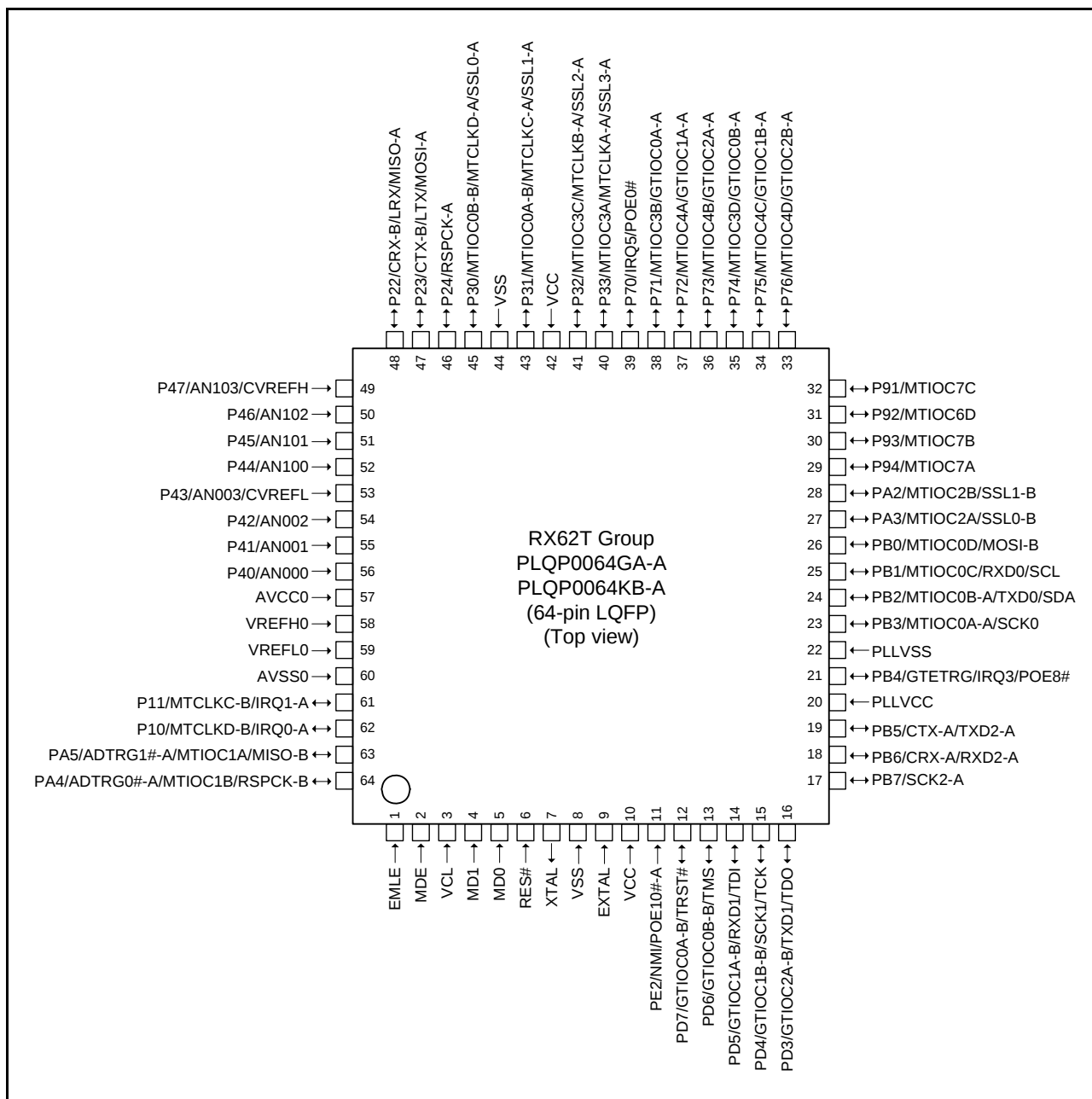


Figure 1.7 Pin Assignment of the 64-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/SSL1-C			TRST#
19		PD6		GTIOC0B-B	SSL0-C			TMS
20		PD5		GTIOC1A-B	RXD1			TDI
21		PD4		GTIOC1B-B	SCK1			TCK
22		PD3		GTIOC2A-B	TXD1			TDO
23		PD2		GTIOC2B-B	MOSI-C			TRCLK
24		PD1		GTIOC3A	MISO-C			TRDATA3
25		PD0		GTIOC3B	RSPCK-C			TRDATA2
26		PB7			SCK2-A			TRDATA1
27		PB6			CRX-A/ RXD2-A			TRDATA0
28		PB5			CTX-A/TXD2-A			TRSYNC
29	PLLVC							
30		PB4		GTETR		IRQ3	POE8#	
31	PLLVS							
32		PB3		MTIOC0A-A	SCK0			
33		PB2		MTIOC0B-A	TXD0/SDA			
34		PB1		MTIOC0C	RXD0/SCL			
35		PB0		MTIOC0D	MOSI-B			
36		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
37		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
38		PA3		MTIOC2A	SSL0-B			
39		PA2		MTIOC2B	SSL1-B			
40		PA1		MTIOC6A	SSL2-B			

(4) Number of Access Cycles to I/O Registers

The number of access cycles to I/O registers is obtained by following equation.*

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided cycles for clock synchronization} + \\ & \text{Number of bus cycles for internal peripheral buses 1, 2, 4, and 6} \end{aligned}$$

The number of bus cycles for internal peripheral buses 1, 2, 4, and 6 differs according to the register to be accessed. For the number of access cycles to each I/O register, see Table 4.1, List of I/O Registers.

When peripheral functions connected to internal peripheral bus 6 are accessed, the number of divided cycles for clock synchronization is added.

Although the number of divided cycles for clock synchronization differs depending on the number of frequency ratio between ICLK and PCLK or bus access timing, the sum of the number of bus cycles for internal main bus 1 and the number of divided cycles for clock synchronization will be one PCLK at a maximum. Therefore, one PCLK is added to the number of access cycles shown in Table 4.1.

Note: • This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DTC).

Table 4.1 List of I/O Registers (Address Order) (18 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 1390h	MTU1	Timer input capture control register	TICCR	8	8	5 ICLK
000C 1400h	MTU2	Timer control register	TCR	8	8, 16	5 ICLK
000C 1401h	MTU2	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1402h	MTU2	Timer I/O control register	TIOR	8	8	5 ICLK
000C 1404h	MTU2	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1405h	MTU2	Timer status register	TSR	8	8	5 ICLK
000C 1406h	MTU2	Timer counter	TCNT	16	16	5 ICLK
000C 1408h	MTU2	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 140Ah	MTU2	Timer general register B	TGRB	16	16	5 ICLK
000C 1A00h	MTU6	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1A01h	MTU7	Timer control register	TCR	8	8	5 ICLK
000C 1A02h	MTU6	Timer mode register 1	TMDR1	8	8, 16	5 ICLK
000C 1A03h	MTU7	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1A04h	MTU6	Timer I/O control register H	TIORH	8	8, 16, 32	5 ICLK
000C 1A05h	MTU6	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1A06h	MTU7	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1A07h	MTU7	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1A08h	MTU6	Timer interrupt enable register	TIER	8	8, 16	5 ICLK
000C 1A09h	MTU7	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 1A0Ah	MTU	Timer output master enable register B	TOERB	8	8	5 ICLK
000C 1A0Eh	MTU	Timer output control register 1B	TOCR1B	8	8, 16	5 ICLK
000C 1A0Fh	MTU	Timer output control register 2B	TOCR2B	8	8	5 ICLK
000C 1A10h	MTU6	Timer counter	TCNT	16	16, 32	5 ICLK
000C 1A12h	MTU7	Timer counter	TCNT	16	16	5 ICLK
000C 1A14h	MTU	Timer cycle data register B	TCDRB	16	16, 32	5 ICLK
000C 1A16h	MTU	Timer dead time data register B	TDDRB	16	16	5 ICLK
000C 1A18h	MTU6	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 1A1Ah	MTU6	Timer general register B	TGRB	16	16	5 ICLK
000C 1A1Ch	MTU7	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 1A1Eh	MTU7	Timer general register B	TGRB	16	16	5 ICLK
000C 1A20h	MTU	Timer subcounter B	TCNTSB	16	16, 32	5 ICLK
000C 1A22h	MTU	Timer cycle buffer register B	TCBRB	16	16	5 ICLK
000C 1A24h	MTU6	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1A26h	MTU6	Timer general register D	TGRD	16	16	5 ICLK
000C 1A28h	MTU7	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1A2Ah	MTU7	Timer general register D	TGRD	16	16	5 ICLK
000C 1A2Ch	MTU6	Timer status register	TSR	8	8, 16	5 ICLK
000C 1A2Dh	MTU7	Timer status register	TSR	8	8	5 ICLK
000C 1A30h	MTU	Timer interrupt skipping set register 1B	TITCR1B	8	8, 16	5 ICLK
000C 1A31h	MTU	Timer interrupt skipping counter 1B	TITCNT1B	8	8	5 ICLK
000C 1A32h	MTU	Timer buffer transfer set register B	TBTERB	8	8	5 ICLK
000C 1A34h	MTU	Timer dead time enable register B	TDERB	8	8	5 ICLK
000C 1A36h	MTU	Timer output level buffer register B	TOLBRB	8	8	5 ICLK
000C 1A38h	MTU6	Timer buffer operation transfer mode register	TBTM	8	8, 16	5 ICLK

Table 4.1 List of I/O Registers (Address Order) (21 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 2116h	GPT0	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2118h	GPT0	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 211Ah	GPT0	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 211Ch	GPT0	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 211Eh	GPT0	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2120h	GPT0	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2124h	GPT0	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2126h	GPT0	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2128h	GPT0	A/D converter start request timing double-buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 212Ch	GPT0	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 212Eh	GPT0	A/D converter start request timing buffer register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2130h	GPT0	A/D converter start request timing double-buffer register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2134h	GPT0	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2136h	GPT0	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2138h	GPT0	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 213Ah	GPT0	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 213Ch	GPT0	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 213Eh	GPT0	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2140h	GPT0	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 2142h	GPT0	General PWM timer output protection function temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2180h	GPT1	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2182h	GPT1	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2184h	GPT1	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2186h	GPT1	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2188h	GPT1	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 218Ah	GPT1	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 218Ch	GPT1	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 218Eh	GPT1	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2190h	GPT1	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2192h	GPT1	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2194h	GPT1	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}
000C 2196h	GPT1	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2198h	GPT1	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 219Ah	GPT1	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 219Ch	GPT1	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 219Eh	GPT1	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.1 List of I/O Registers (Address Order) (23 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 222Ch	GPT2	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 222Eh	GPT2	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2230h	GPT2	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2234h	GPT2	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2236h	GPT2	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2238h	GPT2	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Ah	GPT2	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Ch	GPT2	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Eh	GPT2	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2240h	GPT2	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 2242h	GPT2	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2280h	GPT3	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2282h	GPT3	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2284h	GPT3	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2286h	GPT3	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2288h	GPT3	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Ah	GPT3	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Ch	GPT3	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Eh	GPT3	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2290h	GPT3	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2292h	GPT3	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2294h	GPT3	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}
000C 2296h	GPT3	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2298h	GPT3	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Ah	GPT3	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Ch	GPT3	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Eh	GPT3	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A0h	GPT3	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A4h	GPT3	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A6h	GPT3	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A8h	GPT3	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22ACh	GPT3	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22AEh	GPT3	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B0h	GPT3	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B4h	GPT3	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.2 List of I/O Registers (Bit Order) (8 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IPR03	—	—	—	—			IPR[3:0]	
ICU	IPR04	—	—	—	—			IPR[3:0]	
ICU	IPR05	—	—	—	—			IPR[3:0]	
ICU	IPR06	—	—	—	—			IPR[3:0]	
ICU	IPR07	—	—	—	—			IPR[3:0]	
ICU	IPR14	—	—	—	—			IPR[3:0]	
ICU	IPR18	—	—	—	—			IPR[3:0]	
ICU	IPR20	—	—	—	—			IPR[3:0]	
ICU	IPR21	—	—	—	—			IPR[3:0]	
ICU	IPR22	—	—	—	—			IPR[3:0]	
ICU	IPR23	—	—	—	—			IPR[3:0]	
ICU	IPR24	—	—	—	—			IPR[3:0]	
ICU	IPR25	—	—	—	—			IPR[3:0]	
ICU	IPR26	—	—	—	—			IPR[3:0]	
ICU	IPR27	—	—	—	—			IPR[3:0]	
ICU	IPR40	—	—	—	—			IPR[3:0]	
ICU	IPR44	—	—	—	—			IPR[3:0]	
ICU	IPR48	—	—	—	—			IPR[3:0]	
ICU	IPR49	—	—	—	—			IPR[3:0]	
ICU	IPR51	—	—	—	—			IPR[3:0]	
ICU	IPR52	—	—	—	—			IPR[3:0]	
ICU	IPR53	—	—	—	—			IPR[3:0]	
ICU	IPR54	—	—	—	—			IPR[3:0]	
ICU	IPR55	—	—	—	—			IPR[3:0]	
ICU	IPR56	—	—	—	—			IPR[3:0]	
ICU	IPR57	—	—	—	—			IPR[3:0]	
ICU	IPR58	—	—	—	—			IPR[3:0]	
ICU	IPR59	—	—	—	—			IPR[3:0]	
ICU	IPR5A	—	—	—	—			IPR[3:0]	
ICU	IPR5B	—	—	—	—			IPR[3:0]	
ICU	IPR5C	—	—	—	—			IPR[3:0]	
ICU	IPR5D	—	—	—	—			IPR[3:0]	
ICU	IPR5E	—	—	—	—			IPR[3:0]	
ICU	IPR5F	—	—	—	—			IPR[3:0]	
ICU	IPR60	—	—	—	—			IPR[3:0]	
ICU	IPR67	—	—	—	—			IPR[3:0]	
ICU	IPR68	—	—	—	—			IPR[3:0]	
ICU	IPR69	—	—	—	—			IPR[3:0]	
ICU	IPR6A	—	—	—	—			IPR[3:0]	
ICU	IPR6B	—	—	—	—			IPR[3:0]	
ICU	IPR6C	—	—	—	—			IPR[3:0]	
ICU	IPR6D	—	—	—	—			IPR[3:0]	
ICU	IPR6E	—	—	—	—			IPR[3:0]	
ICU	IPR6F	—	—	—	—			IPR[3:0]	
ICU	IPR80	—	—	—	—			IPR[3:0]	
ICU	IPR81	—	—	—	—			IPR[3:0]	
ICU	IPR82	—	—	—	—			IPR[3:0]	
ICU	IPR88	—	—	—	—			IPR[3:0]	
ICU	IPR89	—	—	—	—			IPR[3:0]	
ICU	IPR8A	—	—	—	—			IPR[3:0]	
ICU	IPR8B	—	—	—	—			IPR[3:0]	
ICU	IPR90	—	—	—	—			IPR[3:0]	

Table 4.2 List of I/O Registers (Bit Order) (10 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
AD0	ADDRB ^{*1}	—	—	—	—	—	—		
AD0	ADDRC ^{*1}	—	—	—	—	—	—		
AD0	ADDRD ^{*1}	—	—	—	—	—	—		
AD0	ADDRE ^{*1}	—	—	—	—	—	—		
AD0	ADDRF ^{*1}	—	—	—	—	—	—		
AD0	ADDRG ^{*1}	—	—	—	—	—	—		
AD0	ADDRH ^{*1}	—	—	—	—	—	—		
AD0	ADCSR	—	ADIE	ADST	—		CH[3:0]		
AD0	ADCR	—	—	—	—	CKS[1:0]		MODE[1:0]	
AD0	ADSSTR								
AD0	ADDIAGR	—	—	—	—	—	—	DIAG[1:0]	
AD0	ADDRI ^{*1}	—	—	—	—	—	—		
AD0	ADDRJ ^{*1}	—	—	—	—	—	—		
AD0	ADDRK ^{*1}	—	—	—	—	—	—		
AD0	ADDRL ^{*1}	—	—	—	—	—	—		
AD0	ADSTRGR	—	—	—		ADSTRS[4:0]			
AD0	ADDP	DPSEL	—	—	—	—	—	—	DPPRC
SCI0	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI0	BRR								
SCI0	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI0	TDR								
SCI0	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI0	RDR								
SCI0	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI0	SEMR	—	—	NFEN	ABCS	—	—	—	—
SMCI0	SMR	GM	BLK	PE	PM	(BCP[1:0])		CKS[1:0]	
SMCI0	BRR								
SMCI0	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMCI0	TDR								
SMCI0	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMCI0	RDR								
SMCI0	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI1	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI1	BRR								
SCI1	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI1	TDR								
SCI1	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI1	RDR								
SCI1	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF

Table 4.2 List of I/O Registers (Bit Order) (11 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SCI1	SEMR	—	—	NFEN	ABCS	—	—	—	—
SMC11	SMR	GM	BLK	PE	PM	(BCP[1:0])			CKS[1:0]
SMC11	BRR								
SMC11	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMC11	TDR								
SMC11	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMC11	RDR								
SMC11	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI2	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI2	BRR								
SCI2	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI2	TDR								
SCI2	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI2	RDR								
SCI2	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SMC12	SMR	GM	BLK	PE	PM	(BCP[1:0])			CKS[1:0]
SMC12	BRR								
SMC12	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMC12	TDR								
SMC12	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMC12	RDR								
SMC12	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
CRC	CRCCR	DORCLR	—	—	—	—	LMS	GPS[1:0]	
CRC	CRCDIR								
CRC	CRCDOR								
RIIC0	ICCR1	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
RIIC0	ICCR2	BBSY	MST	TRS	—	SP	RS	ST	—
RIIC0	ICMR1	MTWP		CKS[2:0]		BCWP		BC[2:0]	
RIIC0	ICMR2	DLCS		SDDL[2:0]		TMWE	TMOH	TMOL	TMOS
RIIC0	ICMR3	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
RIIC0	ICFER	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
RIIC0	ICSER	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
RIIC0	ICIER	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
RIIC0	ICSR1	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
RIIC0	ICSR2	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
RIIC0	SARL0				SVA[6:0]				SVA0
RIIC0	TMOCTL								
RIIC0	SARU0	—	—	—	—	—	SVA[1:0]		FS
RIIC0	TMOCNTU								
RIIC0	SARL1				SVA[6:0]				SVA0
RIIC0	SARU1	—	—	—	—	—	SVA[1:0]		FS
RIIC0	SARL2				SVA[6:0]				SVA0
RIIC0	SARU2	—	—	—	—	—	SVA[1:0]		FS
RIIC0	ICBRL	—	—	—			BRL[4:0]		
RIIC0	ICBRH	—	—	—			BRH[4:0]		
RIIC0	ICDRT								
RIIC0	ICDRR								
RSP10	SPCR	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS

Table 4.2 List of I/O Registers (Bit Order) (13 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
S12AD0	ADDRD ^{*2}	DIAGST[1:0]		—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR0A ^{*2}	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR1 ^{*2}	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR2 ^{*2}	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR3 ^{*2}	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR0B ^{*2}	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADSSTR								
S12AD1	ADCSR	ADST	ADCS[1:0]		ADIE	CKS[1:0]		TRGE	EXTRG
S12AD1	ADANS	—	—	CH[1:0]		—	PG102SEL	PG101SEL	PG100SEL
		—	—	—	—	—	PG102EN	PG101EN	PG100EN
S12AD1	ADPG	—	—	—	—	PG102GAIN[3:0]			
		PG101GAIN[3:0]				PG100GAIN[3:0]			
S12AD1	ADCER	ADRFMT	—	ADIEW	ADIE2	DIAGM	DIAGLD	DIAGVAL[1:0]	
		—	—	ACE	—	—	ADPRC[1:0]		SHBYP
S12AD1	ADSTRGR	—	—	—	ADSTRS1[4:0]				
		—	—	—	ADSTRS0[4:0]				
S12AD1	ADDRD ^{*2}	DIAGST[1:0]		—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR0A ^{*2}	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR1 ^{*2}	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR2 ^{*2}	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR3 ^{*2}	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR0B ^{*2}	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADSSTR								
PORT1	DDR	—	—	—	—	—	—	B1	B0
PORT2	DDR	—	—	—	B4	B3	B2	B1	B0
PORT3	DDR	—	—	—	—	B3	B2	B1	B0
PORT7	DDR	—	B6	B5	B4	B3	B2	B1	B0
PORT8	DDR	—	—	—	—	—	B2	B1	B0
PORT9	DDR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	DDR	—	—	B5	B4	B3	B2	B1	B0
PORTB	DDR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	DDR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	DDR	—	—	B5	B4	B3	—	B1	B0
PORTG	DDR	—	—	B5	B4	B3	B2	B1	B0
PORT1	DR	—	—	—	—	—	—	B1	B0
PORT2	DR	—	—	—	B4	B3	B2	B1	B0
PORT3	DR	—	—	—	—	B3	B2	B1	B0
PORT7	DR	—	B6	B5	B4	B3	B2	B1	B0

Table 4.2 List of I/O Registers (Bit Order) (20 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU0	TMDR1	—	BFE	BFB	BFA			MD[3:0]	
MTU0	TIORH			IOB[3:0]				IOA[3:0]	
MTU0	TIORL			IOD[3:0]				IOC[3:0]	
MTU0	TIER	TTEG	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU0	TSR	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU0	TCNT								
MTU0	TGRA								
MTU0	TGRB								
MTU0	TGRC								
MTU0	TGRD								
MTU0	TGRE								
MTU0	TGRF								
MTU0	TIER2	TTGE2	—	—	—	—	—	TGIEF	TGIEE
MTU0	TSR2	—	—	—	—	—	—	TGFF	TGFE
MTU0	TBTM	—	—	—	—	—	TTSE	TTSB	TTSA
MTU1	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU1	TMDR1	—	—	—	—			MD[3:0]	
MTU1	TIOR		IOB[3:0]					IOA[3:0]	
MTU1	TIER	TTEG	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU1	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU1	TCNT								
MTU1	TGRA								
MTU1	TGRB								
MTU1	TICCR	—	—	—	—	I2BE	I2AE	I1BE	I1AE
MTU2	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU2	TMDR1	—	—	—	—			MD[3:0]	
MTU2	TIOR		IOB[3:0]					IOA[3:0]	
MTU2	TIER	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU2	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU2	TCNT								
MTU2	TGRA								
MTU2	TGRB								
MTU6	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU7	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU6	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU7	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU6	TIORH		IOB[3:0]					IOA[3:0]	
MTU6	TIORL		IOD[3:0]					IOC[3:0]	
MTU7	TIORH		IOB[3:0]					IOA[3:0]	

Table 4.2 List of I/O Registers (Bit Order) (28 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT3	GTCCRB								
GPT3	GTCCRC								
GPT3	GTCCRD								
GPT3	GTCCRE								
GPT3	GTCCRF								
GPT3	GTPR								
GPT3	GTPBR								
GPT3	GTPDBR								
GPT3	GTADTRA								
GPT3	GTADTBRA								
GPT3	GTADTDBRA								
GPT3	GTADTRB								
GPT3	GTADTBRB								
GPT3	GTADTDBRB								
GPT3	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
				NFS[3:0]		NVB	NVA	NEB	NEA
GPT3	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT3	GTDVU								
GPT3	GTDVD								
GPT3	GTDBU								
GPT3	GTDBD	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT3	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT3	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT0	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT1	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN

Table 4.2 List of I/O Registers (Bit Order) (30 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
FLASH	FSTATR0	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	—	ERSSPD	PRGSPD
FLASH	FSTATR1	FCUERR	—	—	FLOCKST	—	—	—	—
FLASH	FENTRYR	FEKEY[7:0]							
		FENTRYD	—	—	—	—	—	—	FENTRY0
FLASH	FPROTR	FPKEY[7:0]							
		—	—	—	—	—	—	—	FPROTCN
FLASH	FRESETR	FRKEY[7:0]							
		—	—	—	—	—	—	—	FRESET
FLASH	FCMDR	CMDR[7:0]							
		PCMDR[7:0]							
FLASH	FCPSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	ESUSPMD
FLASH	DFLBCCNT	BCADR[7:0]							
		BCADR[7:0]							
FLASH	FPESTAT	—	—	—	—	—	—	—	—
		PEERRST[7:0]							
FLASH	DFLBCSTAT	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	BCST
FLASH	PCKAR	—	—	—	—	—	—	—	—
		PCKA[7:0]							

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.

Table 5.2 DC Characteristics (1) (3 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input capacitance	All input pins (except for ports PB1 and PB2)	C _{in}	-	-	15	pF	V _{in} = 0 V, f = 1 MHz, T _a = 25°C
	Ports PB1 and PB2		-	-	30		

Note 1. This includes the multiplexed input pins, except in cases where port pins PB1 and PB2 are used as IIC input pins or port pins P22 to P24, P30, PA3 to PA5, PB0, PD0 to PD2, or PD6 are used as RSPI input pins.

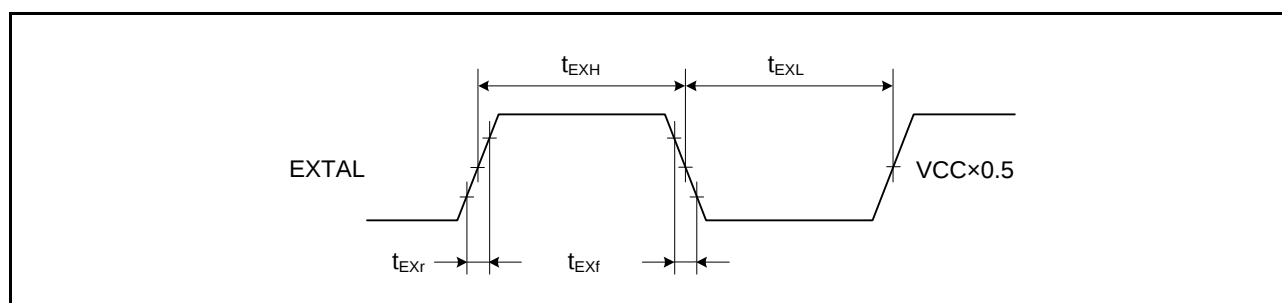


Figure 5.4 EXTAL External Input Clock Timing

5.3.2 Control Signal Timing

Table 5.8 Control Signal Timing

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory*1)	t_{RESW}^{*2}	20	-	t_{cyc}^{*4}	Figure 5.5
		1.5	-	μs	
Internal reset time*3	t_{RESW2}	35	-	μs	
NMI pulse width	t_{NMIW}	200	-	ns	Figure 5.6
IRQ pulse width	t_{IRQW}	200	-	ns	Figure 5.7

Note 1. For a reset by the signal on the RES# pin during programming or erasure of the ROM or data-flash memory or during blank checking of the data-flash memory, see section 31.12, Usage Notes in section 31, ROM (Flash Memory for Code Storage) in the User's manual: Hardware.

Note 2. Both the time and the number of cycles should satisfy the specifications.

Note 3. This is to specify the FCU reset.

Note 4. ICLK cycles.

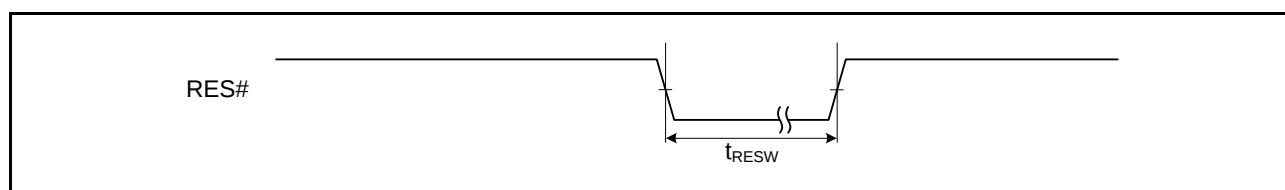
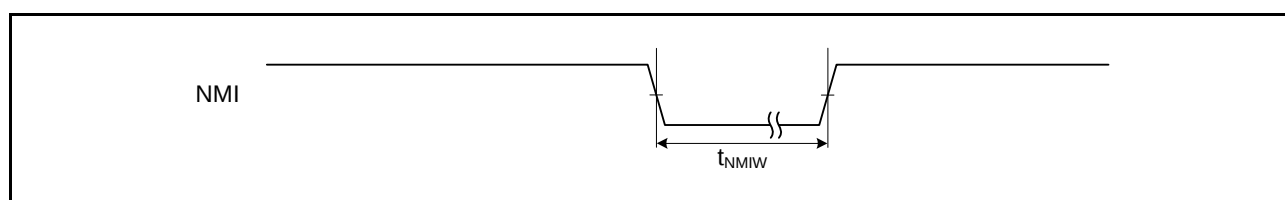
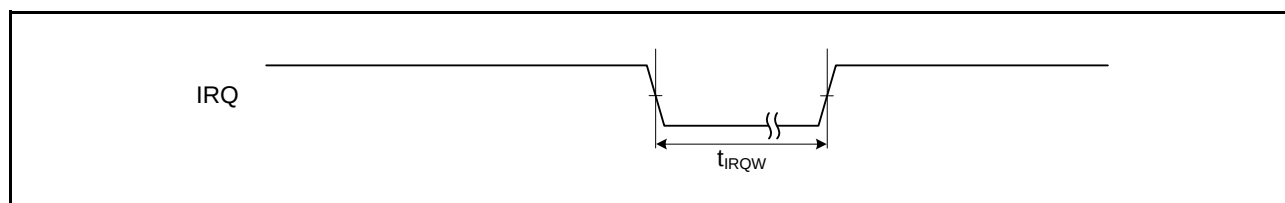

Figure 5.5 Reset Input Timing

Figure 5.6 NMI Interrupt Input Timing

Figure 5.7 IRQ Interrupt Input Timing

Table 5.16 12-Bit A/D Conversion Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Ta = Topr, ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	12	12	12	Bit	
Conversion time*1 (AD clock = 25-MHz operation)	2.0	-	-	μs	Sampling 20 states
Analog input capacitance	-	-	6	pF	
Integral nonlinearity error	-	-	±4.0	LSB	
Offset error	-	-	±7.5	LSB	
Full-scale error	-	-	±7.5	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	When a sample-and-hold circuit is in use	-	±8.0	LSB	AVin = 0.25 to AVREFH - 0.25
	When a sample-and-hold circuit is not in use	-	±8.0	LSB	AVin = AVREFL to AVREFH
Permissible signal source impedance	-	-	3.0	kΩ	

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 2 and 3. ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz.

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	12	12	12	Bit	
Conversion time*1 (AD clock = 25-MHz operation)	1.0	-	-	μs	Sampling 20 states
Analog input capacitance	-	-	6	pF	
Integral nonlinearity error	-	-	±4.0	LSB	
Offset error	-	-	±7.5	LSB	
Full-scale error	-	-	±7.5	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	When a sample-and-hold circuit is in use	-	±8.0	LSB	AVin = 0.25 to AVREFH - 0.25
	When a sample-and-hold circuit is not in use	-	±8.0	LSB	AVin = AVREFL to AVREFH
Permissible signal source impedance	-	-	3.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Appendix 1.Package Dimensions

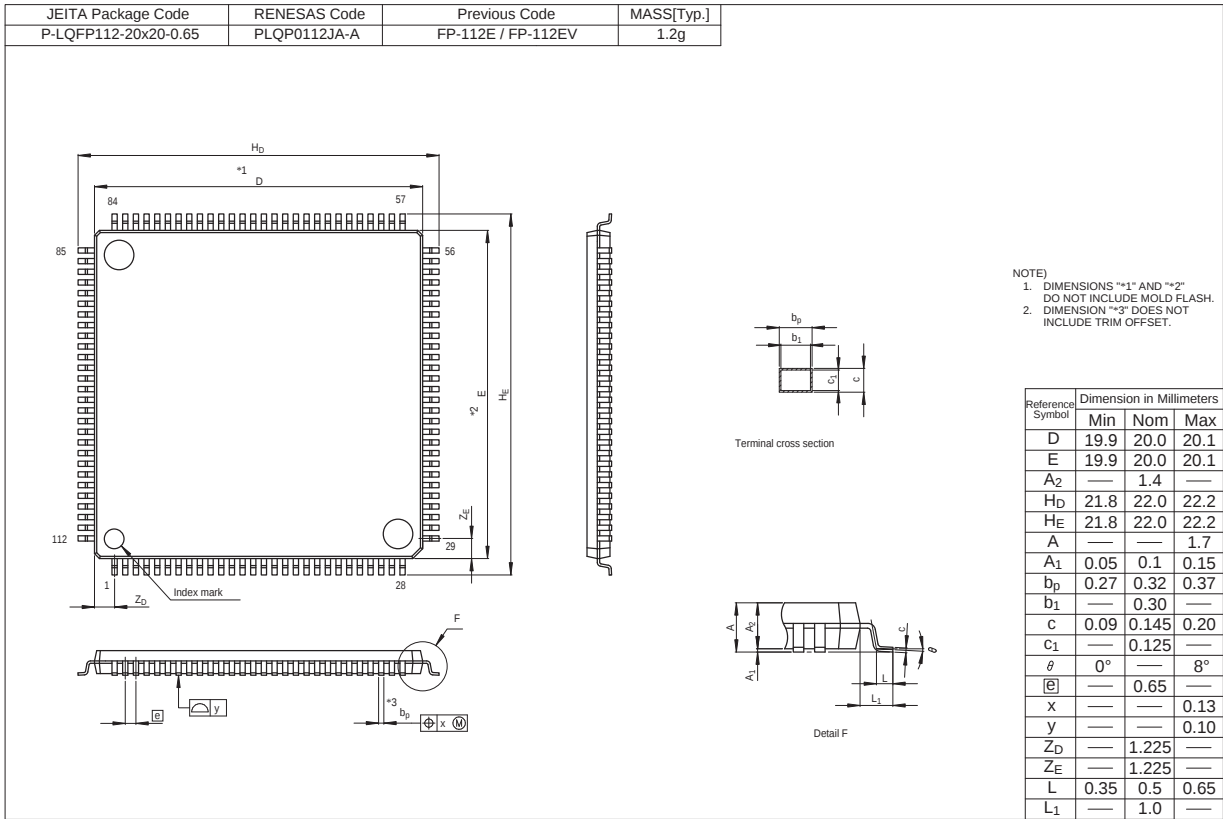


Figure A 112-Pin LQFP (PLQP0112JA-A) Package Dimensions

Rev.	Date	Description	
		Page	Summary
2.00	Jan 10, 2014	98	Table 5.1 Absolute Maximum Ratings, changed
		102	Table 5.3 DC Characteristics (2): Note 3, changed
		103	Table 5.5 Permissible Power Consumption, added
		117	5.3.4 Timing of PWM Delay Generation Circuit, added
		117	Table 5.14 Timing of the PWM Delay Generation Circuit, added
		120	Table 5.17 Characteristics of the Programmable Gain Amplifier, changed
		125	Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1), changed
		125	Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2), added
		126	Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1), changed
		126	Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2), added

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