# Renesas Electronics America Inc - R5F562TADDFH#V1 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | I²C, LINbus, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 61 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 12x10b, 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 112-LQFP |
| Supplier Device Package | 112-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562taddfh-v1 |

**Table 1.1 Outline of Specifications (2 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| Interrupt | Interrupt controller (ICU) | • Peripheral function interrupts: 101 sources<br>• External interrupts: 9 (NMI and IRQ0 to IRQ7 pins)<br>• Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt)<br>• 16 levels specifiable for the order of priority |
| Data transfer | Data transfer controller (DTC) | • Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions |
| I/O ports | Programmable I/O ports | I/O port pins for devices in the 112-pin LQFP/100-pin LQFP/<br>80-pin LQFP (R5F562TxGDFF)/80-pin LQFP (except R5F562TxGDFF)/64-pin LQFP<br>• I/O: 61/55/44/44/37<br>• Input only: 21/21/13/13/9<br>• Open-drain outputs: 2/2/2/2/2 ($I^2C$ bus interface pins)<br>• Large-current outputs: 12/12/12/6/6(0) (MTU3 and GPT pins)<br>The 5-V version of the 64-pin product does not have large-current outputs.<br>• Reading out the states of pins is always possible. |
| Timers | Multi-function timer pulse unit 3 (MTU3) | • 16 bits x 8 channels<br>• Up to 24 pulse inputs/outputs and three pulse inputs<br>• Select from among six to eight counter-input clock signals for each channel (ICLK/1, ICLK/4, ICLK/16, ICLK/64, ICLK/256, ICLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available.<br>• 24 output compare or input capture registers<br>• Counter clearing (clearing is synchronizable with compare match or input capture)<br>• Simultaneous writing to multiple timer counters (TCNT)<br>• Input to and output from all registers in synchronization with counter operation<br>• Buffered operation<br>• Cascade-connected operation<br>• 38 kinds of interrupt source<br>• Automatic transfer of register data<br>• Pulse output modes<br>Toggled, PWM, complementary PWM, and reset synchronous PWM<br>• Complementary PWM output mode<br>Outputs non-overlapping waveforms for controlling 3-phase inverters<br>Automatic specification of dead times<br>PWM duty cycle: Selectable as any value from 0% to 100%<br>Delay can be applied to requests for A/D conversion.<br>Non-generation of interrupt requests at peak or trough values of counters can be selected.<br>Double buffering<br>• Reset-synchronous PWM mode<br>Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles.<br>• Phase-counting mode<br>• Counter functionality for dead-time compensation<br>• Generation of triggers for A/D converters<br>• Differential timing for initiation of A/D conversion |
| | Port output enable 3 (POE3) | • Control of the high-impedance state of the MTU3 and GPT's waveform output pins<br>5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11<br>Initiation on detection of short-circuited outputs (detection of simultaneous switching of large-current pins to the active level)<br>Initiation by comparator-detection of analog level input to the 12-bit A/D converter<br>Initiation by oscillation-stoppage detection<br>Initiation by software<br>• Selection of which output pins should be placed in the high-impedance state at the time of each POE input or comparator detection |

**Table 1.1 Outline of Specifications (5 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| A/D converter | 10-bit A/D converter (ADA) | • 10 bits (1 unit x 12 channels)<br>• 10-bit resolution<br>• Conversion time:<br>1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V<br>2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V<br>• Two basic operating modes<br>Single mode and scan mode<br>• Scan mode<br>One-cycle scan mode<br>Continuous scan mode<br>• Sample-and-hold function<br>A common sample-and-hold circuit for both units is included.<br>• A/D-conversion register settings for each input pin<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal.<br>• Functionality for 8-bit precision output<br>Right-shifting the results of conversion for output by two bits is selectable.<br>• Self-diagnostic function<br>The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF). |
| CRC calculator (CRC) | | • CRC code generation for arbitrary amounts of data in 8-bit units<br>• Select any of three generating polynomials:<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$.<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable. |
| Operating frequency | | ICLK: 8 to 100 MHz<br>PCLK: 8 to 50 MHz |
| Power supply voltage | | • 3-V version<br>VCC = PLLVCC = 2.7 to 3.6V<br>AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V<br>VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0<br>VREF = 3.0 to AVCC, or 4.0 to AVCC<br>• 5-V version<br>VCC = PLLVCC = 4.0 to 5.5V<br>AVCC0 = AVCC = 4.0 to 5.5V<br>VREFH0 = 4.0 to AVCC0<br>VREF = 4.0 to AVCC |
| Operating temperature | | D version: -40 to +85°C, G version: -40 to +105°C*1 |
| Packages | | 112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch)<br>100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch)<br>80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch)<br>64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch)<br>64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch) |

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

**Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (1 / 3)**

| Pin No. (112-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 1 | | PE5 | | | | IRQ0-B | | |
| 2 | EMLE | | | | | | | |
| 3 | VSS | | | | | | | |
| 4 | MDE | | | | | | | |
| 5 | VCL | | | | | | | |
| 6 | MD1 | | | | | | | |
| 7 | MD0 | | | | | | | |
| 8 | | PE4 | | MTCLKC-C | | IRQ1-B | POE10#-B | |
| 9 | | PE3 | | MTCLKD-C | | IRQ2-A | POE11# | |
| 10 | RES# | | | | | | | |
| 11 | XTAL | | | | | | | |
| 12 | VSS | | | | | | | |
| 13 | EXTAL | | | | | | | |
| 14 | VCC | | | | | | | |
| 15 | | PE2 | | | | NMI | POE10#-A | |
| 16 | | PE1 | | | SSL3-C | | | |
| 17 | | PE0 | | | CRX-C/ SSL2-C | | | |
| 18 | | PD7 | | GTIOC0A-B | CTX-C/ SSL1-C | | | |
| 19 | | PD6 | | GTIOC0B-B | SSL0-C | | | |
| 20 | | PD5 | | GTIOC1A-B | RXD1 | | | |
| 21 | | PD4 | | GTIOC1B-B | SCK1 | | | |
| 22 | | PD3 | | GTIOC2A-B | TXD1 | | | |
| 23 | | PD2 | | GTIOC2B-B | MOSI-C | | | |
| 24 | | PD1 | | GTIOC3A | MISO-C | | | |
| 25 | | PD0 | | GTIOC3B | RSPCK-C | | | |
| 26 | | | | | | | | TDI |
| 27 | | | | | | | | TCK |
| 28 | | | | | | | | TDO |
| 29 | | PB7 | | | SCK2-A | | | |
| 30 | | PB6 | | | CRX-A/ RXD2-A | | | |
| 31 | | PB5 | | | CTX-A/ TXD2-A | | | |
| 32 | PLLVCC | | | | | | | |
| 33 | | PB4 | | GTETRG | | IRQ3 | POE8# | |
| 34 | PLLVSS | | | | | | | |
| 35 | | PB3 | | MTIOC0A-A | SCK0 | | | |
| 36 | | PB2 | | MTIOC0B-A | TXD0/SDA | | | |
| 37 | | PB1 | | MTIOC0C | RXD0/SCL | | | |
| 38 | | PB0 | | MTIOC0D | MOSI-B | | | |
| 39 | | PA5 | ADTRG1#-A | MTIOC1A | MISO-B | | | |
| 40 | | PA4 | ADTRG0#-A | MTIOC1B | RSPCK-B | | | |
| 41 | | PA3 | | MTIOC2A | SSL0-B | | | |
| 42 | | PA2 | | MTIOC2B | SSL1-B | | | |
| 43 | | PA1 | | MTIOC6A | SSL2-B | | | |

**Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 77 | | P60 | AN0 | | | | | |
| 78 | | P55 | AN11 | | | | | |
| 79 | | P54 | AN10 | | | | | |
| 80 | | P53 | AN9 | | | | | |
| 81 | | P52 | AN8 | | | | | |
| 82 | | P51 | AN7 | | | | | |
| 83 | | P50 | AN6 | | | | | |
| 84 | | P47 | AN103/ CVREFH | | | | | |
| 85 | | P46 | AN102 | | | | | |
| 86 | | P45 | AN101 | | | | | |
| 87 | | P44 | AN100 | | | | | |
| 88 | | P43 | AN003/ CVREFL | | | | | |
| 89 | | P42 | AN002 | | | | | |
| 90 | | P41 | AN001 | | | | | |
| 91 | | P40 | AN000 | | | | | |
| 92 | AVCC0 | | | | | | | |
| 93 | VREFH0 | | | | | | | |
| 94 | VREFL0 | | | | | | | |
| 95 | AVSS0 | | | | | | | |
| 96 | | P82 | | MTIC5U | SCK2-B | | | |
| 97 | | P81 | | MTIC5V | TXD2-B | | | |
| 98 | | P80 | | MTIC5W | RXD2-B | | | |
| 99 | | P11 | | MTCLKC-B | | IRQ1-A | | |
| 100 | | P10 | | MTCLKD-B | | IRQ0-A | | |

**Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (2 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communication | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 42 | | P76 | | MTIOC4D/ GTIOC2B-A | | | | |
| 43 | | P75 | | MTIOC4C/ GTIOC1B-A | | | | |
| 44 | | P74 | | MTIOC3D/ GTIOC0B-A | | | | |
| 45 | | P73 | | MTIOC4B/ GTIOC2A-A | | | | |
| 46 | | P72 | | MTIOC4A/ GTIOC1A-A | | | | |
| 47 | | P71 | | MTIOC3B/ GTIOC0A-A | | | | |
| 48 | | P70 | | | | IRQ5 | POE0# | |
| 49 | | P33 | | MTIOC3A/ MTCLKA-A | SSL3-A | | | |
| 50 | | P32 | | MTIOC3C/ MTCLKB-A | SSL2-A | | | |
| 51 | VCC | | | | | | | |
| 52 | | P31 | | MTIOC0A-B/ MTCLKC-A | SSL1-A | | | |
| 53 | VSS | | | | | | | |
| 54 | | P30 | | MTIOC0B-B/ MTCLKD-A | SSL0-A | | | |
| 55 | | P24 | | | RSPCK-A | | | |
| 56 | | P23 | | | CTX-B/ LTX/ MOSI-A | | | |
| 57 | | P22 | ADTRG# | | CRX-B/ LRX/ MISO-A | | | |
| 58 | | P20 | ADTRG0#-B | MTCLKB-B | | IRQ7 | | |
| 59 | AVCC | | | | | | | |
| 60 | AVSS | | | | | | | |
| 61 | | P63 | AN3 | | | | | |
| 62 | | P62 | AN2 | | | | | |
| 63 | | P61 | AN1 | | | | | |
| 64 | | P60 | AN0 | | | | | |
| 65 | | P47 | AN103/ CVREFH | | | | | |
| 66 | | P46 | AN102 | | | | | |
| 67 | | P45 | AN101 | | | | | |
| 68 | | P44 | AN100 | | | | | |
| 69 | | P43 | AN003/ CVREFL | | | | | |
| 70 | | P42 | AN002 | | | | | |
| 71 | | P41 | AN001 | | | | | |
| 72 | | P40 | AN000 | | | | | |
| 73 | AVCC0 | | | | | | | |
| 74 | VREFH0 | | | | | | | |
| 75 | VREFL0 | | | | | | | |

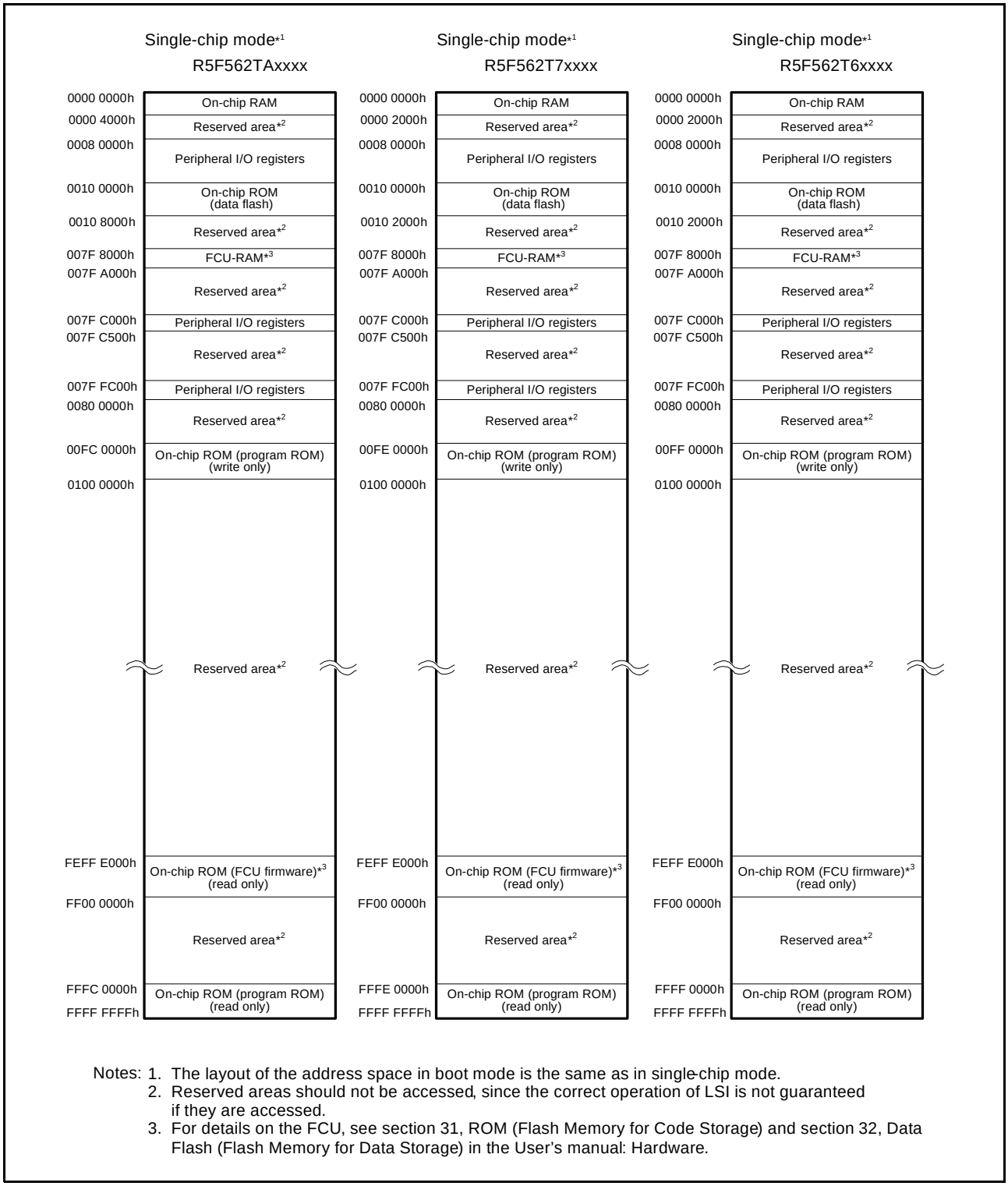
**Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)**

| Pin No. (64-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 1 | EMLE | | | | | | | |
| 2 | MDE | | | | | | | |
| 3 | VCL | | | | | | | |
| 4 | MD1 | | | | | | | |
| 5 | MD0 | | | | | | | |
| 6 | RES# | | | | | | | |
| 7 | XTAL | | | | | | | |
| 8 | VSS | | | | | | | |
| 9 | EXTAL | | | | | | | |
| 10 | VCC | | | | | | | |
| 11 | | PE2 | | | | NMI | POE10#-A | |
| 12 | | PD7 | | GTIOC0A-B | | | | TRST# |
| 13 | | PD6 | | GTIOC0B-B | | | | TMS |
| 14 | | PD5 | | GTIOC1A-B | RXD1 | | | TDI |
| 15 | | PD4 | | GTIOC1B-B | SCK1 | | | TCK |
| 16 | | PD3 | | GTIOC2A-B | TXD1 | | | TDO |
| 17 | | PB7 | | | SCK2-A | | | |
| 18 | | PB6 | | | CRX-A/ RXD2-A | | | |
| 19 | | PB5 | | | CTX-A/ TXD2-A | | | |
| 20 | PLLVCC | | | | | | | |
| 21 | | PB4 | | GTETRG | | IRQ3 | POE8# | |
| 22 | PLLVSS | | | | | | | |
| 23 | | PB3 | | MTIOC0A-A | SCK0 | | | |
| 24 | | PB2 | | MTIOC0B-A | TXD0/SDA | | | |
| 25 | | PB1 | | MTIOC0C | RXD0/SCL | | | |
| 26 | | PB0 | | MTIOC0D | MOSI-B | | | |
| 27 | | PA3 | | MTIOC2A | SSL0-B | | | |
| 28 | | PA2 | | MTIOC2B | SSL1-B | | | |
| 29 | | P94 | | MTIOC7A | | | | |
| 30 | | P93 | | MTIOC7B | | | | |
| 31 | | P92 | | MTIOC6D | | | | |
| 32 | | P91 | | MTIOC7C | | | | |
| 33 | | P76 | | MTIOC4D/ GTIOC2B-A | | | | |
| 34 | | P75 | | MTIOC4C/ GTIOC1B-A | | | | |
| 35 | | P74 | | MTIOC3D/ GTIOC0B-A | | | | |
| 36 | | P73 | | MTIOC4B/ GTIOC2A-A | | | | |
| 37 | | P72 | | MTIOC4A/ GTIOC1A-A | | | | |
| 38 | | P71 | | MTIOC3B/ GTIOC0A-A | | | | |
| 39 | | P70 | | | | IRQ5 | POE0# | |

# 3. Address Space

## 3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas. Figure 3.1 shows the memory maps.




Notes: 1. The layout of the address space in boot mode is the same as in single-chip mode.
2. Reserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
3. For details on the FCU, see section 31, ROM (Flash Memory for Code Storage) and section 32, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

**Figure 3.1 Memory Map (RX62T Group)**

**Table 4.1 List of I/O Registers (Address Order) (5 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 7172h | ICU | DTC activation enable register 114 | DTCER114 | 8 | 8 | 2 ICLK |
| 0008 7173h | ICU | DTC activation enable register 115 | DTCER115 | 8 | 8 | 2 ICLK |
| 0008 7174h | ICU | DTC activation enable register 116 | DTCER116 | 8 | 8 | 2 ICLK |
| 0008 7175h | ICU | DTC activation enable register 117 | DTCER117 | 8 | 8 | 2 ICLK |
| 0008 7179h | ICU | DTC activation enable register 121 | DTCER121 | 8 | 8 | 2 ICLK |
| 0008 717Ah | ICU | DTC activation enable register 122 | DTCER122 | 8 | 8 | 2 ICLK |
| 0008 717Dh | ICU | DTC activation enable register 125 | DTCER125 | 8 | 8 | 2 ICLK |
| 0008 717Eh | ICU | DTC activation enable register 126 | DTCER126 | 8 | 8 | 2 ICLK |
| 0008 7181h | ICU | DTC activation enable register 129 | DTCER129 | 8 | 8 | 2 ICLK |
| 0008 7182h | ICU | DTC activation enable register 130 | DTCER130 | 8 | 8 | 2 ICLK |
| 0008 7183h | ICU | DTC activation enable register 131 | DTCER131 | 8 | 8 | 2 ICLK |
| 0008 7184h | ICU | DTC activation enable register 132 | DTCER132 | 8 | 8 | 2 ICLK |
| 0008 7186h | ICU | DTC activation enable register 134 | DTCER134 | 8 | 8 | 2 ICLK |
| 0008 7187h | ICU | DTC activation enable register 135 | DTCER135 | 8 | 8 | 2 ICLK |
| 0008 7188h | ICU | DTC activation enable register 136 | DTCER136 | 8 | 8 | 2 ICLK |
| 0008 7189h | ICU | DTC activation enable register 137 | DTCER137 | 8 | 8 | 2 ICLK |
| 0008 718Ah | ICU | DTC activation enable register 138 | DTCER138 | 8 | 8 | 2 ICLK |
| 0008 718Bh | ICU | DTC activation enable register 139 | DTCER139 | 8 | 8 | 2 ICLK |
| 0008 718Ch | ICU | DTC activation enable register 140 | DTCER140 | 8 | 8 | 2 ICLK |
| 0008 718Dh | ICU | DTC activation enable register 141 | DTCER141 | 8 | 8 | 2 ICLK |
| 0008 718Eh | ICU | DTC activation enable register 142 | DTCER142 | 8 | 8 | 2 ICLK |
| 0008 718Fh | ICU | DTC activation enable register 143 | DTCER143 | 8 | 8 | 2 ICLK |
| 0008 7190h | ICU | DTC activation enable register 144 | DTCER144 | 8 | 8 | 2 ICLK |
| 0008 7191h | ICU | DTC activation enable register 145 | DTCER145 | 8 | 8 | 2 ICLK |
| 0008 7195h | ICU | DTC activation enable register 149 | DTCER149 | 8 | 8 | 2 ICLK |
| 0008 7196h | ICU | DTC activation enable register 150 | DTCER150 | 8 | 8 | 2 ICLK |
| 0008 7197h | ICU | DTC activation enable register 151 | DTCER151 | 8 | 8 | 2 ICLK |
| 0008 7198h | ICU | DTC activation enable register 152 | DTCER152 | 8 | 8 | 2 ICLK |
| 0008 7199h | ICU | DTC activation enable register 153 | DTCER153 | 8 | 8 | 2 ICLK |
| 0008 71AEh | ICU | DTC activation enable register 174 | DTCER174 | 8 | 8 | 2 ICLK |
| 0008 71AFh | ICU | DTC activation enable register 175 | DTCER175 | 8 | 8 | 2 ICLK |
| 0008 71B0h | ICU | DTC activation enable register 176 | DTCER176 | 8 | 8 | 2 ICLK |
| 0008 71B1h | ICU | DTC activation enable register 177 | DTCER177 | 8 | 8 | 2 ICLK |
| 0008 71B2h | ICU | DTC activation enable register 178 | DTCER178 | 8 | 8 | 2 ICLK |
| 0008 71B3h | ICU | DTC activation enable register 179 | DTCER179 | 8 | 8 | 2 ICLK |
| 0008 71B4h | ICU | DTC activation enable register 180 | DTCER180 | 8 | 8 | 2 ICLK |
| 0008 71B5h | ICU | DTC activation enable register 181 | DTCER181 | 8 | 8 | 2 ICLK |
| 0008 71B6h | ICU | DTC activation enable register 182 | DTCER182 | 8 | 8 | 2 ICLK |
| 0008 71B7h | ICU | DTC activation enable register 183 | DTCER183 | 8 | 8 | 2 ICLK |
| 0008 71B8h | ICU | DTC activation enable register 184 | DTCER184 | 8 | 8 | 2 ICLK |
| 0008 71BAh | ICU | DTC activation enable register 186 | DTCER186 | 8 | 8 | 2 ICLK |
| 0008 71BBh | ICU | DTC activation enable register 187 | DTCER187 | 8 | 8 | 2 ICLK |
| 0008 71BCh | ICU | DTC activation enable register 188 | DTCER188 | 8 | 8 | 2 ICLK |
| 0008 71BDh | ICU | DTC activation enable register 189 | DTCER189 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (17 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 123Ah | MTU | Timer interrupt skipping mode register A | TITMRA | 8 | 8 | 5 ICLK |
| 000C 123Bh | MTU | Timer interrupt skipping set register 2A | TITCR2A | 8 | 8 | 5 ICLK |
| 000C 123Ch | MTU | Timer interrupt skipping counter 2A | TITCNT2A | 8 | 8 | 5 ICLK |
| 000C 1240h | MTU4 | Timer A/D converter start request control register | TADCR | 16 | 16 | 5 ICLK |
| 000C 1244h | MTU4 | Timer A/D converter start request cycle set register A | TADCORA | 16 | 16, 32 | 5 ICLK |
| 000C 1246h | MTU4 | Timer A/D converter start request cycle set register B | TADCORB | 16 | 16 | 5 ICLK |
| 000C 1248h | MTU4 | Timer A/D converter start request cycle set buffer register A | TADCOBRA | 16 | 16, 32 | 5 ICLK |
| 000C 124Ah | MTU4 | Timer A/D converter start request cycle set buffer register B | TADCOBRB | 16 | 16 | 5 ICLK |
| 000C 1260h | MTU | Timer waveform control register A | TWCRA | 8 | 8 | 5 ICLK |
| 000C 1270h | MTU3 | Timer mode register 2A | TMDR2A | 8 | 8 | 5 ICLK |
| 000C 1272h | MTU3 | Timer general register E | TGRE | 16 | 16 | 5 ICLK |
| 000C 1274h | MTU4 | Timer general register E | TGRE | 16 | 16 | 5 ICLK |
| 000C 1276h | MTU4 | Timer general register F | TGRF | 16 | 16 | 5 ICLK |
| 000C 1280h | MTU | Timer start register A | TSTRA | 8 | 8, 16 | 5 ICLK |
| 000C 1281h | MTU | Timer synchronous register A | TSYRA | 8 | 8 | 5 ICLK |
| 000C 1282h | MTU | Timer counter synchronous start register | TCSYSTR | 8 | 8 | 5 ICLK |
| 000C 1284h | MTU | Timer read/write enable register A | TRWERA | 8 | 8 | 5 ICLK |
| 000C 1300h | MTU0 | Timer control register | TCR | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1301h | MTU0 | Timer mode register 1 | TMDR1 | 8 | 8 | 5 ICLK |
| 000C 1302h | MTU0 | Timer I/O control register H | TIORH | 8 | 8, 16 | 5 ICLK |
| 000C 1303h | MTU0 | Timer I/O control register L | TIORL | 8 | 8 | 5 ICLK |
| 000C 1304h | MTU0 | Timer interrupt enable register | TIER | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1305h | MTU0 | Timer status register | TSR | 8 | 8 | 5 ICLK |
| 000C 1306h | MTU0 | Timer counter | TCNT | 16 | 16 | 5 ICLK |
| 000C 1308h | MTU0 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 130Ah | MTU0 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |
| 000C 130Ch | MTU0 | Timer general register C | TGRC | 16 | 16, 32 | 5 ICLK |
| 000C 130Eh | MTU0 | Timer general register D | TGRD | 16 | 16 | 5 ICLK |
| 000C 1320h | MTU0 | Timer general register E | TGRE | 16 | 16, 32 | 5 ICLK |
| 000C 1322h | MTU0 | Timer general register F | TGRF | 16 | 16 | 5 ICLK |
| 000C 1324h | MTU0 | Timer interrupt enable register 2 | TIER2 | 8 | 8, 16 | 5 ICLK |
| 000C 1325h | MTU0 | Timer status register 2 | TSR2 | 8 | 8 | 5 ICLK |
| 000C 1326h | MTU0 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 5 ICLK |
| 000C 1380h | MTU1 | Timer control register | TCR | 8 | 8, 16 | 5 ICLK |
| 000C 1381h | MTU1 | Timer mode register 1 | TMDR1 | 8 | 8 | 5 ICLK |
| 000C 1382h | MTU1 | Timer I/O control register | TIOR | 8 | 8 | 5 ICLK |
| 000C 1384h | MTU1 | Timer interrupt enable register | TIER | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1385h | MTU1 | Timer status register | TSR | 8 | 8 | 5 ICLK |
| 000C 1386h | MTU1 | Timer counter | TCNT | 16 | 16 | 5 ICLK |
| 000C 1388h | MTU1 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 138Ah | MTU1 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |

**Table 4.2 List of I/O Registers (Bit Order) (4 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| ICU | IR044 | — | — | — | — | — | — | — | IR |
| ICU | IR045 | — | — | — | — | — | — | — | IR |
| ICU | IR046 | — | — | — | — | — | — | — | IR |
| ICU | IR047 | — | — | — | — | — | — | — | IR |
| ICU | IR056 | — | — | — | — | — | — | — | IR |
| ICU | IR057 | — | — | — | — | — | — | — | IR |
| ICU | IR058 | — | — | — | — | — | — | — | IR |
| ICU | IR059 | — | — | — | — | — | — | — | IR |
| ICU | IR060 | — | — | — | — | — | — | — | IR |
| ICU | IR064 | — | — | — | — | — | — | — | IR |
| ICU | IR065 | — | — | — | — | — | — | — | IR |
| ICU | IR066 | — | — | — | — | — | — | — | IR |
| ICU | IR067 | — | — | — | — | — | — | — | IR |
| ICU | IR068 | — | — | — | — | — | — | — | IR |
| ICU | IR069 | — | — | — | — | — | — | — | IR |
| ICU | IR070 | — | — | — | — | — | — | — | IR |
| ICU | IR071 | — | — | — | — | — | — | — | IR |
| ICU | IR096 | — | — | — | — | — | — | — | IR |
| ICU | IR098 | — | — | — | — | — | — | — | IR |
| ICU | IR102 | — | — | — | — | — | — | — | IR |
| ICU | IR103 | — | — | — | — | — | — | — | IR |
| ICU | IR106 | — | — | — | — | — | — | — | IR |
| ICU | IR114 | — | — | — | — | — | — | — | IR |
| ICU | IR115 | — | — | — | — | — | — | — | IR |
| ICU | IR116 | — | — | — | — | — | — | — | IR |
| ICU | IR117 | — | — | — | — | — | — | — | IR |
| ICU | IR118 | — | — | — | — | — | — | — | IR |
| ICU | IR119 | — | — | — | — | — | — | — | IR |
| ICU | IR120 | — | — | — | — | — | — | — | IR |
| ICU | IR121 | — | — | — | — | — | — | — | IR |
| ICU | IR122 | — | — | — | — | — | — | — | IR |
| ICU | IR123 | — | — | — | — | — | — | — | IR |
| ICU | IR124 | — | — | — | — | — | — | — | IR |
| ICU | IR125 | — | — | — | — | — | — | — | IR |
| ICU | IR126 | — | — | — | — | — | — | — | IR |
| ICU | IR127 | — | — | — | — | — | — | — | IR |
| ICU | IR128 | — | — | — | — | — | — | — | IR |
| ICU | IR129 | — | — | — | — | — | — | — | IR |
| ICU | IR130 | — | — | — | — | — | — | — | IR |
| ICU | IR131 | — | — | — | — | — | — | — | IR |
| ICU | IR132 | — | — | — | — | — | — | — | IR |
| ICU | IR133 | — | — | — | — | — | — | — | IR |
| ICU | IR134 | — | — | — | — | — | — | — | IR |
| ICU | IR135 | — | — | — | — | — | — | — | IR |
| ICU | IR136 | — | — | — | — | — | — | — | IR |
| ICU | IR137 | — | — | — | — | — | — | — | IR |
| ICU | IR138 | — | — | — | — | — | — | — | IR |
| ICU | IR139 | — | — | — | — | — | — | — | IR |
| ICU | IR140 | — | — | — | — | — | — | — | IR |
| ICU | IR141 | — | — | — | — | — | — | — | IR |
| ICU | IR142 | — | — | — | — | — | — | — | IR |
| ICU | IR143 | — | — | — | — | — | — | — | IR |

**Table 4.2 List of I/O Registers (Bit Order) (5 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| ICU | IR144 | — | — | — | — | — | — | — | IR |
| ICU | IR145 | — | — | — | — | — | — | — | IR |
| ICU | IR146 | — | — | — | — | — | — | — | IR |
| ICU | IR149 | — | — | — | — | — | — | — | IR |
| ICU | IR150 | — | — | — | — | — | — | — | IR |
| ICU | IR151 | — | — | — | — | — | — | — | IR |
| ICU | IR152 | — | — | — | — | — | — | — | IR |
| ICU | IR153 | — | — | — | — | — | — | — | IR |
| ICU | IR170 | — | — | — | — | — | — | — | IR |
| ICU | IR171 | — | — | — | — | — | — | — | IR |
| ICU | IR172 | — | — | — | — | — | — | — | IR |
| ICU | IR173 | — | — | — | — | — | — | — | IR |
| ICU | IR174 | — | — | — | — | — | — | — | IR |
| ICU | IR175 | — | — | — | — | — | — | — | IR |
| ICU | IR176 | — | — | — | — | — | — | — | IR |
| ICU | IR177 | — | — | — | — | — | — | — | IR |
| ICU | IR178 | — | — | — | — | — | — | — | IR |
| ICU | IR179 | — | — | — | — | — | — | — | IR |
| ICU | IR180 | — | — | — | — | — | — | — | IR |
| ICU | IR181 | — | — | — | — | — | — | — | IR |
| ICU | IR182 | — | — | — | — | — | — | — | IR |
| ICU | IR183 | — | — | — | — | — | — | — | IR |
| ICU | IR184 | — | — | — | — | — | — | — | IR |
| ICU | IR186 | — | — | — | — | — | — | — | IR |
| ICU | IR187 | — | — | — | — | — | — | — | IR |
| ICU | IR188 | — | — | — | — | — | — | — | IR |
| ICU | IR189 | — | — | — | — | — | — | — | IR |
| ICU | IR190 | — | — | — | — | — | — | — | IR |
| ICU | IR192 | — | — | — | — | — | — | — | IR |
| ICU | IR193 | — | — | — | — | — | — | — | IR |
| ICU | IR194 | — | — | — | — | — | — | — | IR |
| ICU | IR195 | — | — | — | — | — | — | — | IR |
| ICU | IR196 | — | — | — | — | — | — | — | IR |
| ICU | IR214 | — | — | — | — | — | — | — | IR |
| ICU | IR215 | — | — | — | — | — | — | — | IR |
| ICU | IR216 | — | — | — | — | — | — | — | IR |
| ICU | IR217 | — | — | — | — | — | — | — | IR |
| ICU | IR218 | — | — | — | — | — | — | — | IR |
| ICU | IR219 | — | — | — | — | — | — | — | IR |
| ICU | IR220 | — | — | — | — | — | — | — | IR |
| ICU | IR221 | — | — | — | — | — | — | — | IR |
| ICU | IR222 | — | — | — | — | — | — | — | IR |
| ICU | IR223 | — | — | — | — | — | — | — | IR |
| ICU | IR224 | — | — | — | — | — | — | — | IR |
| ICU | IR225 | — | — | — | — | — | — | — | IR |
| ICU | IR246 | — | — | — | — | — | — | — | IR |
| ICU | IR247 | — | — | — | — | — | — | — | IR |
| ICU | IR248 | — | — | — | — | — | — | — | IR |
| ICU | IR249 | — | — | — | — | — | — | — | IR |
| ICU | IR254 | — | — | — | — | — | — | — | IR |
| ICU | DTCER027 | — | — | — | — | — | — | — | DTCE |
| ICU | DTCER028 | — | — | — | — | — | — | — | DTCE |

**Table 4.2 List of I/O Registers (Bit Order) (10 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| AD0 | ADDRB*1 | — | — | — | — | — | — | | |
| AD0 | ADDRC*1 | — | — | — | — | — | — | | |
| AD0 | ADDRD*1 | — | — | — | — | — | — | | |
| AD0 | ADDRE*1 | — | — | — | — | — | — | | |
| AD0 | ADDRF*1 | — | — | — | — | — | — | | |
| AD0 | ADDRG*1 | — | — | — | — | — | — | | |
| AD0 | ADDRH*1 | — | — | — | — | — | — | | |
| AD0 | ADCSR | — | ADIE | ADST | — | | CH[3:0] | | |
| AD0 | ADCR | — | — | — | — | CKS[1:0] | | MODE[1:0] | |
| AD0 | ADSSTR | | | | | | | | |
| AD0 | ADDIAGR | — | — | — | — | — | — | DIAG[1:0] | |
| AD0 | ADDRI*1 | — | — | — | — | — | — | | |
| AD0 | ADDRJ*1 | — | — | — | — | — | — | | |
| AD0 | ADDRK *1 | — | — | — | — | — | — | | |
| AD0 | ADDRL*1 | — | — | — | — | — | — | | |
| AD0 | ADSTRGR | — | — | — | | | ADSTRS[4:0] | | |
| AD0 | ADDPR | DPSEL | — | — | — | — | — | — | DPPRC |
| SCI0 | SMR | CM | CHR | PE | PM | STOP | MP | CKS[1:0] | |
| SCI0 | BRR | | | | | | | | |
| SCI0 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SCI0 | TDR | | | | | | | | |
| SCI0 | SSR | TDRE | RDRF | ORER | FER | PER | TEND | MPB | MPBT |
| SCI0 | RDR | | | | | | | | |
| SCI0 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| SCI0 | SEMR | — | — | NFEN | ABCS | — | — | — | — |
| SMCI0 | SMR | GM | BLK | PE | PM | (BCP[1:0]) | | CKS[1:0] | |
| SMCI0 | BRR | | | | | | | | |
| SMCI0 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SMCI0 | TDR | | | | | | | | |
| SMCI0 | SSR | TDRE | RDRF | ORER | ERS | PER | TEND | MPB | MPBT |
| SMCI0 | RDR | | | | | | | | |
| SMCI0 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| SCI1 | SMR | CM | CHR | PE | PM | STOP | MP | CKS[1:0] | |
| SCI1 | BRR | | | | | | | | |
| SCI1 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SCI1 | TDR | | | | | | | | |
| SCI1 | SSR | TDRE | RDRF | ORER | FER | PER | TEND | MPB | MPBT |
| SCI1 | RDR | | | | | | | | |
| SCI1 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |

**Table 4.2 List of I/O Registers (Bit Order) (12 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| RSPI0 | SSLP | — | — | — | — | SSLP3 | SSLP2 | SSLP1 | SSLP0 |
| RSPI0 | SPPCR | — | — | MOIFE | MOIFV | — | — | SPLP2 | SPLP |
| RSPI0 | SPSR | SPRF | — | SPTEF | — | PERF | MODF | IDLNF | OVRF |
| RSPI0 | SPDR | H[15:0] | | | | | | | |
| | | H[15:0] | | | | | | | |
| | | L[15:0] | | | | | | | |
| | | L[15:0] | | | | | | | |
| RSPI0 | SPSCR | — | — | — | — | — | | SPSLN[2:0] | |
| RSPI0 | SPSSR | — | | SPECM[2:0] | | — | | SPCP[2:0] | |
| RSPI0 | SPBR | SPR7 | SPR6 | SPR5 | SPR4 | SPR3 | SPR2 | SPR1 | SPR0 |
| RSPI0 | SPDCR | — | — | SPLW | SPRDTD | SLSEL[1:0] | | SPFC[1:0] | |
| RSPI0 | SPCKD | — | — | — | — | — | | SCKDL[2:0] | |
| RSPI0 | SSLND | — | — | — | — | — | | SLNDL[2:0] | |
| RSPI0 | SPND | — | — | — | — | — | | SPNDL[2:0] | |
| RSPI0 | SPCR2 | — | — | — | — | PTE | SPIIE | SPOE | SPPE |
| RSPI0 | SPCMD0 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD1 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD2 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD3 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD4 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD5 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD6 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| RSPI0 | SPCMD7 | SCKDEN | SLNDEN | SPNDEN | LSBF | | SPB[3:0] | | |
| | | SSLKP | | SSLA[2:0] | | BRDV[1:0] | | CPOL | CPHA |
| S12AD0 | ADCSR | ADST | ADCS[1:0] | | ADIE | CKS[1:0] | | TRGE | EXTRG |
| S12AD0 | ADANS | — | — | CH[1:0] | | — | PG002SEL | PG001SEL | PG000SEL |
| | | — | — | — | — | — | PG002EN | PG001EN | PG000EN |
| S12AD0 | ADPG | — | — | — | — | PG002GAIN[3:0] | | | |
| | | PG001GAIN[3:0] | | | | PG000GAIN[3:0] | | | |
| S12AD0 | ADCER | ADRFMT | — | ADIEW | ADIE2 | DIAGM | DIAGLD | DIAGVAL[1:0] | |
| | | — | — | ACE | — | — | ADPRC[1:0] | | SHBYP |
| S12AD0 | ADSTRGR | — | — | — | ADSTRS1[4:0] | | | | |
| | | — | — | — | ADSTRS0[4:0] | | | | |
| S12AD | ADCMPMD0 | — | — | CEN102[1:0] | | CEN101[1:0] | | CEN100[1:0] | |
| | | — | — | CEN002[1:0] | | CEN001[1:0] | | CEN000[1:0] | |
| S12AD | ADCMPMD1 | — | VSELL1 | VSELH1 | CSEL1 | — | VSELL0 | VSELH0 | CSEL0 |
| | | — | | REFH[2:0] | | — | | REFL[2:0] | |
| S12AD | ADCMPNR0 | — | — | — | — | C002NR[3:0] | | | |
| | | C001NR[3:0] | | | | C000NR[3:0] | | | |
| S12AD | ADCMPNR1 | — | — | — | — | C102NR[3:0] | | | |
| | | C101NR[3:0] | | | | C100NR[3:0] | | | |
| S12AD | ADCMPFR | — | — | C102FLAG | C101FLAG | C100FLAG | C002FLAG | C001FLAG | C000FLAG |
| S12AD | ADCMPSEL | — | — | — | — | — | — | POERQ | IE |
| | | — | — | SEL102 | SEL101 | SEL100 | SEL002 | SEL001 | SEL000 |

**Table 5.3 DC Characteristics (2)**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Supply current*1 | In operation | Max.*2 | $I_{CC}$*3 | - | - | 70 | mA | ICLK = 100 MHz PCLK = 50 MHz |
| | | Normal*4 | | - | 35 | - | | |
| | | Increased by BGO operation*5 | | - | 15 | - | | |
| | Sleep | | | | 22 | 60 | | |
| | All-module-clock-stop mode*6 | | | | 14 | 28 | | |
| | Standby mode | Software standby mode | | - | 0.10 | 3 | mA | |
| | | Deep software standby mode | | - | 20 | 60 | µA | |
| Analog power supply current | During 12-bit A/D conversion (when a sample-and-hold circuit is in use; per unit) | | $AI_{CC0}$ | - | 3 | 5 | mA | |
| | During 12-bit A/D conversion (when a sample-and-hold circuit is not in use; per unit) | | | - | 3 | 5 | mA | |
| | Programmable gain amp (per channel) | | | - | 1 | 2 | mA | |
| | Window comparator (1 channel) | | | | 0.5 | 1 | mA | |
| | Window comparator (6 channels) | | | - | 1 | 2 | mA | |
| | During 12-bit A/D conversion (per unit) | | | - | 60 | 90 | µA | |
| | During 10-bit A/D conversion (per unit) | | $AI_{CC}$ | - | 0.9 | 2 | mA | |
| | Waiting for 10-bit A/D conversion (all units) | | | - | 0.3 | 3 | µA | |
| Reference power supply current | During 12-bit A/D conversion (per unit) | | $AI_{REFH0}$ | - | 1.6 | 3 | mA | |
| | Waiting for 12-bit A/D conversion (all units) | | | - | 1.6 | 3 | mA | |
| | During 10-bit A/D conversion (per unit) | | $AI_{REF}$ | - | 0.1 | 1 | mA | |
| | Waiting for 10-bit A/D conversion (all units) | | | - | 0.1 | 3 | µA | |
| VCC rising gradient | | | $SV_{CC}$ | - | - | 20 | ms/V | |

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. $I_{CC}$ depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max. = 0.54 x f + 16 (max.)
ICC max. = 0.3 x f + 5 (normal operation)
ICC max. = 0.44 x f + 16 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
Note 6. The values are for reference.

## 5.3 AC Characteristics

**Table 5.6 Operation Frequency Value**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | System clock (ICLK) | f | 8 | - | 100 | MHz |
| | Peripheral module clock (PCLK) | | 8 | - | 50 | |

### 5.3.1 Clock Timing

**Table 5.7 Clock Timing**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Oscillation settling time after reset (crystal) | $t_{OSC1}$ | 10 | - | ms | Figure 5.1 |
| Oscillation settling time after leaving software standby mode (crystal) | $t_{OSC2}$ | 10 | - | ms | Figure 5.2 |
| Oscillation settling time after leaving deep software standby mode (crystal) | $t_{OSC3}$ | 10 | - | ms | Figure 5.3 |
| EXTAL external clock output delay settling time | $t_{DEXT}$ | 1 | - | ms | Figure 5.1 |
| EXTAL external clock input low pulse width | $t_{EXL}$ | 35 | - | ns | Figure 5.4 |
| EXTAL external clock input high pulse width | $t_{EXH}$ | 35 | - | ns | |
| EXTAL external clock rising time | $t_{EXr}$ | - | 5 | ns | |
| EXTAL external clock falling time | $t_{EXf}$ | - | 5 | ns | |
| On-chip oscillator (IWDTCLK) oscillation frequency | $f_{IWDTCLK}$ | 62.5 | 187.5 | kHz | |

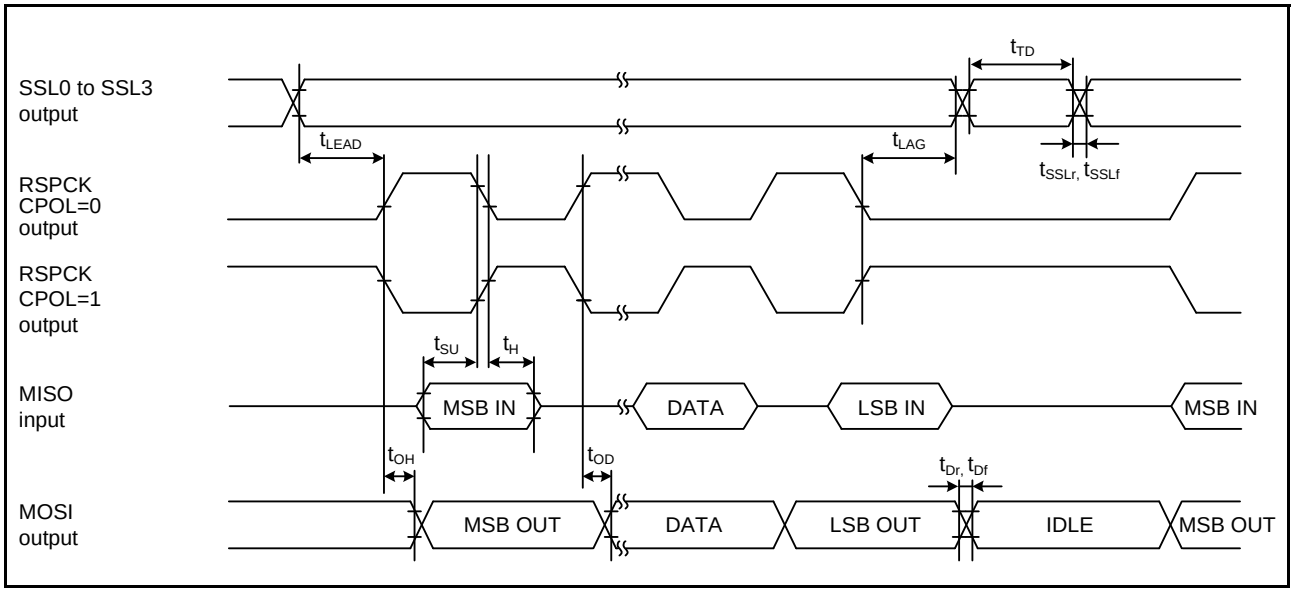



**Figure 5.13 RSPI Timing (Master, CPHA = 1)**

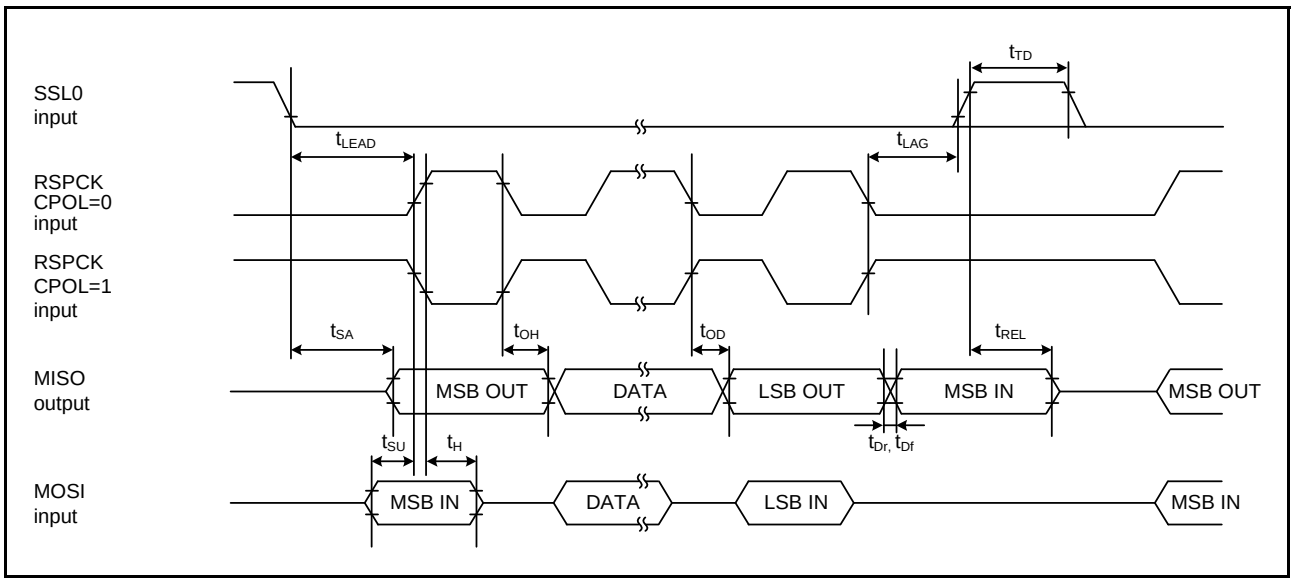



**Figure 5.14 RSPI Timing (Slave, CPHA = 0)**

## 5.6 Oscillation Stop Detection Timing

**Table 5.20 Oscillation Stop Detection Circuit Characteristics**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Detection time | tdr | - | - | 1.0 | ms | Figure 5.23 |
| Internal oscillation frequency when oscillation stop is detected | $f_{MAIN}$ | 0.5 | - | 7.0 | MHz | |

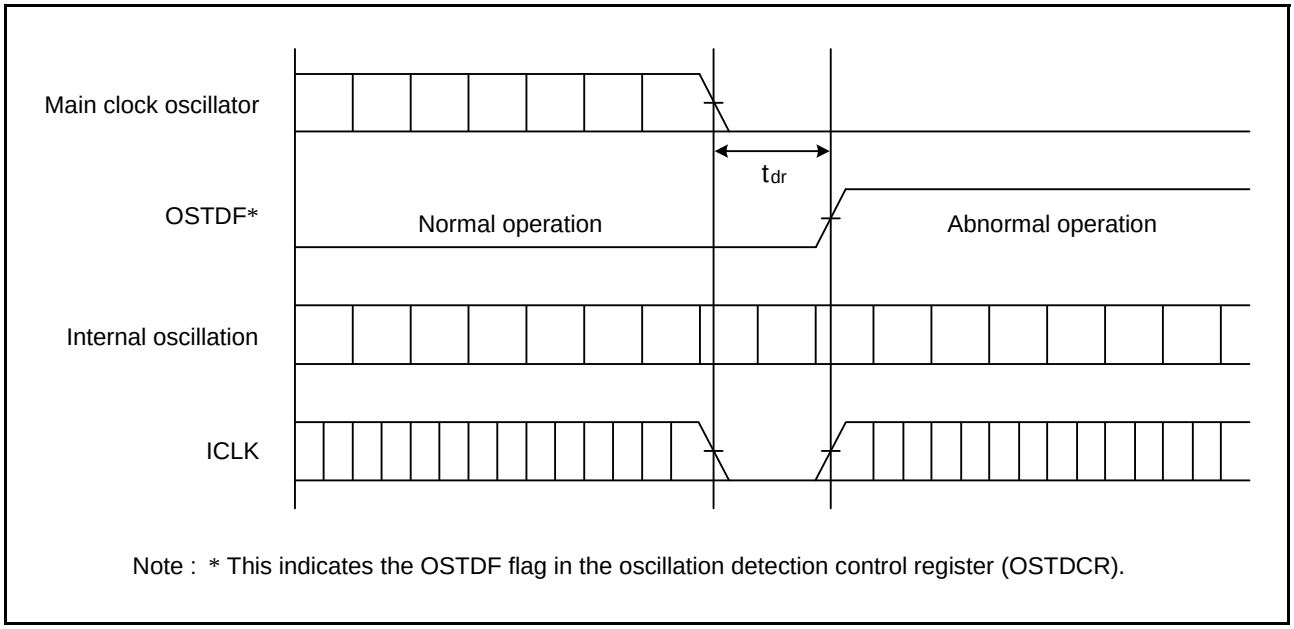
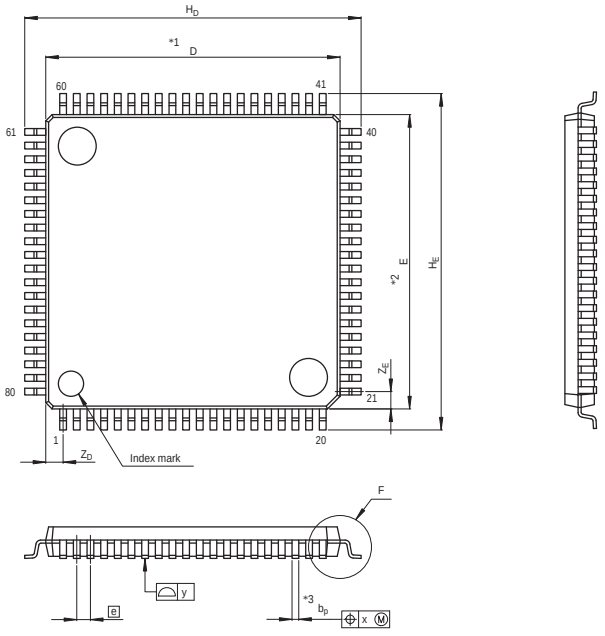
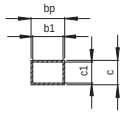



**Figure 5.23 Oscillation Stop Detection Timing**

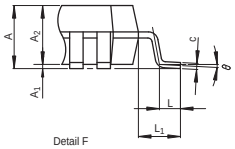
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP80-14x14-0.65 | PLQP0080JA-A | FP-80W / FP-80WV | 0.6g |






Terminal cross section



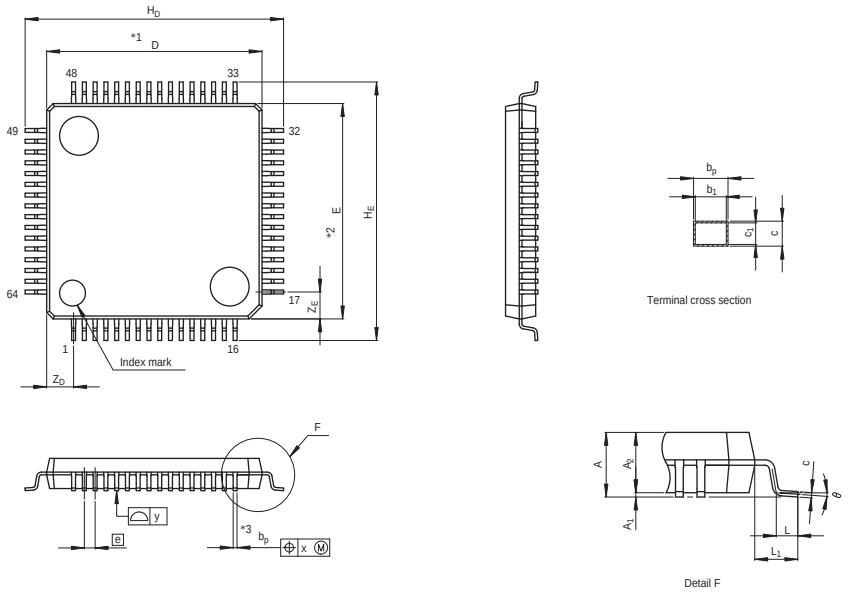

Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.27 | 0.32 | 0.37 |
| $b_1$ | — | 0.30 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 8° |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.825 | — |
| $Z_E$ | — | 0.825 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure C 80-Pin LQFP (PLQP0080JA-A) Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP64-10x10-0.50 | PLQP0064KB-A | 64P6Q-A / FP-64K / FP-64KV | 0.3g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure D 64-Pin LQFP (PLQP0064KB-A) Package Dimensions

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.