Renesas Electronics America Inc - R5F562TADDFH#V3 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	61
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562taddfh-v3

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.

Table 1.1 Outline of Specifications (1 / 5)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU • General purpose: Sixteen 32-bit registers • Control: Nine 32-bit registers • Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement • Instructions: Little endian • Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• ROM capacity: 256 Kbytes (max.) • Two on-board programming modes • Boot mode (The user MAT is programmable via the SCI) • User program mode • Off-board programming • A PROM programmer can be used to program the user mat.
	RAM	• RAM capacity: 16 Kbytes (max.)
	Data flash	• Data flash capacity: 32 Kbytes (max.) • Supports background operations (BGO)
MCU operating mode		• Single-chip mode
Clock	Clock generation circuit	• One circuit: Main clock oscillator • Internal oscillator: Low-speed on-chip oscillator dedicated to IWDT • Structure of a PLL frequency synthesizer and frequency divider for selectable operating frequency • Oscillation stoppage detection • Independent frequency-division and multiplication settings for the system clock (ICLK) and peripheral module clock (PCLK) • The CPU and system sections such as other bus masters, MTU3, and GPT run in synchronization with the system clock (ICLK): 8 to 100 MHz. • Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz
Reset		Pin reset, power-on reset (automatic power-on reset when the power is turned on), voltage-monitoring reset, watchdog timer reset, independent watchdog timer reset, and deep software standby reset
Voltage detection circuit (LVD)		When the voltage on VCC falls below the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes • Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode

Table 1.1 Outline of Specifications (5 / 5)

Classification	Module/Function	Description
A/D converter	10-bit A/D converter (ADA)	• 10 bits (1 unit x 12 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V • Two basic operating modes Single mode and scan mode • Scan mode One-cycle scan mode Continuous scan mode • Sample-and-hold function A common sample-and-hold circuit for both units is included. • A/D-conversion register settings for each input pin • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8-bit precision output Right-shifting the results of conversion for output by two bits is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF).
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Operating frequency		ICLK: 8 to 100 MHz PCLK: 8 to 50 MHz
Power supply voltage		• 3-V version VCC = PLLVCC = 2.7 to 3.6V AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 VREF = 3.0 to AVCC, or 4.0 to AVCC • 5-V version VCC = PLLVCC = 4.0 to 5.5V AVCC0 = AVCC = 4.0 to 5.5V VREFH0 = 4.0 to AVCC0 VREF = 4.0 to AVCC
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Packages		112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch) 100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch) 80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch) 64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch) 64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

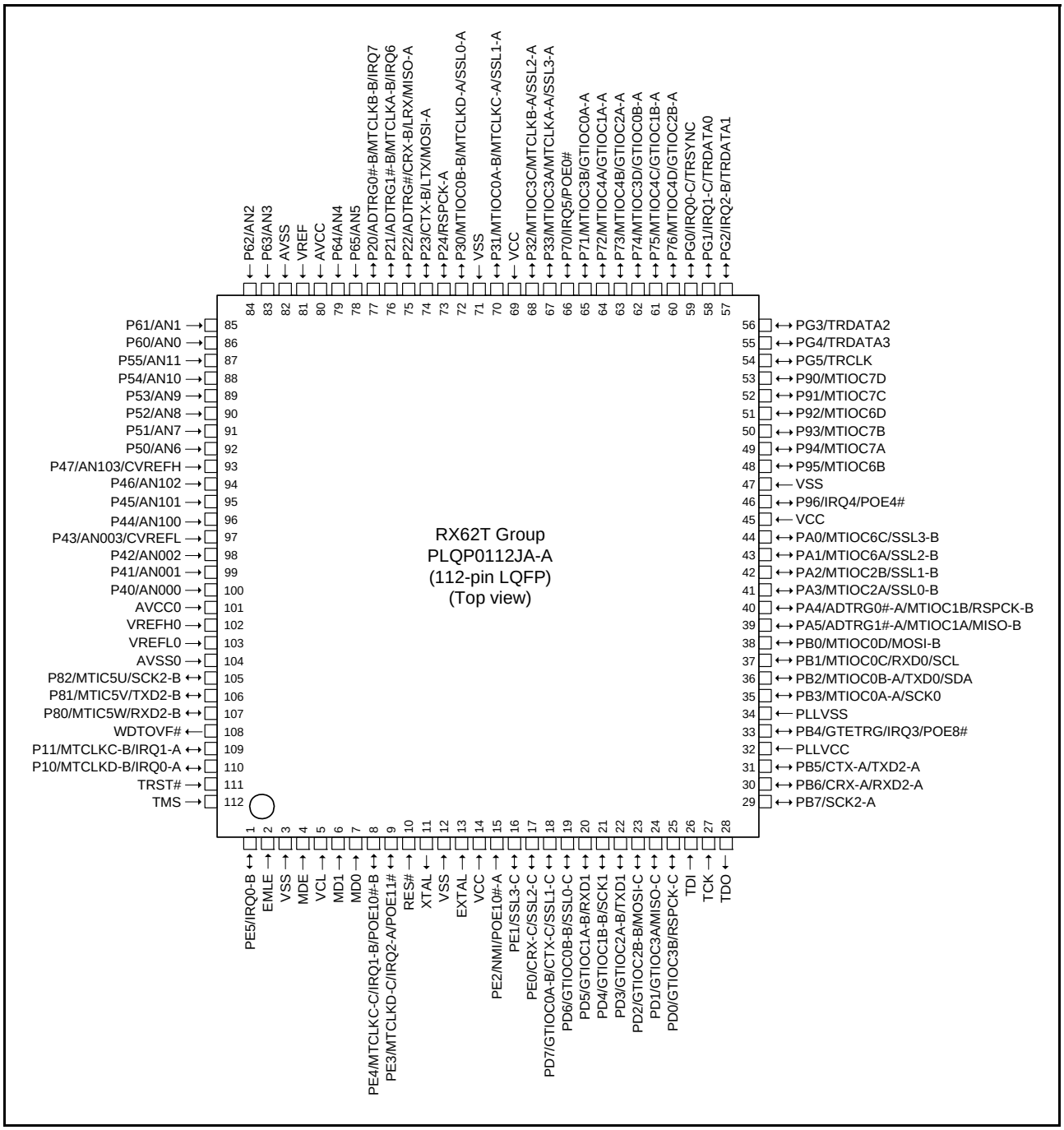


Figure 1.3 Pin Assignment of the 112-Pin LQFP

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (1 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/ SSL1-C			
19		PD6		GTIOC0B-B	SSL0-C			
20		PD5		GTIOC1A-B	RXD1			
21		PD4		GTIOC1B-B	SCK1			
22		PD3		GTIOC2A-B	TXD1			
23		PD2		GTIOC2B-B	MOSI-C			
24		PD1		GTIOC3A	MISO-C			
25		PD0		GTIOC3B	RSPCK-C			
26								TDI
27								TCK
28								TDO
29		PB7			SCK2-A			
30		PB6			CRX-A/ RXD2-A			
31		PB5			CTX-A/ TXD2-A			
32	PLLVCC							
33		PB4		GTETRG		IRQ3	POE8#	
34	PLLVSS							
35		PB3		MTIOC0A-A	SCK0			
36		PB2		MTIOC0B-A	TXD0/SDA			
37		PB1		MTIOC0C	RXD0/SCL			
38		PB0		MTIOC0D	MOSI-B			
39		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
40		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
41		PA3		MTIOC2A	SSL0-B			
42		PA2		MTIOC2B	SSL1-B			
43		PA1		MTIOC6A	SSL2-B			

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
42		P76		MTIOC4D/ GTIOC2B-A				
43		P75		MTIOC4C/ GTIOC1B-A				
44		P74		MTIOC3D/ GTIOC0B-A				
45		P73		MTIOC4B/ GTIOC2A-A				
46		P72		MTIOC4A/ GTIOC1A-A				
47		P71		MTIOC3B/ GTIOC0A-A				
48		P70				IRQ5	POE0#	
49		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
50		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
51	VCC							
52		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
53	VSS							
54		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
55		P24			RSPCK-A			
56		P23			CTX-B/ LTX/ MOSI-A			
57		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
58		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
59	AVCC							
60	AVSS							
61		P63	AN3					
62		P62	AN2					
63		P61	AN1					
64		P60	AN0					
65		P47	AN103/ CVREFH					
66		P46	AN102					
67		P45	AN101					
68		P44	AN100					
69		P43	AN003/ CVREFL					
70		P42	AN002					
71		P41	AN001					
72		P40	AN000					
73	AVCC0							
74	VREFH0							
75	VREFL0							

Table 1.9 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
I/O ports	P10, P11	I/O	2-bit input/output pins.
	P20 to P24	I/O	5-bit input/output pins. The P20/P21 pin is not included in the 64-pin version.
	P30 to P33	I/O	4-bit input/output pins.
	P40 to P47	Input	8-bit input pins.
	P50 to P55	Input	6-bit input pins. Not included in the 80-/64-pin versions.
	P60 to P65	Input	6-bit input pins. The P64/P6 pin is not included in the 80-pin version. Not included in the 64-pin version.
	P70 to P76	I/O	7-bit input/output pins.
	P80 to P82	I/O	3-bit input/output pins. Not included in the 80-/64-pin versions.
	P90 to P96	I/O	7-bit input/output pins. The P90 pin is not included in the 80-pin version. The P90/P95/P96 pin is not included in the 64-pin version.
	PA0 to PA5	I/O	6-bit input/output pins. The PA0/PA1 pin is not included in the 80-/64-pin versions.
	PB0 to PB7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins. The PD0/PD1/PD2 pin is not included in the 80-/64-pin versions.
	PE0, PE1, PE3 to PE5	I/O	5-bit input/output pins. The PE1/PE5 pin is not included in the 80-pin version. Not included in the 64-pin version.
	PE2	Input	1-bit input pin.
	PG0 to PG5	I/O	6-bit input/output pins. Not included in the 100-/80-/64-pin versions.

Note: • Which pins are and are not incorporated depends on the package.
For details, see the list of pins and pin functions in Table 1.4 to Table 1.8.

(9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (4 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2 ICLK
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FEh	ICU	Interrupt request register 254	IR254	8	8	2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C29Ch	SYSTEM	Deep standby backup register 12	DPSBKR12	8	8	4, 5 PCLK*3
0008 C29Dh	SYSTEM	Deep standby backup register 13	DPSBKR13	8	8	4, 5 PCLK*3
0008 C29Eh	SYSTEM	Deep standby backup register 14	DPSBKR14	8	8	4, 5 PCLK*3
0008 C29Fh	SYSTEM	Deep standby backup register 15	DPSBKR15	8	8	4, 5 PCLK*3
0008 C2A0h	SYSTEM	Deep standby backup register 16	DPSBKR16	8	8	4, 5 PCLK*3
0008 C2A1h	SYSTEM	Deep standby backup register 17	DPSBKR17	8	8	4, 5 PCLK*3
0008 C2A2h	SYSTEM	Deep standby backup register 18	DPSBKR18	8	8	4, 5 PCLK*3
0008 C2A3h	SYSTEM	Deep standby backup register 19	DPSBKR19	8	8	4, 5 PCLK*3
0008 C2A4h	SYSTEM	Deep standby backup register 20	DPSBKR20	8	8	4, 5 PCLK*3
0008 C2A5h	SYSTEM	Deep standby backup register 21	DPSBKR21	8	8	4, 5 PCLK*3
0008 C2A6h	SYSTEM	Deep standby backup register 22	DPSBKR22	8	8	4, 5 PCLK*3
0008 C2A7h	SYSTEM	Deep standby backup register 23	DPSBKR23	8	8	4, 5 PCLK*3
0008 C2A8h	SYSTEM	Deep standby backup register 24	DPSBKR24	8	8	4, 5 PCLK*3
0008 C2A9h	SYSTEM	Deep standby backup register 25	DPSBKR25	8	8	4, 5 PCLK*3
0008 C2AAh	SYSTEM	Deep standby backup register 26	DPSBKR26	8	8	4, 5 PCLK*3
0008 C2ABh	SYSTEM	Deep standby backup register 27	DPSBKR27	8	8	4, 5 PCLK*3
0008 C2ACh	SYSTEM	Deep standby backup register 28	DPSBKR28	8	8	4, 5 PCLK*3
0008 C2ADh	SYSTEM	Deep standby backup register 29	DPSBKR29	8	8	4, 5 PCLK*3
0008 C2AEh	SYSTEM	Deep standby backup register 30	DPSBKR30	8	8	4, 5 PCLK*3
0008 C2AFh	SYSTEM	Deep standby backup register 31	DPSBKR31	8	8	4, 5 PCLK*3
0008 C4C0h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLK*3
0008 C4C2h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLK*3
0008 C4C4h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLK*3
0008 C4C6h	POE	Output level control/status register 2	OCSR2	16	8, 16	2, 3 PCLK*3
0008 C4C8h	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLK*3
0008 C4CAh	POE	Software port output enable register	SPOER	8	8	2, 3 PCLK*3
0008 C4CBh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLK*3
0008 C4CCh	POE	Port output enable control register 2	POECR2	16	16	2, 3 PCLK*3
0008 C4CEh	POE	Port output enable control register 3	POECR3	16	16	2, 3 PCLK*3
0008 C4D0h	POE	Port output enable control register 4	POECR4	16	16	2, 3 PCLK*3
0008 C4D2h	POE	Port output enable control register 5	POECR5	16	16	2, 3 PCLK*3
0008 C4D4h	POE	Port output enable control register 6	POECR6	16	16	2, 3 PCLK*3
0008 C4D6h	POE	Input level control/status register 4	ICSR4	16	8, 16	2, 3 PCLK*3
0008 C4D8h	POE	Input level control/status register 5	ICSR5	16	8, 16	2, 3 PCLK*3
0008 C4DAh	POE	Active level setting register 1	ALR1	16	8, 16	2, 3 PCLK*3
0009 0200h to 0009 03FFh	CAN0*2	Mailbox registers 0 to 31	MB0 to MB 31	128	8, 16, 32	2, 3 PCLK*3
0009 0400h	CAN0*2	Mask register 0	MKR0	32	8, 16, 32	2, 3 PCLK*3
0009 0404h	CAN0*2	Mask register 1	MKR1	32	8, 16, 32	2, 3 PCLK*3
0009 0408h	CAN0*2	Mask register 2	MKR2	32	8, 16, 32	2, 3 PCLK*3
0009 040Ch	CAN0*2	Mask register 3	MKR3	32	8, 16, 32	2, 3 PCLK*3
0009 0410h	CAN0*2	Mask register 4	MKR4	32	8, 16, 32	2, 3 PCLK*3
0009 0414h	CAN0*2	Mask register 5	MKR5	32	8, 16, 32	2, 3 PCLK*3
0009 0418h	CAN0*2	Mask register 6	MKR6	32	8, 16, 32	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (20 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 200Ah	GPT	General PWM timer hardware stop/clear source select register	GTHPSR	16	8, 16, 32	3 to 5 ICLK*4
000C 200Ch	GPT	General PWM timer write-protection register	GTWP	16	8, 16, 32	3 to 5 ICLK*4
000C 200Eh	GPT	General PWM timer sync register	GTSYNC	16	8, 16, 32	3 to 5 ICLK*4
000C 2010h	GPT	General PWM timer external trigger input interrupt register	GTETINT	16	8, 16, 32	3 to 5 ICLK*4
000C 2014h	GPT	General PWM timer buffer operation disable register	GTBDR	16	8, 16, 32	3 to 5 ICLK*4
000C 2018h	GPT	General PWM timer start write protection register	GTSWP	16	16, 32	3 to 5 ICLK*4
000C 2080h	GPT	LOCO count control register	LCCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2082h	GPT	LOCO count status register	LCST	16	8, 16, 32	3 to 5 ICLK*4
000C 2084h	GPT	LOCO count value register	LCNT	16	8, 16, 32	3 to 5 ICLK*4
000C 2086h	GPT	LOCO count result average register	LCNTA	16	8, 16, 32	3 to 5 ICLK*4
000C 2088h	GPT	LOCO count result register 0	LCNT00	16	8, 16, 32	3 to 5 ICLK*4
000C 208Ah	GPT	LOCO count result register 1	LCNT01	16	8, 16, 32	3 to 5 ICLK*4
000C 208Ch	GPT	LOCO count result register 2	LCNT02	16	8, 16, 32	3 to 5 ICLK*4
000C 208Eh	GPT	LOCO count result register 3	LCNT03	16	8, 16, 32	3 to 5 ICLK*4
000C 2090h	GPT	LOCO count result register 4	LCNT04	16	8, 16, 32	3 to 5 ICLK*4
000C 2092h	GPT	LOCO count result register 5	LCNT05	16	8, 16, 32	3 to 5 ICLK*4
000C 2094h	GPT	LOCO count result register 6	LCNT06	16	8, 16, 32	3 to 5 ICLK*4
000C 2096h	GPT	LOCO count result register 7	LCNT07	16	8, 16, 32	3 to 5 ICLK*4
'000C 2098h	GPT	LOCO count result register 8	LCNT08	16	8, 16, 32	3 to 5 ICLK*4
000C 209Ah	GPT	LOCO count result register 9	LCNT09	16	8, 16, 32	3 to 5 ICLK*4
000C 209Ch	GPT	LOCO count result register 10	LCNT10	16	8, 16, 32	3 to 5 ICLK*4
000C 209Eh	GPT	LOCO count result register 11	LCNT11	16	8, 16, 32	3 to 5 ICLK*4
000C 20A0h	GPT	LOCO count result register 12	LCNT12	16	8, 16, 32	3 to 5 ICLK*4
000C 20A2h	GPT	LOCO count result register 13	LCNT13	16	8, 16, 32	3 to 5 ICLK*4
000C 20A4h	GPT	LOCO count result register 14	LCNT14	16	8, 16, 32	3 to 5 ICLK*4
000C 20A6h	GPT	LOCO count result register 15	LCNT15	16	8, 16, 32	3 to 5 ICLK*4
000C 20A8h	GPT	LOCO count upper permissible deviation register	LCNTDU	16	8, 16, 32	3 to 5 ICLK*4
000C 20AAh	GPT	LOCO count lower permissible deviation register	LCNTDL	16	8, 16, 32	3 to 5 ICLK*4
000C 2100h	GPT0	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK*4
000C 2102h	GPT0	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK*4
000C 2104h	GPT0	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2106h	GPT0	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK*4
000C 2108h	GPT0	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK*4
000C 210Ah	GPT0	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK*4
000C 210Ch	GPT0	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK*4
000C 210Eh	GPT0	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK*4
000C 2110h	GPT0	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK*4
000C 2112h	GPT0	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK*4
000C 2114h	GPT0	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK*4

Table 4.2 List of I/O Registers (Bit Order) (8 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IPR03	—	—	—	—	IPR[3:0]			
ICU	IPR04	—	—	—	—	IPR[3:0]			
ICU	IPR05	—	—	—	—	IPR[3:0]			
ICU	IPR06	—	—	—	—	IPR[3:0]			
ICU	IPR07	—	—	—	—	IPR[3:0]			
ICU	IPR14	—	—	—	—	IPR[3:0]			
ICU	IPR18	—	—	—	—	IPR[3:0]			
ICU	IPR20	—	—	—	—	IPR[3:0]			
ICU	IPR21	—	—	—	—	IPR[3:0]			
ICU	IPR22	—	—	—	—	IPR[3:0]			
ICU	IPR23	—	—	—	—	IPR[3:0]			
ICU	IPR24	—	—	—	—	IPR[3:0]			
ICU	IPR25	—	—	—	—	IPR[3:0]			
ICU	IPR26	—	—	—	—	IPR[3:0]			
ICU	IPR27	—	—	—	—	IPR[3:0]			
ICU	IPR40	—	—	—	—	IPR[3:0]			
ICU	IPR44	—	—	—	—	IPR[3:0]			
ICU	IPR48	—	—	—	—	IPR[3:0]			
ICU	IPR49	—	—	—	—	IPR[3:0]			
ICU	IPR51	—	—	—	—	IPR[3:0]			
ICU	IPR52	—	—	—	—	IPR[3:0]			
ICU	IPR53	—	—	—	—	IPR[3:0]			
ICU	IPR54	—	—	—	—	IPR[3:0]			
ICU	IPR55	—	—	—	—	IPR[3:0]			
ICU	IPR56	—	—	—	—	IPR[3:0]			
ICU	IPR57	—	—	—	—	IPR[3:0]			
ICU	IPR58	—	—	—	—	IPR[3:0]			
ICU	IPR59	—	—	—	—	IPR[3:0]			
ICU	IPR5A	—	—	—	—	IPR[3:0]			
ICU	IPR5B	—	—	—	—	IPR[3:0]			
ICU	IPR5C	—	—	—	—	IPR[3:0]			
ICU	IPR5D	—	—	—	—	IPR[3:0]			
ICU	IPR5E	—	—	—	—	IPR[3:0]			
ICU	IPR5F	—	—	—	—	IPR[3:0]			
ICU	IPR60	—	—	—	—	IPR[3:0]			
ICU	IPR67	—	—	—	—	IPR[3:0]			
ICU	IPR68	—	—	—	—	IPR[3:0]			
ICU	IPR69	—	—	—	—	IPR[3:0]			
ICU	IPR6A	—	—	—	—	IPR[3:0]			
ICU	IPR6B	—	—	—	—	IPR[3:0]			
ICU	IPR6C	—	—	—	—	IPR[3:0]			
ICU	IPR6D	—	—	—	—	IPR[3:0]			
ICU	IPR6E	—	—	—	—	IPR[3:0]			
ICU	IPR6F	—	—	—	—	IPR[3:0]			
ICU	IPR80	—	—	—	—	IPR[3:0]			
ICU	IPR81	—	—	—	—	IPR[3:0]			
ICU	IPR82	—	—	—	—	IPR[3:0]			
ICU	IPR88	—	—	—	—	IPR[3:0]			
ICU	IPR89	—	—	—	—	IPR[3:0]			
ICU	IPR8A	—	—	—	—	IPR[3:0]			
ICU	IPR8B	—	—	—	—	IPR[3:0]			
ICU	IPR90	—	—	—	—	IPR[3:0]			

Table 4.2 List of I/O Registers (Bit Order) (12 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
RSPI0	SSLP	—	—	—	—	SSLP3	SSLP2	SSLP1	SSLP0
RSPI0	SPPCR	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
RSPI0	SPSR	SPRF	—	SPTEF	—	PERF	MODF	IDLNF	OVRF
RSPI0	SPDR	H[15:0]							
		H[15:0]							
		L[15:0]							
		L[15:0]							
RSPI0	SPSCR	—	—	—	—	—		SPSLN[2:0]	
RSPI0	SPSSR	—		SPECM[2:0]		—		SPCP[2:0]	
RSPI0	SPBR	SPR7	SPR6	SPR5	SPR4	SPR3	SPR2	SPR1	SPR0
RSPI0	SPDCR	—	—	SPLW	SPRDTD	SLSEL[1:0]		SPFC[1:0]	
RSPI0	SPCKD	—	—	—	—	—		SCKDL[2:0]	
RSPI0	SSLND	—	—	—	—	—		SLNDL[2:0]	
RSPI0	SPND	—	—	—	—	—		SPNDL[2:0]	
RSPI0	SPCR2	—	—	—	—	PTE	SPIIE	SPOE	SPPE
RSPI0	SPCMD0	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD1	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD2	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD3	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD4	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD5	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD6	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD7	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
S12AD0	ADCSR	ADST	ADCS[1:0]		ADIE	CKS[1:0]		TRGE	EXTRG
S12AD0	ADANS	—	—	CH[1:0]		—	PG002SEL	PG001SEL	PG000SEL
		—	—	—	—	—	PG002EN	PG001EN	PG000EN
S12AD0	ADPG	—	—	—	—	PG002GAIN[3:0]			
		PG001GAIN[3:0]				PG000GAIN[3:0]			
S12AD0	ADCER	ADRFMT	—	ADIEW	ADIE2	DIAGM	DIAGLD	DIAGVAL[1:0]	
		—	—	ACE	—	—	ADPRC[1:0]		SHBYP
S12AD0	ADSTRGR	—	—	—	ADSTRS1[4:0]				
		—	—	—	ADSTRS0[4:0]				
S12AD	ADCMPMD0	—	—	CEN102[1:0]		CEN101[1:0]		CEN100[1:0]	
		—	—	CEN002[1:0]		CEN001[1:0]		CEN000[1:0]	
S12AD	ADCMPMD1	—	VSELL1	VSELH1	CSEL1	—	VSELL0	VSELH0	CSEL0
		—		REFH[2:0]		—		REFL[2:0]	
S12AD	ADCMPNR0	—	—	—	—	C002NR[3:0]			
		C001NR[3:0]				C000NR[3:0]			
S12AD	ADCMPNR1	—	—	—	—	C102NR[3:0]			
		C101NR[3:0]				C100NR[3:0]			
S12AD	ADCMPFR	—	—	C102FLAG	C101FLAG	C100FLAG	C002FLAG	C001FLAG	C000FLAG
S12AD	ADCMPSEL	—	—	—	—	—	—	POERQ	IE
		—	—	SEL102	SEL101	SEL100	SEL002	SEL001	SEL000

Table 4.2 List of I/O Registers (Bit Order) (14 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
PORT8	DR	—	—	—	—	—	B2	B1	B0
PORT9	DR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	DR	—	—	B5	B4	B3	B2	B1	B0
PORTB	DR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	DR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	DR	—	—	B5	B4	B3	—	B1	B0
PORTG	DR	—	—	B5	B4	B3	B2	B1	B0
PORT1	PORT	—	—	—	—	—	—	B1	B0
PORT2	PORT	—	—	—	B4	B3	B2	B1	B0
PORT3	PORT	—	—	—	—	B3	B2	B1	B0
PORT4	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORT5	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT6	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT7	PORT	—	B6	B5	B4	B3	B2	B1	B0
PORT8	PORT	—	—	—	—	—	B2	B1	B0
PORT9	PORT	—	B6	B5	B4	B3	B2	B1	B0
PORTA	PORT	—	—	B5	B4	B3	B2	B1	B0
PORTB	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	PORT	—	—	B5	B4	B3	B2	B1	B0
PORTG	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT1	ICR	—	—	—	—	—	—	B1	B0
PORT2	ICR	—	—	—	B4	B3	B2	B1	B0
PORT3	ICR	—	—	—	—	B3	B2	B1	B0
PORT4	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORT5	ICR	—	—	B5	B4	B3	B2	B1	B0
PORT6	ICR	—	—	B5	B4	B3	B2	B1	B0
PORT7	ICR	—	B6	B5	B4	B3	B2	B1	B0
PORT8	ICR	—	—	—	—	—	B2	B1	B0
PORT9	ICR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	ICR	—	—	B5	B4	B3	B2	B1	B0
PORTB	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	ICR	—	—	B5	B4	B3	—	B1	B0
PORTG	ICR	—	—	B5	B4	B3	B2	B1	B0
IOPORT	PF8IRQ	—	—	—	—	ITS1[1:0]		ITS0[1:0]	
IOPORT	PF9IRQ	—	—	—	—	—	ITS2	—	—
IOPORT	PFAADC	—	—	—	—	—	—	ADTRG1S	ADTRG0S
IOPORT	PFCMTU	TCLKS[1:0]		—	—	—	—	MTUS1	MTUS0
IOPORT	PFDGPT	—	—	—	—	—	—	—	GPTS
IOPORT	PFFSCI	—	—	—	—	—	SCI2S	—	—
IOPORT	PFGSPI	SSL3E	SSL2E	SSL1E	SSL0E	MISOE	MOSIE	RSPCKE	—
IOPORT	PFHSPI	—	—	—	—	—	—	RSPIS[1:0]	
IOPORT	PFJCAN	CANS[1:0]		—	—	—	—	—	CANE
IOPORT	PFKLIN	—	—	—	—	—	—	—	LINE
IOPORT	PFMPOE	—	—	—	POE11E	POE10E	POE8E	POE4E	POE0E
IOPORT	PFNPOE	POE10S	—	—	—	—	—	—	—
SYSTEM	DPSBYCR	DPSBY	IOKEEP	—	—	—	—	—	—
SYSTEM	DPSWCR	—	—	WTSTS[5:0]					
SYSTEM	DPSIER	DNMIE	—	—	DLVDE	—	—	DIRQ1E	DIRQ0E

Table 4.2 List of I/O Registers (Bit Order) (19 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU3	TGRA								
MTU3	TGRB								
MTU4	TGRA								
MTU4	TGRB								
MTU	TCNTSA								
MTU	TCBRA								
MTU3	TGRC								
MTU3	TGRD								
MTU4	TGRC								
MTU4	TGRD								
MTU3	TSR	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU4	TSR	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU	TITCR1A	T3AEN		T3ACOR[2:0]		T4VEN		T4VCOR[2:0]	
MTU	TBTERA	—		T3ACOR[2:0]		—		T4VCNT[2:0]]	
MTU	TBTERA	—	—	—	—	—	—	BTE[1:0]	
MTU	TDERA	—	—	—	—	—	—	—	TDER
MTU	TOLBRA	—	—	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
MTU3	TBTM	—	—	—	—	—	—	TTSB	TTSA
MTU4	TBTM	—	—	—	—	—	—	TTSB	TTSA
MTU	TITMRA	—	—	—	—	—	—	—	TITM
MTU	TITCR2A	—	—	—	—	—		TRG4COR[2:0]	
MTU	TITCNT2A	—	—	—	—	—		TRG4COR[2:0]	
MTU4	TADCR	BF[1:0]		—	—	—	—	—	—
		UT4AE	DT4AE	UT4BE	DT4BE	ITA3AE	ITA4VE	ITB3AE	ITB4VE
MTU4	TADCORA								
MTU4	TADCORB								
MTU4	TADCOBRA								
MTU4	TADCOBRB								
MTU	TWCRA	CCE	—	—	—	—	—	—	WRE
MTU	TMDR2A	—	—	—	—	—	—	—	DRS
MTU3	TGRE								
MTU4	TGRE								
MTU4	TGRF								
MTU	TSTRA	CST4	CST3	—	—	—	CST2	CST1	CST0
MTU	TSYRA	SYNC4	SYNC3	—	—	—	SYNC2	SYNC1	SYNC0
MTU	TCSYSTR	SCH0	SCH1	SCH2	SCH3	SCH4	—	SCH6	SCH7
MTU	TRWERA	—	—	—	—	—	—	—	RWE
MTU0	TCR		CCLR[2:0]			CKEG[1:0]		TPSC[2:0]	

5.2 DC Characteristics

Table 5.2 DC Characteristics (1) (1 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CAN input pin IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin NMI input pin GPT input pin LIN input pin RES#	V_{IH}	VCC×0.8	-	VCC+0.3	V	
		V_{IL}	-0.3	-	VCC×0.2		
		ΔV_T	VCC ×0.06	-	-		
	RIIC input pin (IICBus)	V_{IH}	VCC×0.7	-	VCC+0.3		
		V_{IL}	-0.3	-	VCC×0.3		
		ΔV_T	VCC ×0.05	-	-		
	Port 4*1 (also usable as an analog port)	V_{IH}	AVCC0 ×0.8	-	AVCC0 +0.3		
		V_{IL}	- 0.3	-	AVCC0 ×0.2		
		ΔV_T	AVCC0 ×0.06	-	-		
	Ports 5 and 6*1 (also usable as analog ports)	V_{IH}	AVCC ×0.8	-	AVCC +0.3		
		V_{IL}	-0.3	-	AVCC ×0.2		
		ΔV_T	AVCC ×0.06	-	-		
	Ports 1 to 3*1 Ports 7 to B*1 Ports D, E, and G*1	V_{IH}	VCC×0.8	-	VCC+0.3		
		V_{IL}	-0.3	-	VCC×0.2		
		ΔV_T	VCC ×0.06	-	-		
Input high voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC×0.9	-	VCC+0.3	V	
	EXTAL RSPI input pin		VCC×0.8		VCC+0.3		
	RIIC input pin (SMBus)		2.1		VCC+0.3		Conditions 1 and 2
Input low voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	-0.3	-	VCC×0.1	V	
	EXTAL RSPI input pin		-0.3	-	VCC×0.2		
	RIIC input pin (SMBus)		-0.3	-	0.8		Conditions 1 and 2

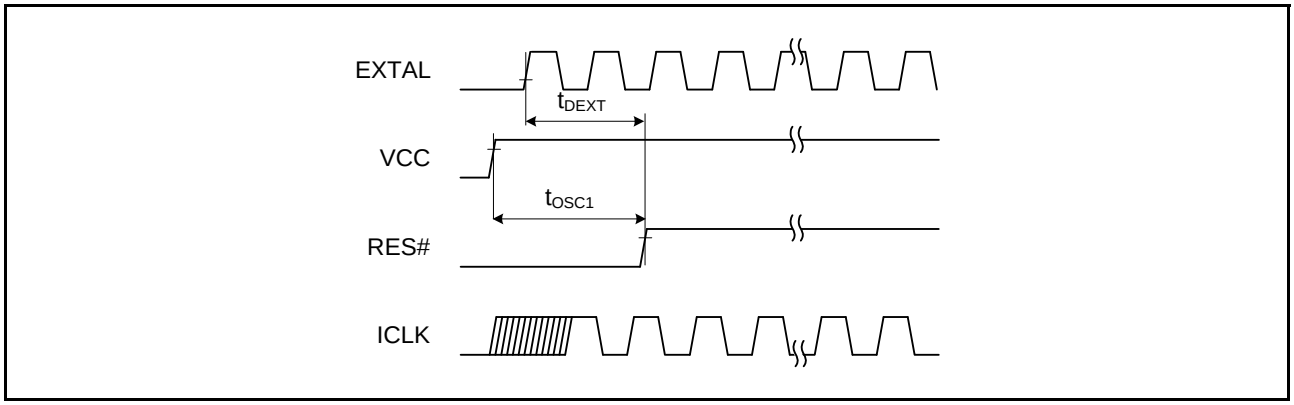


Figure 5.1 Oscillation Settling Timing

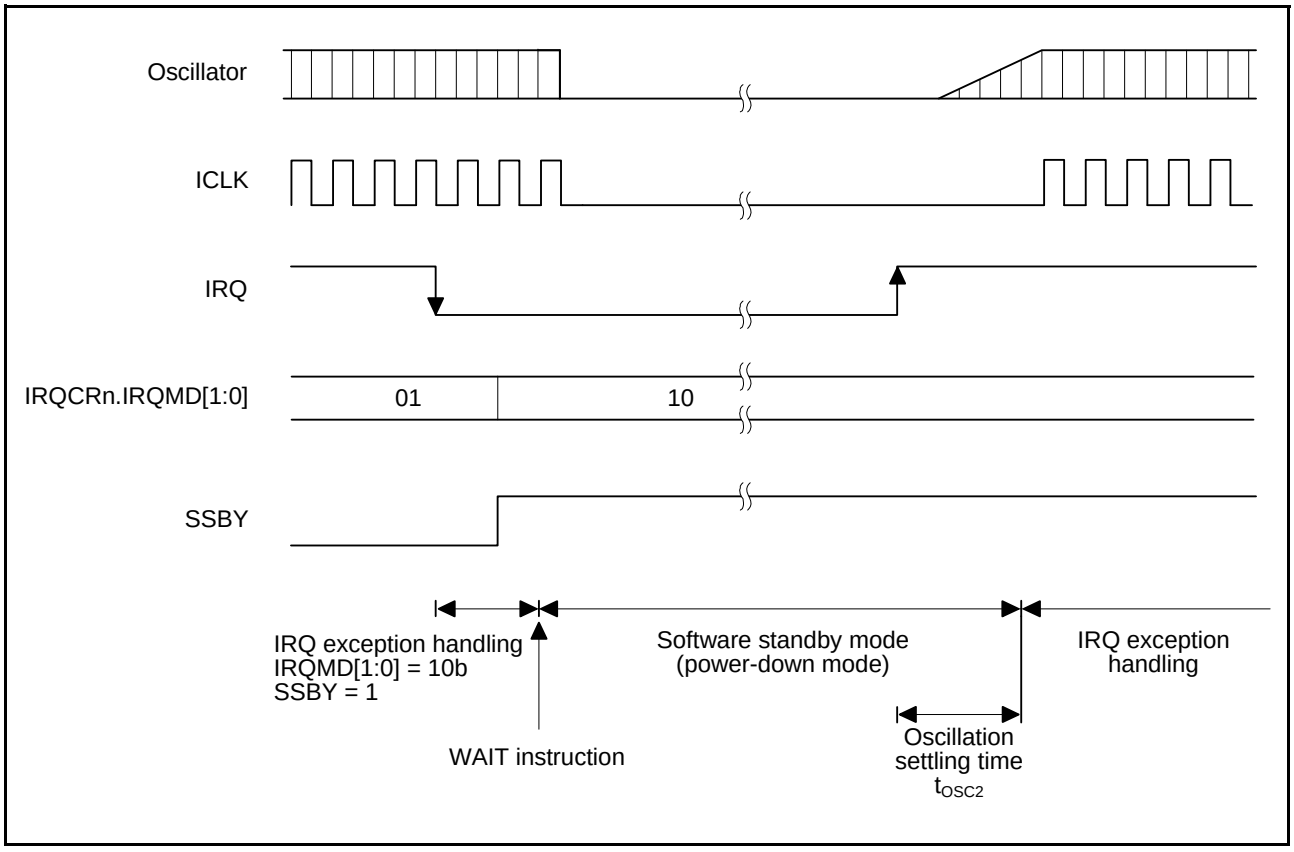


Figure 5.2 Oscillation Settling Timing after Software Standby Mode

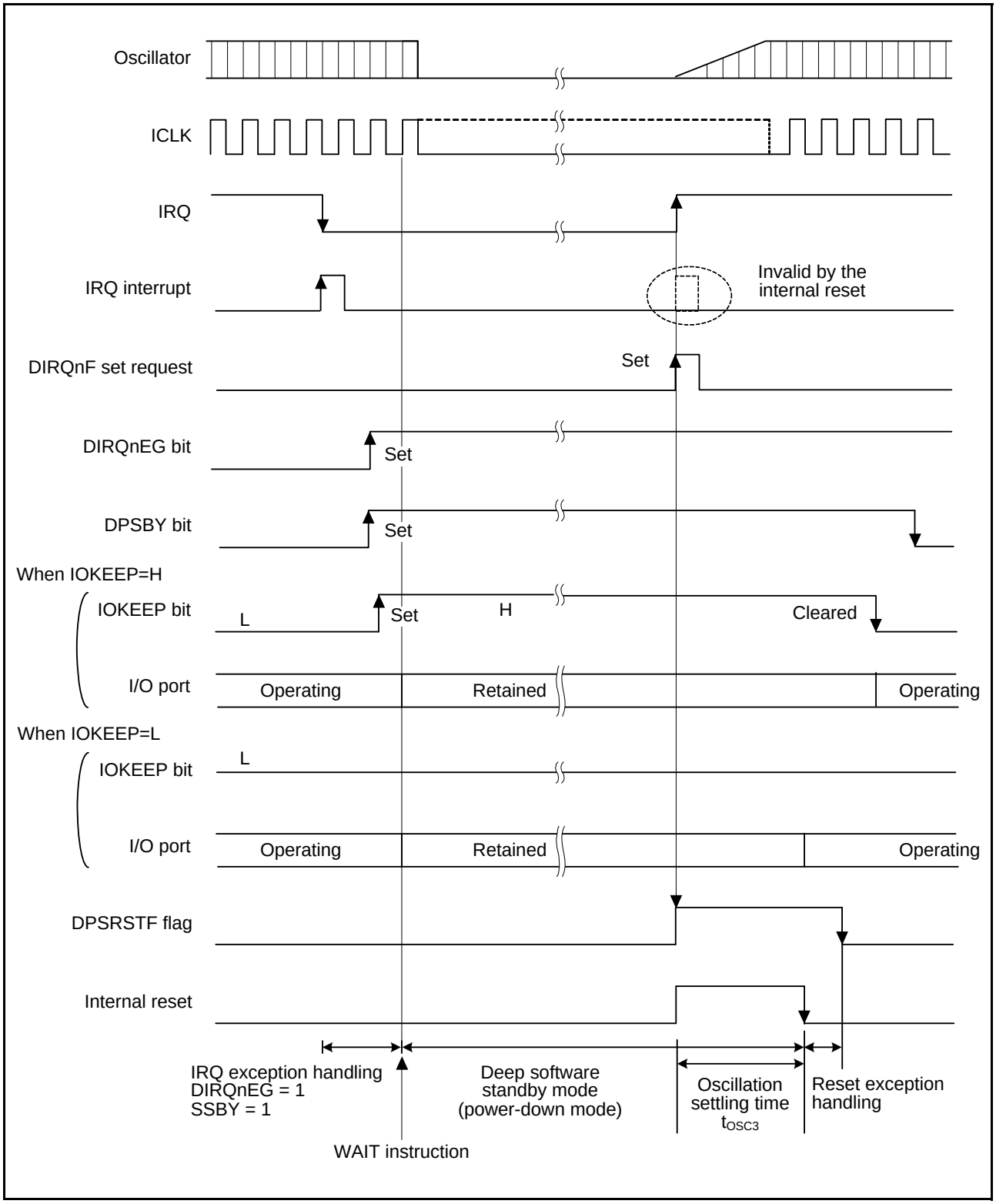


Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode

5.6 Oscillation Stop Detection Timing

Table 5.20 Oscillation Stop Detection Circuit Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	tdr	-	-	1.0	ms	Figure 5.23
Internal oscillation frequency when oscillation stop is detected	f_{MAIN}	0.5	-	7.0	MHz	

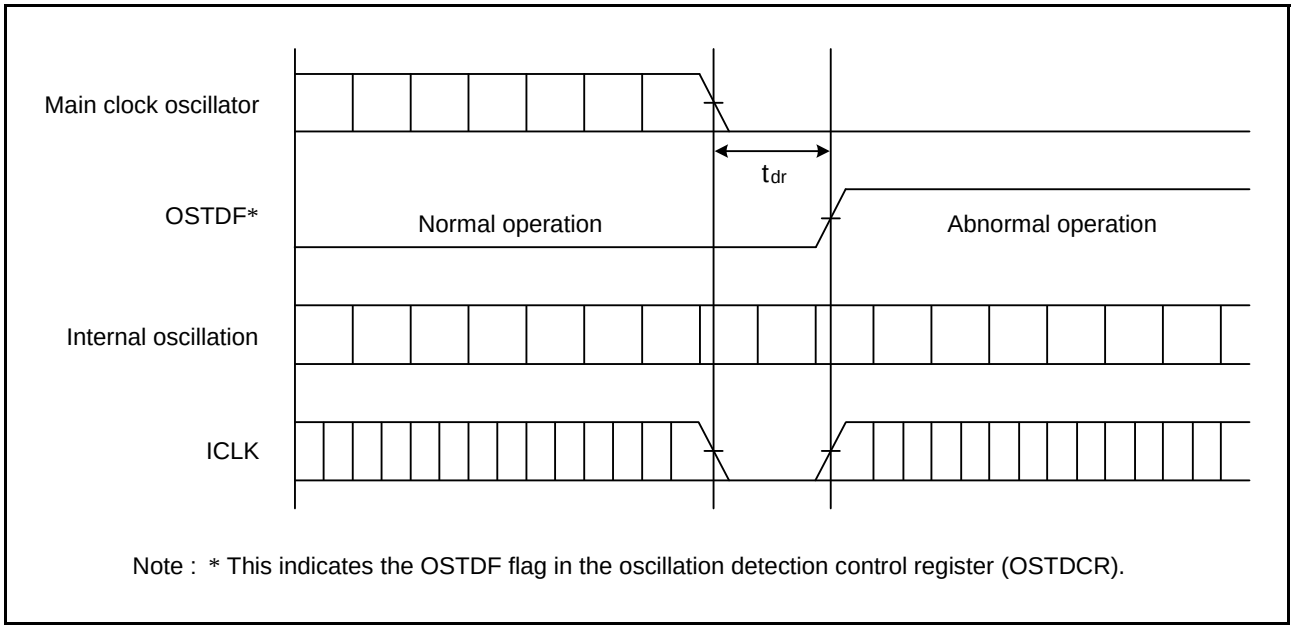


Figure 5.23 Oscillation Stop Detection Timing

5.7 ROM (Flash Memory for Code Storage) Characteristics

Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	N_{PEC}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	Ta = +85C°

Note 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

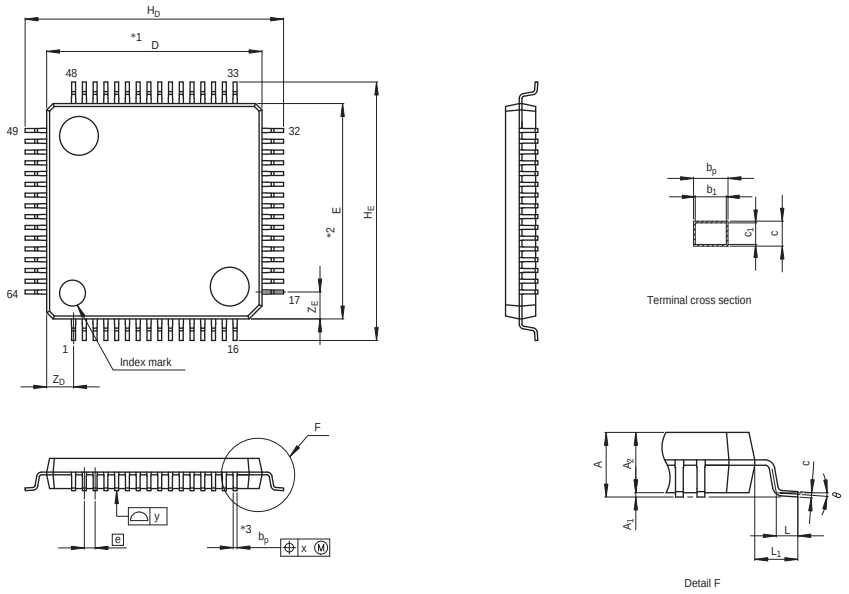
Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t_{P256}	—	2	12	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	256 byte	t_{P256}	—	2.4	14.4	ms	PCLK = 50 MHz $N_{PEC} > 100$
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	PCLK = 50 MHz $N_{PEC} > 100$
	16 Kbytes	t_{E16K}	—	120	288	ms	
Suspend delay time during writing		t_{SPD}	—	—	120	µs	Figure 5.24 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure D 64-Pin LQFP (PLQP0064KB-A) Package Dimensions