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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562taddfk-v3

Table 1.1 Outline of Specifications (5 / 5)

Classification	Module/Function	Description
A/D converter	10-bit A/D converter (ADA)	• 10 bits (1 unit x 12 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V • Two basic operating modes - Single mode and scan mode • Scan mode - One-cycle scan mode - Continuous scan mode • Sample-and-hold function - A common sample-and-hold circuit for both units is included. • A/D-conversion register settings for each input pin • Three ways to start A/D conversion - Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8-bit precision output - Right-shifting the results of conversion for output by two bits is selectable. • Self-diagnostic function - The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF).
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Operating frequency		ICLK: 8 to 100 MHz PCLK: 8 to 50 MHz
Power supply voltage		• 3-V version - VCC = PLLVCC = 2.7 to 3.6V - AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V - VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 - VREF = 3.0 to AVCC, or 4.0 to AVCC • 5-V version - VCC = PLLVCC = 4.0 to 5.5V - AVCC0 = AVCC = 4.0 to 5.5V - VREFH0 = 4.0 to AVCC0 - VREF = 4.0 to AVCC
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Packages		112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch) 100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch) 80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch) 64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch) 64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.2 Functions of RX62T Group and RX62G Group Products (1 / 2)

Functions		RX62G Group		RX62T Group				
Pin number		112 Pins	100 Pins	112 Pins	100 Pins	80 Pins (R5F562T xGDFF)	80 Pins	64 Pins
Data transfer	Data transfer controller (DTC)	√						
Interrupt controller (ICU)	Input on the NMI pin	√						
	Input on the IRQ pins	√ (8)						√ (4)
Timers	Multi-function timer pulse unit 3 (MTU3)	√				√*1		
	General PWM timer (GPT)	—		√		√*1		
	General PWM timer (GPTa)	√		—				
	MTU3/GPT complementary PWM pin	12					6	
	Port output enable 3 (POE3)	√ (POE pins: 5)						√ (POE pins: 3)
	Compare match timer (CMT)	√						
	Watchdog timer (WDT)	√						
	Independent watchdog timer (IWDT)	√						
Communication function	Serial communications interface (SCI)	√						
	I ² C bus interface (RIIC)	√						
	CAN module (CAN) (as an optional function)	√						
	LIN module (LIN)	√						
	Serial peripheral interface (RSPI)	√						
12-bit A/D converter (S12ADA)		√ (4 ch. x 2 units)						
	Simultaneous sampling on three channels	√ (2 units)						
	Programmable gain amplifier	√ (3 ch. x 2 units)						
	Window comparator	√ (3 ch. x 2 units)						
10-bit A/D converter (ADA)		√ (12 ch.)				√ (4 ch.)		—
CRC calculator (CRC)		√						
I/O ports	I/O pins	61	55	61	55	44	44	37
	Input pins	21	21	21	21	13	13	9

1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

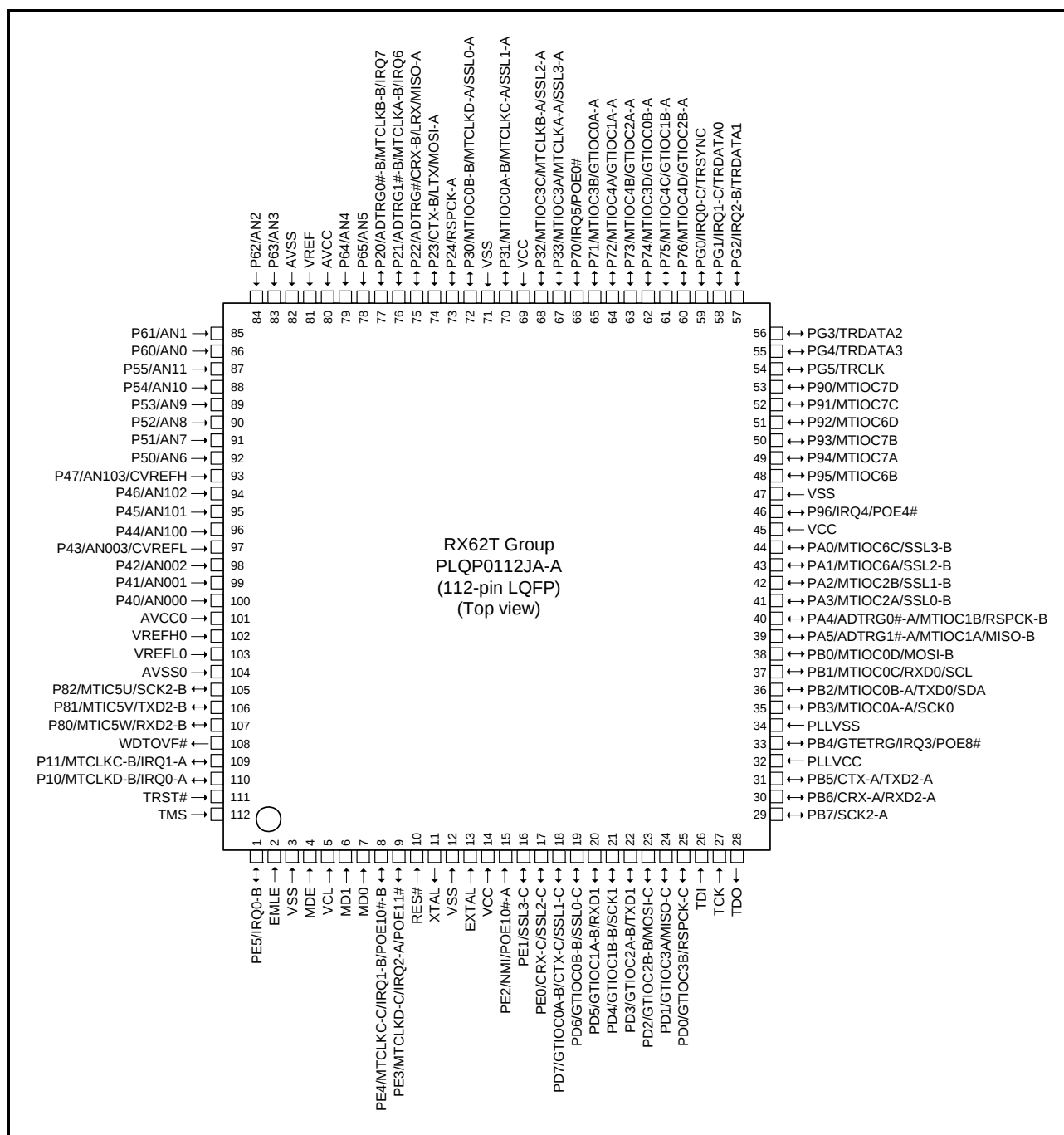


Figure 1.3 Pin Assignment of the 112-Pin LQFP

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (2 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
44		PA0		MTIOC6C	SSL3-B			
45	VCC							
46		P96				IRQ4	POE4#	
47	VSS							
48		P95		MTIOC6B				
49		P94		MTIOC7A				
50		P93		MTIOC7B				
51		P92		MTIOC6D				
52		P91		MTIOC7C				
53		P90		MTIOC7D				
54		PG5						TRCLK
55		PG4						TRDATA3
56		PG3						TRDATA2
57		PG2				IRQ2-B		TRDATA1
58		PG1				IRQ1-C		TRDATA0
59		PG0				IRQ0-C		TRSYNC
60		P76		MTIOC4D/ GTIOC2B-A				
61		P75		MTIOC4C/ GTIOC1B-A				
62		P74		MTIOC3D/ GTIOC0B-A				
63		P73		MTIOC4B/ GTIOC2A-A				
64		P72		MTIOC4A/ GTIOC1A-A				
65		P71		MTIOC3B/ GTIOC0A-A				
66		P70				IRQ5	POE0#	
67		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
68		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
69	VCC							
70		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
71	VSS							
72		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
73		P24			RSPCK-A			
74		P23			CTX-B/ LTX/ MOSI-A			
75		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
76		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
77		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
78		P65	AN5					
79		P64	AN4					

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
76	AVSS0							
77		P11		MTCLKC-B		IRQ1-A		
78		P10		MTCLKD-B		IRQ0-A		
79		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
80		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
76	AVSS0							
77		P82		MTIC5U	SCK2-B			
78		P81		MTIC5V	TXD2-B			
79		P80		MTIC5W	RXD2-B			
80		P10		MTCLKD-B		IRQ0-A		

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	16	16	3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region 0 start page-number register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region 0 end page-number register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region 1 start page-number register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region 1 end page-number register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region 2 start page-number register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region 2 end page-number register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region 3 start page-number register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region 3 end page-number register	REPAGE3	32	32	1 ICLK
0008 6420h	MPU	Region 4 start page-number register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region 4 end page-number register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region 5 start page-number register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region 5 end page-number register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region 6 start page-number register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region 6 end page-number register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region 7 start page-number register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region 7 end page-number register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background access control register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region search address register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region search operation register	MPOPS	16	16	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (19 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 1A39h	MTU7	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK
000C 1A3Ah	MTU	Timer interrupt skipping mode register B	TITMRB	8	8	5 ICLK
000C 1A3Bh	MTU	Timer interrupt skipping set register 2B	TITCR2B	8	8	5 ICLK
000C 1A3Ch	MTU	Timer interrupt skipping counter 2B	TITCNT2B	8	8	5 ICLK
000C 1A40h	MTU7	Timer A/D converter start request control register	TADCR	16	16	5 ICLK
000C 1A44h	MTU7	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	5 ICLK
000C 1A46h	MTU7	Timer A/D converter start request cycle set register B	TADCORB	16	16	5 ICLK
000C 1A48h	MTU7	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	5 ICLK
000C 1A4Ah	MTU7	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	5 ICLK
000C 1A50h	MTU6	Timer synchronous clear register	TSYCR	8	8	5 ICLK
000C 1A60h	MTU	Timer waveform control register B	TWCRB	8	8	5 ICLK
000C 1A70h	MTU	Timer mode register 2B	TMDR2B	8	8	5 ICLK
000C 1A72h	MTU6	Timer general register E	TGRE	16	16	5 ICLK
000C 1A74h	MTU7	Timer general register E	TGRE	16	16	5 ICLK
000C 1A76h	MTU7	Timer general register F	TGRF	16	16	5 ICLK
000C 1A80h	MTU	Timer start register B	TSTRB	8	8, 16	5 ICLK
000C 1A81h	MTU	Timer synchronous register B	TSYRB	8	8	5 ICLK
000C 1A84h	MTU	Timer read/write enable register B	TRWERB	8	8	5 ICLK
000C 1C80h	MTU5	Timer counter U	TCNTU	16	16, 32	5 ICLK
000C 1C82h	MTU5	Timer general register U	TGRU	16	16	5 ICLK
000C 1C84h	MTU5	Timer control register U	TCRU	8	8	5 ICLK
000C 1C86h	MTU5	Timer I/O control register U	TIORU	8	8	5 ICLK
000C 1C90h	MTU5	Timer counter V	TCNTV	16	16, 32	5 ICLK
000C 1C92h	MTU5	Timer general register V	TGRV	16	16	5 ICLK
000C 1C94h	MTU5	Timer control register V	TCRV	8	8	5 ICLK
000C 1C96h	MTU5	Timer I/O control register V	TIORV	8	8	5 ICLK
000C 1CA0h	MTU5	Timer counter W	TCNTW	16	16, 32	5 ICLK
000C 1CA2h	MTU5	Timer general register W	TGRW	16	16	5 ICLK
000C 1CA4h	MTU5	Timer control register W	TCRW	8	8	5 ICLK
000C 1CA6h	MTU5	Timer I/O control register W	TIORW	8	8	5 ICLK
000C 1CB0h	MTU5	Timer status register	TSR	8	8	5 ICLK
000C 1CB2h	MTU5	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 1CB4h	MTU5	Timer start register	TSTR	8	8	5 ICLK
000C 1CB6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	5 ICLK
000C 2000h	GPT	General PWM timer software start register	GTSTR	16	8, 16, 32	3 to 5 ICLK*4
000C 2004h	GPT	General PWM timer hardware source start control register	GTHSCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2006h	GPT	General PWM timer hardware source clear control register	GTHCCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2008h	GPT	General PWM timer hardware start source select register	GTHSSR	16	8, 16, 32	3 to 5 ICLK*4

Table 4.1 List of I/O Registers (Address Order) (22 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 21A0h	GPT1	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 21A4h	GPT1	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 21A6h	GPT1	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 21A8h	GPT1	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 21ACh	GPT1	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 21AEh	GPT1	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B0h	GPT1	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B4h	GPT1	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B6h	GPT1	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B8h	GPT1	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 21BAh	GPT1	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 21BCh	GPT1	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 21BEh	GPT1	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 21C0h	GPT1	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 21C2h	GPT1	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2200h	GPT2	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2202h	GPT2	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2204h	GPT2	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2206h	GPT2	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2208h	GPT2	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 220Ah	GPT2	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 220Ch	GPT2	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 220Eh	GPT2	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2210h	GPT2	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2212h	GPT2	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2214h	GPT2	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}
000C 2216h	GPT2	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2218h	GPT2	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 221Ah	GPT2	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 221Ch	GPT2	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 221Eh	GPT2	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2220h	GPT2	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2224h	GPT2	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2226h	GPT2	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2228h	GPT2	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.1 List of I/O Registers (Address Order) (25 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 PCLK ^{*3}
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 PCLK ^{*3}
007F FFCAh	FLASH	Data flash blank check control register	DFLBCCNT	16	16	2, 3 PCLK ^{*3}
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 PCLK ^{*3}
007F FFCEh	FLASH	Data flash blank check status register	DFLBCSTAT	16	16	2, 3 PCLK ^{*3}
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 PCLK ^{*3}

Note 1. This register is not supported by the 100-pin LQFP version.

Note 2. This register is not supported by the product without the CAN function.

Note 3. The number of access states depends on the number of divided cycles for clock synchronization (0 to 1 PCLK).

Note 4. Reading the registers takes 3 cycles of ICLK and writing to the registers takes 5 cycles of ICLK.

Table 4.2 List of I/O Registers (Bit Order) (6 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	DTCER029	—	—	—	—	—	—	—	DTCE
ICU	DTCER030	—	—	—	—	—	—	—	DTCE
ICU	DTCER031	—	—	—	—	—	—	—	DTCE
ICU	DTCER045	—	—	—	—	—	—	—	DTCE
ICU	DTCER046	—	—	—	—	—	—	—	DTCE
ICU	DTCER064	—	—	—	—	—	—	—	DTCE
ICU	DTCER065	—	—	—	—	—	—	—	DTCE
ICU	DTCER066	—	—	—	—	—	—	—	DTCE
ICU	DTCER067	—	—	—	—	—	—	—	DTCE
ICU	DTCER068	—	—	—	—	—	—	—	DTCE
ICU	DTCER069	—	—	—	—	—	—	—	DTCE
ICU	DTCER070	—	—	—	—	—	—	—	DTCE
ICU	DTCER071	—	—	—	—	—	—	—	DTCE
ICU	DTCER098	—	—	—	—	—	—	—	DTCE
ICU	DTCER102	—	—	—	—	—	—	—	DTCE
ICU	DTCER103	—	—	—	—	—	—	—	DTCE
ICU	DTCER106	—	—	—	—	—	—	—	DTCE
ICU	DTCER114	—	—	—	—	—	—	—	DTCE
ICU	DTCER115	—	—	—	—	—	—	—	DTCE
ICU	DTCER116	—	—	—	—	—	—	—	DTCE
ICU	DTCER117	—	—	—	—	—	—	—	DTCE
ICU	DTCER121	—	—	—	—	—	—	—	DTCE
ICU	DTCER122	—	—	—	—	—	—	—	DTCE
ICU	DTCER125	—	—	—	—	—	—	—	DTCE
ICU	DTCER126	—	—	—	—	—	—	—	DTCE
ICU	DTCER129	—	—	—	—	—	—	—	DTCE
ICU	DTCER130	—	—	—	—	—	—	—	DTCE
ICU	DTCER131	—	—	—	—	—	—	—	DTCE
ICU	DTCER132	—	—	—	—	—	—	—	DTCE
ICU	DTCER134	—	—	—	—	—	—	—	DTCE
ICU	DTCER135	—	—	—	—	—	—	—	DTCE
ICU	DTCER136	—	—	—	—	—	—	—	DTCE
ICU	DTCER137	—	—	—	—	—	—	—	DTCE
ICU	DTCER138	—	—	—	—	—	—	—	DTCE
ICU	DTCER139	—	—	—	—	—	—	—	DTCE
ICU	DTCER140	—	—	—	—	—	—	—	DTCE
ICU	DTCER141	—	—	—	—	—	—	—	DTCE
ICU	DTCER142	—	—	—	—	—	—	—	DTCE
ICU	DTCER143	—	—	—	—	—	—	—	DTCE
ICU	DTCER144	—	—	—	—	—	—	—	DTCE
ICU	DTCER145	—	—	—	—	—	—	—	DTCE
ICU	DTCER149	—	—	—	—	—	—	—	DTCE
ICU	DTCER150	—	—	—	—	—	—	—	DTCE
ICU	DTCER151	—	—	—	—	—	—	—	DTCE
ICU	DTCER152	—	—	—	—	—	—	—	DTCE
ICU	DTCER153	—	—	—	—	—	—	—	DTCE
ICU	DTCER174	—	—	—	—	—	—	—	DTCE
ICU	DTCER175	—	—	—	—	—	—	—	DTCE
ICU	DTCER176	—	—	—	—	—	—	—	DTCE
ICU	DTCER177	—	—	—	—	—	—	—	DTCE
ICU	DTCER178	—	—	—	—	—	—	—	DTCE
ICU	DTCER179	—	—	—	—	—	—	—	DTCE

Table 4.2 List of I/O Registers (Bit Order) (8 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IPR03	—	—	—	—			IPR[3:0]	
ICU	IPR04	—	—	—	—			IPR[3:0]	
ICU	IPR05	—	—	—	—			IPR[3:0]	
ICU	IPR06	—	—	—	—			IPR[3:0]	
ICU	IPR07	—	—	—	—			IPR[3:0]	
ICU	IPR14	—	—	—	—			IPR[3:0]	
ICU	IPR18	—	—	—	—			IPR[3:0]	
ICU	IPR20	—	—	—	—			IPR[3:0]	
ICU	IPR21	—	—	—	—			IPR[3:0]	
ICU	IPR22	—	—	—	—			IPR[3:0]	
ICU	IPR23	—	—	—	—			IPR[3:0]	
ICU	IPR24	—	—	—	—			IPR[3:0]	
ICU	IPR25	—	—	—	—			IPR[3:0]	
ICU	IPR26	—	—	—	—			IPR[3:0]	
ICU	IPR27	—	—	—	—			IPR[3:0]	
ICU	IPR40	—	—	—	—			IPR[3:0]	
ICU	IPR44	—	—	—	—			IPR[3:0]	
ICU	IPR48	—	—	—	—			IPR[3:0]	
ICU	IPR49	—	—	—	—			IPR[3:0]	
ICU	IPR51	—	—	—	—			IPR[3:0]	
ICU	IPR52	—	—	—	—			IPR[3:0]	
ICU	IPR53	—	—	—	—			IPR[3:0]	
ICU	IPR54	—	—	—	—			IPR[3:0]	
ICU	IPR55	—	—	—	—			IPR[3:0]	
ICU	IPR56	—	—	—	—			IPR[3:0]	
ICU	IPR57	—	—	—	—			IPR[3:0]	
ICU	IPR58	—	—	—	—			IPR[3:0]	
ICU	IPR59	—	—	—	—			IPR[3:0]	
ICU	IPR5A	—	—	—	—			IPR[3:0]	
ICU	IPR5B	—	—	—	—			IPR[3:0]	
ICU	IPR5C	—	—	—	—			IPR[3:0]	
ICU	IPR5D	—	—	—	—			IPR[3:0]	
ICU	IPR5E	—	—	—	—			IPR[3:0]	
ICU	IPR5F	—	—	—	—			IPR[3:0]	
ICU	IPR60	—	—	—	—			IPR[3:0]	
ICU	IPR67	—	—	—	—			IPR[3:0]	
ICU	IPR68	—	—	—	—			IPR[3:0]	
ICU	IPR69	—	—	—	—			IPR[3:0]	
ICU	IPR6A	—	—	—	—			IPR[3:0]	
ICU	IPR6B	—	—	—	—			IPR[3:0]	
ICU	IPR6C	—	—	—	—			IPR[3:0]	
ICU	IPR6D	—	—	—	—			IPR[3:0]	
ICU	IPR6E	—	—	—	—			IPR[3:0]	
ICU	IPR6F	—	—	—	—			IPR[3:0]	
ICU	IPR80	—	—	—	—			IPR[3:0]	
ICU	IPR81	—	—	—	—			IPR[3:0]	
ICU	IPR82	—	—	—	—			IPR[3:0]	
ICU	IPR88	—	—	—	—			IPR[3:0]	
ICU	IPR89	—	—	—	—			IPR[3:0]	
ICU	IPR8A	—	—	—	—			IPR[3:0]	
ICU	IPR8B	—	—	—	—			IPR[3:0]	
ICU	IPR90	—	—	—	—			IPR[3:0]	

Table 4.2 List of I/O Registers (Bit Order) (27 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT2	GTPBR								
GPT2	GTPDBR								
GPT2	GTADTRA								
GPT2	GTADTBRA								
GPT2	GTADTDBRA								
GPT2	GTADTRB								
GPT2	GTADTBRB								
GPT2	GTADTDBRB								
GPT2	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
		NFS[3:0]				NVB	NVA	NEB	NEA
GPT2	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT2	GTDVU								
GPT2	GTDVD								
GPT2	GTDBU								
GPT2	GTDBD								
GPT2	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT2	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT3	GTIOR	OBHLD	OBDFLT			GTIOB[5:0]			
		OAHLd	OADFLt			GTIOA[5:0]			
GPT3	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA
GPT3	GTCR	—	—	CCLR[1:0]		—	—	—	—
		—	—	—	—	—	—	—	—
GPT3	GTBER	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]	
		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
GPT3	GTUDC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	UDF	UD
GPT3	GTITC	—	ADTBL	—	ADTAL	—	—	IVTT[2:0]	
		IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
GPT3	GTST	TUCF	—	—	—	DTEF	—	ITCNT[2:0]	
		TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
GPT3	GCNT								
GPT3	GTCCRA								

Table 4.2 List of I/O Registers (Bit Order) (29 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT2	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLEN
GPT3	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLEN
GPT0	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT0	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT0	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT0	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
FLASH	FMODR	—	—	—	FRDMD	—	—	—	—
FLASH	FASTAT	ROMAE	—	—	CMDLK	DFLAE	—	DFLRPE	DFLWPE
FLASH	FAEINT	ROMAEIE	—	—	CMDLKIE	DFLAEIE	—	DFLRPEIE	DFLWPEIE
FLASH	FRDYIE	—	—	—	—	—	—	—	FRDYIE
FLASH	DFLRE0	KEY[7:0]							
		DBRE07	DBRE06	DBRE05	DBRE04	DBRE03	DBRE02	DBRE01	DBRE00
FLASH	DFLRE1	KEY[7:0]							
		DBRE15	DBRE14	DBRE13	DBRE12	DBRE11	DBRE10	DBRE09	DBRE08
FLASH	DFLWE0	KEY[7:0]							
		DBWE07	DBWE06	DBWE05	DBWE04	DBWE03	DBWE02	DBWE01	DBWE00
FLASH	DFLWE1	KEY[7:0]							
		DBWE15	DBWE14	DBWE13	DBWE12	DBWE11	DBWE10	DBWE09	DBWE08
FLASH	FCURAME	KEY[7:0]							
		—	—	—	—	—	—	—	FCRME

Table 5.2 DC Characteristics (1) (3 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input capacitance	All input pins (except for ports PB1 and PB2)	C _{in}	-	-	15	pF	V _{in} = 0 V, f = 1 MHz, T _a = 25°C
	Ports PB1 and PB2		-	-	30		

Note 1. This includes the multiplexed input pins, except in cases where port pins PB1 and PB2 are used as IIC input pins or port pins P22 to P24, P30, PA3 to PA5, PB0, PD0 to PD2, or PD6 are used as RSPI input pins.

Table 5.3 DC Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Supply current*1	In operation	Max.*2	I _{CC} *3	-	-	70	mA	ICLK = 100 MHz PCLK = 50 MHz	
		Normal*4		-	35	-			
		Increased by BGO operation*5		-	15	-			
	Sleep				22	60			
	All-module-clock-stop mode*6				14	28			
	Standby mode	Software standby mode		-	0.10	3	mA		
		Deep software standby mode		-	20	60	μA		
	Analog power supply current	During 12-bit A/D conversion (when a sample-and-hold circuit is in use; per unit)		AI _{CC0}	-	3	5	mA	
During 12-bit A/D conversion (when a sample-and-hold circuit is not in use; per unit)		-	3		5	mA			
Programmable gain amp (per channel)		-	1		2	mA			
Window comparator (1 channel)			0.5		1	mA			
Window comparator (6 channels)		-	1		2	mA			
During 12-bit A/D conversion (per unit)		-	60		90	μA			
During 10-bit A/D conversion (per unit)		AI _{CC}	-	0.9	2	mA			
Waiting for 10-bit A/D conversion (all units)			-	0.3	3	μA			
Reference power supply current	During 12-bit A/D conversion (per unit)		AI _{REFH0}	-	1.6	3	mA		
	Waiting for 12-bit A/D conversion (all units)			-	1.6	3	mA		
	During 10-bit A/D conversion (per unit)		AI _{REF}	-	0.1	1	mA		
	Waiting for 10-bit A/D conversion (all units)			-	0.1	3	μA		
VCC rising gradient			SV _{CC}	-	-	20	ms/V		

Note 1. Supply current values are with all output pins unloaded.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)

ICC max. = 0.54 × f + 16 (max.)

ICC max. = 0.3 × f + 5 (normal operation)

ICC max. = 0.44 × f + 16 (sleep mode)

Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.

Note 5. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.

Note 6. The values are for reference.

5.3.2 Control Signal Timing

Table 5.8 Control Signal Timing

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory*1)	t_{RESW}^{*2}	20	-	t_{cyc}^{*4}	Figure 5.5
		1.5	-	μs	
Internal reset time*3	t_{RESW2}	35	-	μs	
NMI pulse width	t_{NMIW}	200	-	ns	Figure 5.6
IRQ pulse width	t_{IRQW}	200	-	ns	Figure 5.7

Note 1. For a reset by the signal on the RES# pin during programming or erasure of the ROM or data-flash memory or during blank checking of the data-flash memory, see section 31.12, Usage Notes in section 31, ROM (Flash Memory for Code Storage) in the User's manual: Hardware.

Note 2. Both the time and the number of cycles should satisfy the specifications.

Note 3. This is to specify the FCU reset.

Note 4. ICLK cycles.

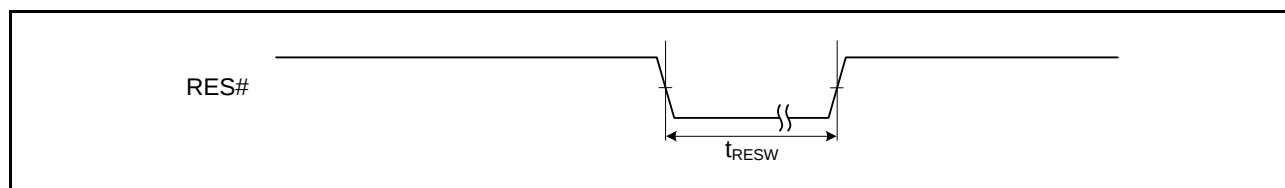


Figure 5.5 Reset Input Timing

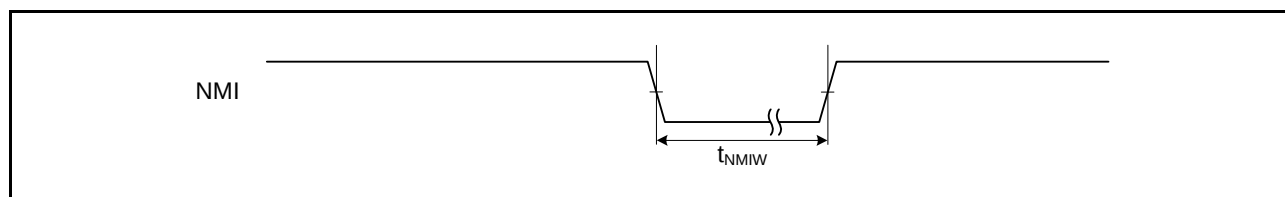


Figure 5.6 NMI Interrupt Input Timing

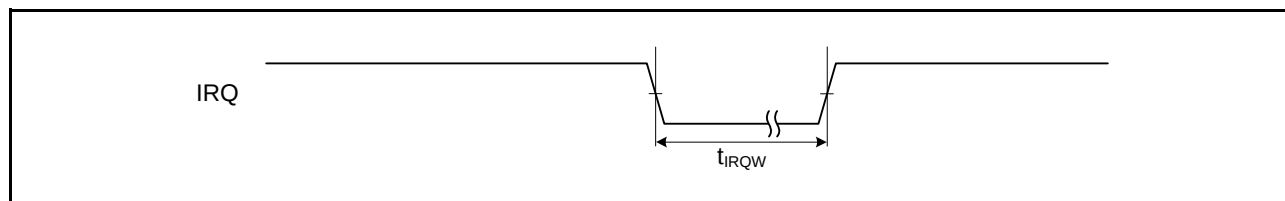


Figure 5.7 IRQ Interrupt Input Timing

Table 5.17 Characteristics of the Programmable Gain Amplifier

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		Cin	-	-	6	pF	
Input offset voltage		Voff	-	-	8	mV	
Input voltage range (Vin)	Gain × 2.000	Vin	0.050 × AVcc	-	0.450 × AVcc	V	
	Gain × 2.500		0.047 × AVcc	-	0.360 × AVcc		
	Gain × 3.077		0.045 × AVcc	-	0.292 × AVcc		
	Gain × 3.636		0.042 × AVcc	-	0.247 × AVcc		
	Gain × 4.000		0.040 × AVcc	-	0.212 × AVcc		
	Gain × 4.444		0.036 × AVcc	-	0.191 × AVcc		
	Gain × 5.000		0.033 × AVcc	-	0.170 × AVcc		
	Gain × 5.714		0.031 × AVcc	-	0.148 × AVcc		
	Gain × 6.667		0.029 × AVcc	-	0.127 × AVcc		
	Gain × 10.000		0.025 × AVcc	-	0.08 × AVcc		
	Gain × 13.333		0.023 × AVcc	-	0.06 × AVcc		
Slew rate		SR	10	-	-	V/μs	
Gain error	Gain × 2.000	-	-	-	1	%	
	Gain × 2.500		-	-	1		
	Gain × 3.077		-	-	1		
	Gain × 3.636		-	-	1.5		
	Gain × 4.000		-	-	1.5		
	Gain × 4.444		-	-	2		
	Gain × 5.000		-	-	2		
	Gain × 5.714		-	-	2		
	Gain × 6.667		-	-	3		
	Gain × 10.000		-	-	4		
	Gain × 13.333		-	-	4		

Table 5.18 Comparator Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	Cin	-	-	6	pF	
REFH pin offset voltage	Voff	-	-	5	mV	
REFL pin offset voltage		-	-	5	mV	
REFH input voltage range	Vin	1.7	-	AVcc – 0.3	V	
REFL input voltage range		0.3	-	AVcc – 1.7	V	
REFH reply time	tCR	-	-	1	μs	
REFL reply time	tCF	-	-	1	μs	

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.