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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562taedff-v1

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range		
RX62T	R5F562TAADFH	R5F562TAADFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support- ed	-40 to +85°C (D version)		
	R5F562TAADFP	R5F562TAADFP#V3	PLQP0100KB-A								
	R5F562TAADFF	R5F562TAADFF#V3	PLQP0080JA-A								
	R5F562TAGDFF	R5F562TAGDFF#V3	PLQP0080JA-A								
	R5F562TAADFM	R5F562TAADFM#V3	PLQP0064KB-A								
	R5F562TAADFK	R5F562TAADFK#V3	PLQP0064GA-A								
	R5F562T7ADFH	R5F562T7ADFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes					
	R5F562T7ADFP	R5F562T7ADFP#V3	PLQP0100KB-A								
	R5F562T7ADFF	R5F562T7ADFF#V3	PLQP0080JA-A								
	R5F562T7GDFF	R5F562T7GDFF#V3	PLQP0080JA-A								
	R5F562T7ADFM	R5F562T7ADFM#V3	PLQP0064KB-A								
	R5F562T7ADFK	R5F562T7ADFK#V3	PLQP0064GA-A								
	R5F562T6ADFF	R5F562T6ADFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes						
	R5F562T6ADFM	R5F562T6ADFM#V3	PLQP0064KB-A								
	R5F562T6ADFK	R5F562T6ADFK#V3	PLQP0064GA-A								
	R5F562TABDFH	R5F562TABDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V				
	R5F562TABDFP	R5F562TABDFP#V3	PLQP0100KB-A								
	R5F562TABDFF	R5F562TABDFF#V3	PLQP0080JA-A								
	R5F562TABDFM	R5F562TABDFM#V3	PLQP0064KB-A								
	R5F562TABDFK	R5F562TABDFK#V3	PLQP0064GA-A								
	R5F562T7BDFH	R5F562T7BDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes					
	R5F562T7BDFP	R5F562T7BDFP#V3	PLQP0100KB-A								
	R5F562T7BDFF	R5F562T7BDFF#V3	PLQP0080JA-A								
	R5F562T7BDFM	R5F562T7BDFM#V3	PLQP0064KB-A								
	R5F562T7BDFK	R5F562T7BDFK#V3	PLQP0064GA-A	64 Kbytes	8 Kbytes						
	R5F562T6BDFF	R5F562T6BDFF#V3	PLQP0080JA-A								
	R5F562T6BDFM	R5F562T6BDFM#V3	PLQP0064KB-A								
	R5F562T6BDFK	R5F562T6BDFK#V3	PLQP0064GA-A								
	R5F562TADDFH	R5F562TADDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	4.0 to 5.5 V	Not Support- ed			
	R5F562TADDFP	R5F562TADDFP#V3	PLQP0100KB-A								
	R5F562TADDDFF	R5F562TADDDFF#V3	PLQP0080JA-A								
	R5F562TADDDFM	R5F562TADDDFM#V3	PLQP0064KB-A								
	R5F562TADDDFK	R5F562TADDDFK#V3	PLQP0064GA-A								
	R5F562T7DDFH	R5F562T7DDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes					
	R5F562T7DDFP	R5F562T7DDFP#V3	PLQP0100KB-A								
	R5F562T7DDFF	R5F562T7DDFF#V3	PLQP0080JA-A								
	R5F562T7DDFM	R5F562T7DDFM#V3	PLQP0064KB-A								
	R5F562T7DDFK	R5F562T7DDFK#V3	PLQP0064GA-A								
	R5F562T6DDFF	R5F562T6DDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes						
	R5F562T6DDFM	R5F562T6DDFM#V3	PLQP0064KB-A								
	R5F562T6DDFK	R5F562T6DDFK#V3	PLQP0064GA-A								
	R5F562TAEDFH	R5F562TAEDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	2.7 to 3.6 V				
	R5F562TAEDFP	R5F562TAEDFP#V3	PLQP0100KB-A								
	R5F562TAEDFF	R5F562TAEDFF#V3	PLQP0080JA-A								
	R5F562TAEDFM	R5F562TAEDFM#V3	PLQP0064KB-A								
R5F562TAEDFK	R5F562TAEDFK#V3	PLQP0064GA-A									

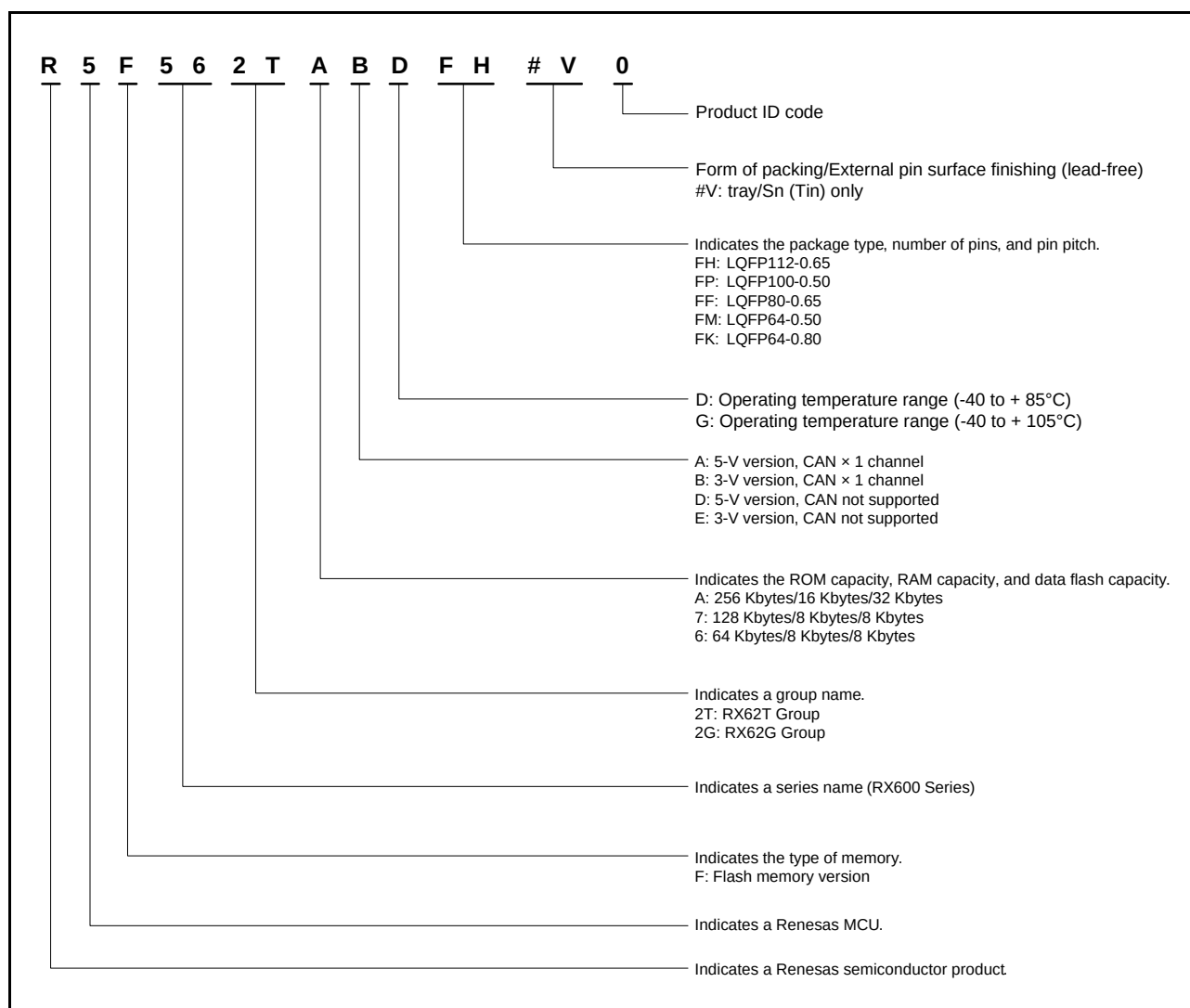


Figure 1.1 **How to Read the Product Part No.**

Table 4.1 List of I/O Registers (Address Order) (7 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7305h	ICU	Interrupt source priority register 05	IPR05	8	8	2 ICLK
0008 7306h	ICU	Interrupt source priority register 06	IPR06	8	8	2 ICLK
0008 7307h	ICU	Interrupt source priority register 07	IPR07	8	8	2 ICLK
0008 7314h	ICU	Interrupt source priority register 14	IPR14	8	8	2 ICLK
0008 7318h	ICU	Interrupt source priority register 18	IPR18	8	8	2 ICLK
0008 7320h	ICU	Interrupt source priority register 20	IPR20	8	8	2 ICLK
0008 7321h	ICU	Interrupt source priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt source priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt source priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt source priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt source priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt source priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt source priority register 27	IPR27	8	8	2 ICLK
0008 7340h	ICU	Interrupt source priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt source priority register 44	IPR44	8	8	2 ICLK
0008 7348h	ICU	Interrupt source priority register 48	IPR48	8	8	2 ICLK
0008 7349h	ICU	Interrupt source priority register 49	IPR49	8	8	2 ICLK
0008 7351h	ICU	Interrupt source priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt source priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt source priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt source priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt source priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt source priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt source priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt source priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt source priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt source priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt source priority register 5B	IPR5B	8	8	2 ICLK
0008 735Ch	ICU	Interrupt source priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt source priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt source priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt source priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt source priority register 60	IPR60	8	8	2 ICLK
0008 7367h	ICU	Interrupt source priority register 67	IPR67	8	8	2 ICLK
0008 7368h	ICU	Interrupt source priority register 68	IPR68	8	8	2 ICLK
0008 7369h	ICU	Interrupt source priority register 69	IPR69	8	8	2 ICLK
0008 736Ah	ICU	Interrupt source priority register 6A	IPR6A	8	8	2 ICLK
0008 736Bh	ICU	Interrupt source priority register 6B	IPR6B	8	8	2 ICLK
0008 736Ch	ICU	Interrupt source priority register 6C	IPR6C	8	8	2 ICLK
0008 736Dh	ICU	Interrupt source priority register 6D	IPR6D	8	8	2 ICLK
0008 736Eh	ICU	Interrupt source priority register 6E	IPR6E	8	8	2 ICLK
0008 736Fh	ICU	Interrupt source priority register 6F	IPR6F	8	8	2 ICLK
0008 7380h	ICU	Interrupt source priority register 80	IPR80	8	8	2 ICLK
0008 7381h	ICU	Interrupt source priority register 81	IPR81	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0009 041Ch	CAN0*2	Mask register 7	MKR7	32	8, 16, 32	2, 3 PCLK*3
0009 0420h	CAN0*2	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLK*3
0009 0424h	CAN0*2	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLK*3
0009 0428h	CAN0*2	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLK*3
0009 042Ch	CAN0*2	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLK*3
0009 0820h to 0009 083Fh	CAN0*2	Message control registers 0 to 31	MCTL0 to MCTL31	8	8	2, 3 PCLK*3
0009 0840h	CAN0*2	Control register	CTLR	16	8, 16	2, 3 PCLK*3
0009 0842h	CAN0*2	Status register	STR	16	8, 16	2, 3 PCLK*3
0009 0844h	CAN0*2	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLK*3
0009 0848h	CAN0*2	Receive FIFO control register	RFCR	8	8	2, 3 PCLK*3
0009 0849h	CAN0*2	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLK*3
0009 084Ah	CAN0*2	Transmit FIFO control register	TFCR	8	8	2, 3 PCLK*3
0009 084Bh	CAN0*2	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLK*3
0009 084Ch	CAN0*2	Error interrupt enable register	EIER	8	8	2, 3 PCLK*3
0009 084Dh	CAN0*2	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLK*3
0009 084Eh	CAN0*2	Receive error count register	RECR	8	8	2, 3 PCLK*3
0009 084Fh	CAN0*2	Transmit error count register	TECR	8	8	2, 3 PCLK*3
0009 0850h	CAN0*2	Error code store register	ECSR	8	8	2, 3 PCLK*3
0009 0851h	CAN0*2	Channel search support register	CSSR	8	8	2, 3 PCLK*3
0009 0852h	CAN0*2	Mailbox search status register	MSSR	8	8	2, 3 PCLK*3
0009 0853h	CAN0*2	Mailbox search mode register	MSMR	8	8	2, 3 PCLK*3
0009 0854h	CAN0*2	Time stamp register	TSR	16	8, 16	2, 3 PCLK*3
0009 0856h	CAN0*2	Acceptance filter support register	AFSR	16	8, 16	2, 3 PCLK*3
0009 0858h	CAN0*2	Test control register	TCR	8	8	2, 3 PCLK*3
0009 4001h	LIN0	LIN wake-up baud rate select register	LWBR	8	8	2, 3 PCLK*3
0009 4002h	LIN0	LIN baud rate prescaler 0 register	LBRP0	8	8, 16	2, 3 PCLK*3
0009 4003h	LIN0	LIN baud rate prescaler 1 register	LBRP1	8	8, 16	2, 3 PCLK*3
0009 4004h	LIN0	LIN self-test control register	LSTC	8	8	2, 3 PCLK*3
0009 4008h	LIN0	Mode register	L0MD	8	8, 16, 32	2, 3 PCLK*3
0009 4009h	LIN0	Break field setting register	L0BRK	8	8, 16, 32	2, 3 PCLK*3
0009 400Ah	LIN0	Space setting register	L0SPC	8	8, 16, 32	2, 3 PCLK*3
0009 400Bh	LIN0	Wake-up setting register	L0WUP	8	8, 16, 32	2, 3 PCLK*3
0009 400Ch	LIN0	Interrupt enable register	L0IE	8	8, 16	2, 3 PCLK*3
0009 400Dh	LIN0	Error detection enable register	L0EDE	8	8, 16	2, 3 PCLK*3
0009 400Eh	LIN0	Control register	L0C	8	8	2, 3 PCLK*3
0009 4010h	LIN0	Transmission control register	L0TC	8	8, 16, 32	2, 3 PCLK*3
0009 4011h	LIN0	Mode status register	L0MST	8	8, 16, 32	2, 3 PCLK*3
0009 4012h	LIN0	Status register	L0ST	8	8, 16, 32	2, 3 PCLK*3
0009 4013h	LIN0	Error status register	L0EST	8	8, 16, 32	2, 3 PCLK*3
0009 4014h	LIN0	Response field set register	L0RFC	8	8, 16	2, 3 PCLK*3
0009 4015h	LIN0	Buffer register	L0IDB	8	8, 16	2, 3 PCLK*3
0009 4016h	LIN0	Check sum buffer register	L0CBR	8	8	2, 3 PCLK*3
0009 4018h	LIN0	Data 1 buffer register	L0DB1	8	8, 16, 32	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (18 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 1390h	MTU1	Timer input capture control register	TICCR	8	8	5 ICLK
000C 1400h	MTU2	Timer control register	TCR	8	8, 16	5 ICLK
000C 1401h	MTU2	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1402h	MTU2	Timer I/O control register	TIOR	8	8	5 ICLK
000C 1404h	MTU2	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1405h	MTU2	Timer status register	TSR	8	8	5 ICLK
000C 1406h	MTU2	Timer counter	TCNT	16	16	5 ICLK
000C 1408h	MTU2	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 140Ah	MTU2	Timer general register B	TGRB	16	16	5 ICLK
000C 1A00h	MTU6	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1A01h	MTU7	Timer control register	TCR	8	8	5 ICLK
000C 1A02h	MTU6	Timer mode register 1	TMDR1	8	8, 16	5 ICLK
000C 1A03h	MTU7	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1A04h	MTU6	Timer I/O control register H	TIORH	8	8, 16, 32	5 ICLK
000C 1A05h	MTU6	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1A06h	MTU7	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1A07h	MTU7	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1A08h	MTU6	Timer interrupt enable register	TIER	8	8, 16	5 ICLK
000C 1A09h	MTU7	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 1A0Ah	MTU	Timer output master enable register B	TOERB	8	8	5 ICLK
000C 1A0Eh	MTU	Timer output control register 1B	TOCR1B	8	8, 16	5 ICLK
000C 1A0Fh	MTU	Timer output control register 2B	TOCR2B	8	8	5 ICLK
000C 1A10h	MTU6	Timer counter	TCNT	16	16, 32	5 ICLK
000C 1A12h	MTU7	Timer counter	TCNT	16	16	5 ICLK
000C 1A14h	MTU	Timer cycle data register B	TCDRB	16	16, 32	5 ICLK
000C 1A16h	MTU	Timer dead time data register B	TDDRB	16	16	5 ICLK
000C 1A18h	MTU6	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 1A1Ah	MTU6	Timer general register B	TGRB	16	16	5 ICLK
000C 1A1Ch	MTU7	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 1A1Eh	MTU7	Timer general register B	TGRB	16	16	5 ICLK
000C 1A20h	MTU	Timer subcounter B	TCNTSB	16	16, 32	5 ICLK
000C 1A22h	MTU	Timer cycle buffer register B	TCBRB	16	16	5 ICLK
000C 1A24h	MTU6	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1A26h	MTU6	Timer general register D	TGRD	16	16	5 ICLK
000C 1A28h	MTU7	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1A2Ah	MTU7	Timer general register D	TGRD	16	16	5 ICLK
000C 1A2Ch	MTU6	Timer status register	TSR	8	8, 16	5 ICLK
000C 1A2Dh	MTU7	Timer status register	TSR	8	8	5 ICLK
000C 1A30h	MTU	Timer interrupt skipping set register 1B	TITCR1B	8	8, 16	5 ICLK
000C 1A31h	MTU	Timer interrupt skipping counter 1B	TITCNT1B	8	8	5 ICLK
000C 1A32h	MTU	Timer buffer transfer set register B	TBTERB	8	8	5 ICLK
000C 1A34h	MTU	Timer dead time enable register B	TDERB	8	8	5 ICLK
000C 1A36h	MTU	Timer output level buffer register B	TOLBRB	8	8	5 ICLK
000C 1A38h	MTU6	Timer buffer operation transfer mode register	TBTM	8	8, 16	5 ICLK

Table 4.1 List of I/O Registers (Address Order) (22 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 21A0h	GPT1	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 21A4h	GPT1	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 21A6h	GPT1	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 21A8h	GPT1	A/D converter start request timing double-buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 21ACh	GPT1	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 21AEh	GPT1	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B0h	GPT1	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B4h	GPT1	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B6h	GPT1	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B8h	GPT1	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 21BAh	GPT1	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 21BCh	GPT1	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 21BEh	GPT1	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 21C0h	GPT1	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 21C2h	GPT1	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2200h	GPT2	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2202h	GPT2	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2204h	GPT2	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2206h	GPT2	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2208h	GPT2	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 220Ah	GPT2	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 220Ch	GPT2	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 220Eh	GPT2	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2210h	GPT2	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2212h	GPT2	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2214h	GPT2	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}
000C 2216h	GPT2	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2218h	GPT2	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 221Ah	GPT2	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 221Ch	GPT2	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 221Eh	GPT2	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2220h	GPT2	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2224h	GPT2	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2226h	GPT2	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2228h	GPT2	A/D converter start request timing double-buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.2 List of I/O Registers (Bit Order) (4 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IR044	—	—	—	—	—	—	—	IR
ICU	IR045	—	—	—	—	—	—	—	IR
ICU	IR046	—	—	—	—	—	—	—	IR
ICU	IR047	—	—	—	—	—	—	—	IR
ICU	IR056	—	—	—	—	—	—	—	IR
ICU	IR057	—	—	—	—	—	—	—	IR
ICU	IR058	—	—	—	—	—	—	—	IR
ICU	IR059	—	—	—	—	—	—	—	IR
ICU	IR060	—	—	—	—	—	—	—	IR
ICU	IR064	—	—	—	—	—	—	—	IR
ICU	IR065	—	—	—	—	—	—	—	IR
ICU	IR066	—	—	—	—	—	—	—	IR
ICU	IR067	—	—	—	—	—	—	—	IR
ICU	IR068	—	—	—	—	—	—	—	IR
ICU	IR069	—	—	—	—	—	—	—	IR
ICU	IR070	—	—	—	—	—	—	—	IR
ICU	IR071	—	—	—	—	—	—	—	IR
ICU	IR096	—	—	—	—	—	—	—	IR
ICU	IR098	—	—	—	—	—	—	—	IR
ICU	IR102	—	—	—	—	—	—	—	IR
ICU	IR103	—	—	—	—	—	—	—	IR
ICU	IR106	—	—	—	—	—	—	—	IR
ICU	IR114	—	—	—	—	—	—	—	IR
ICU	IR115	—	—	—	—	—	—	—	IR
ICU	IR116	—	—	—	—	—	—	—	IR
ICU	IR117	—	—	—	—	—	—	—	IR
ICU	IR118	—	—	—	—	—	—	—	IR
ICU	IR119	—	—	—	—	—	—	—	IR
ICU	IR120	—	—	—	—	—	—	—	IR
ICU	IR121	—	—	—	—	—	—	—	IR
ICU	IR122	—	—	—	—	—	—	—	IR
ICU	IR123	—	—	—	—	—	—	—	IR
ICU	IR124	—	—	—	—	—	—	—	IR
ICU	IR125	—	—	—	—	—	—	—	IR
ICU	IR126	—	—	—	—	—	—	—	IR
ICU	IR127	—	—	—	—	—	—	—	IR
ICU	IR128	—	—	—	—	—	—	—	IR
ICU	IR129	—	—	—	—	—	—	—	IR
ICU	IR130	—	—	—	—	—	—	—	IR
ICU	IR131	—	—	—	—	—	—	—	IR
ICU	IR132	—	—	—	—	—	—	—	IR
ICU	IR133	—	—	—	—	—	—	—	IR
ICU	IR134	—	—	—	—	—	—	—	IR
ICU	IR135	—	—	—	—	—	—	—	IR
ICU	IR136	—	—	—	—	—	—	—	IR
ICU	IR137	—	—	—	—	—	—	—	IR
ICU	IR138	—	—	—	—	—	—	—	IR
ICU	IR139	—	—	—	—	—	—	—	IR
ICU	IR140	—	—	—	—	—	—	—	IR
ICU	IR141	—	—	—	—	—	—	—	IR
ICU	IR142	—	—	—	—	—	—	—	IR
ICU	IR143	—	—	—	—	—	—	—	IR

Table 4.2 List of I/O Registers (Bit Order) (7 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	DTCER180	—	—	—	—	—	—	—	DTCE
ICU	DTCER181	—	—	—	—	—	—	—	DTCE
ICU	DTCER182	—	—	—	—	—	—	—	DTCE
ICU	DTCER183	—	—	—	—	—	—	—	DTCE
ICU	DTCER184	—	—	—	—	—	—	—	DTCE
ICU	DTCER186	—	—	—	—	—	—	—	DTCE
ICU	DTCER187	—	—	—	—	—	—	—	DTCE
ICU	DTCER188	—	—	—	—	—	—	—	DTCE
ICU	DTCER189	—	—	—	—	—	—	—	DTCE
ICU	DTCER190	—	—	—	—	—	—	—	DTCE
ICU	DTCER192	—	—	—	—	—	—	—	DTCE
ICU	DTCER193	—	—	—	—	—	—	—	DTCE
ICU	DTCER194	—	—	—	—	—	—	—	DTCE
ICU	DTCER195	—	—	—	—	—	—	—	DTCE
ICU	DTCER196	—	—	—	—	—	—	—	DTCE
ICU	DTCER215	—	—	—	—	—	—	—	DTCE
ICU	DTCER216	—	—	—	—	—	—	—	DTCE
ICU	DTCER219	—	—	—	—	—	—	—	DTCE
ICU	DTCER220	—	—	—	—	—	—	—	DTCE
ICU	DTCER223	—	—	—	—	—	—	—	DTCE
ICU	DTCER224	—	—	—	—	—	—	—	DTCE
ICU	DTCER247	—	—	—	—	—	—	—	DTCE
ICU	DTCER248	—	—	—	—	—	—	—	DTCE
ICU	DTCER254	—	—	—	—	—	—	—	DTCE
ICU	IER02	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER03	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER05	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER07	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER08	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0C	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0D	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0E	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0F	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER10	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER11	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER12	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER13	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER15	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER16	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER17	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER18	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1A	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1B	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1C	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1E	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1F	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	SWINTR	—	—	—	—	—	—	—	SWINT
ICU	FIR	FIEN	—	—	—	—	—	—	—
FVCT[7:0]									
ICU	IPR00	—	—	—	—	IPR[3:0]			
ICU	IPR01	—	—	—	—	IPR[3:0]			
ICU	IPR02	—	—	—	—	IPR[3:0]			

Table 4.2 List of I/O Registers (Bit Order) (16 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
POE	POECR2	—	—	—	—	—	MTU3BDZE	MTU4ACZE	MTU4BDZE
		—	—	—	—	—	MTU6BDZE	MTU7ACZE	MTU7BDZE
POE	POECR3	—	—	—	—	—	—	GPT3ABZE	GPT2ABZE
		—	—	—	—	—	—	GPT1ABZE	GPT0ABZE
POE	POECR4	—	—	IC5ADDMT67 ZE	IC4ADDMT67 ZE	IC3ADDMT67 ZE	—	IC1ADDMT67 ZE	CMADDMT67 ZE
		—	—	IC5ADDMT34 ZE	IC4ADDMT34 ZE	IC3ADDMT34 ZE	IC2ADDMT34 ZE	—	CMADDMT34 ZE
POE	POECR5	—	—	—	—	—	—	—	—
		—	—	IC5ADDMT0Z E	IC4ADDMT0Z E	—	IC2ADDMT0Z E	IC1ADDMT0Z E	CMADDMT0Z E
POE	POECR6	—	—	—	IC4ADDGPT2 3ZE	IC3ADDGPT2 3ZE	IC2ADDGPT2 3ZE	IC1ADDGPT2 3ZE	CMADDGPT2 3ZE
		—	—	IC5ADDGPT0 1ZE	—	IC3ADDGPT0 1ZE	IC2ADDGPT0 1ZE	IC1ADDGPT0 1ZE	CMADDGPT0 1ZE
POE	ICSR4	—	—	—	POE10F	—	—	POE10E	PIE4
		—	—	—	—	—	—	POE10M[1:0]	
POE	ALR1	—	—	—	—	—	—	—	—
		OLSEN	—	OLSG2B	OLSG2A	OLSG1B	OLSG1A	OLSG0B	OLSG0A
POE	ICSR5	—	—	—	POE11F	—	—	POE11E	PIE5
		—	—	—	—	—	—	POE11M[1:0]	
CAN0*3	MB.ID	IDE	RTR	—	—	—	SID[10:0]		
		SID[10:0]				EID[17:0]			
		—				EID[17:0]			
		—				EID[17:0]			
	MB.DLC	—	—	—	—	—	—	—	—
		—	—	—	—	DLC[3:0]			
	MB.DATA 0 to 7								
CAN0*3	MKR0	—				TSH[7:0]			
		—				TSL[7:0]			
—		—	—	SID[10:0]			EID[17 0]		
SID[10:0]				EID[17:0]					
CAN0*3	MKR1	—	—	—	SID[10:0]			EID[17:0]	
		SID[10:0]				EID[17:0]			
		—				EID[17:0]			
		—				EID[17:0]			
CAN0*3	MKR2	—	—	—	SID[10:0]			EID[17 0]	
		SID[10:0]				EID[17:0]			
		—				EID[17:0]			
		—				EID[17:0]			
CAN0*3	MKR3	—	—	—	SID[10:0]			EID[17 0]	
		SID[10:0]				EID[17:0]			
		—				EID[17:0]			
		—				EID[17:0]			
CAN0*3	MKR4	—	—	—	SID[10:0]			EID[17 0]	
		SID[10:0]				EID[17:0]			
		—				EID[17:0]			
		—				EID[17:0]			

Table 4.2 List of I/O Registers (Bit Order) (26 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT1	GTADTBRB								
GPT1	GTADTDBRB								
GPT1	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
		NFS[3:0]				NVB	NVA	NEB	NEA
GPT1	GTDTCCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT1	GTDVU								
GPT1	GTDVD								
GPT1	GTDBU								
GPT1	GTDBD								
GPT1	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT1	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT2	GTIOR	OBHLD	OBDFLT	GTIOB[5:0]					
		OAHL	OADFLT	GTIOA[5:0]					
GPT2	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA
GPT2	GTCR	—	—	CCLR[1:0]		—	—	TPCS[1:0]	
		—	—	—	—	—	—	MD[2:0]	
GPT2	GTBER	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]	
		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
GPT2	GTUDC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	UDF	UD
GPT2	GTITC	—	ADTBL	—	ADTAL	—	—	IVTT[2:0]	
		IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
GPT2	GTST	TUCF	—	—	—	DTEF	—	ITCNT[2:0]	
		TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
GPT2	GT CNT								
GPT2	GTCCRA								
GPT2	GTCCRB								
GPT2	GTCCRC								
GPT2	GTCCRD								
GPT2	GTCCRE								
GPT2	GTCCRF								
GPT2	GTPR								

Table 4.2 List of I/O Registers (Bit Order) (28 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT3	GTCCRB								
GPT3	GTCCRC								
GPT3	GTCCRD								
GPT3	GTCCRE								
GPT3	GTCCRF								
GPT3	GTPR								
GPT3	GTPBR								
GPT3	GTPDBR								
GPT3	GTADTRA								
GPT3	GTADTBRA								
GPT3	GTADTDBRA								
GPT3	GTADTRB								
GPT3	GTADTBRB								
GPT3	GTADTDBRB								
GPT3	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
				NFS[3:0]		NVB	NVA	NEB	NEA
GPT3	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT3	GTDVU								
GPT3	GTDVD								
GPT3	GTDBU								
GPT3	GTDBD	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT3	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT3	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT0	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT1	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		VCC PLLVCC	-0.3 to +6.5	V
Input voltage (except for ports 4 to 6)		V _{IN}	-0.3 to VCC+0.3	V
Input voltage (port 4)		V _{IN}	-0.3 to AVCC0+0.3	V
Input voltage (ports 5 and 6)		V _{IN}	-0.3 to AVCC+0.3	V
Analog power supply voltage		AVCC0, AVCC* ¹	-0.3 to +6.5	V
Reference power supply voltage		VREFH0* ¹	-0.3 to AVCC0+0.3	V
		VREF* ¹	-0.3 to AVCC+0.3	
Analog input voltage (port 4)		V _{AN}	-0.3 to AVCC0+0.3	V
Analog input voltage (ports 5 and 6)		V _{AN}	-0.3 to AVCC+0.3	V
Operating temperature	D version	T _{opr}	-40 to +85	°C
	G version	T _{opr}	-40 to +105	°C
Storage temperature		T _{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open circuit even if the A/D converter is not to be used.

- When the 12-bit converter is not in use:
Connect the AVCC0 pin to AVCC (or VCC for a 64-pin product), the VREFH0 pin to VREF (or AVCC or VCC for an 80- or 64-pin product, respectively), and the AVSS0 and VREFL0 pins to VSS.
- When the 10-bit converter is not in use:
Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0.
- When neither the 10- nor the 12-bit converter is in use:
Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS.

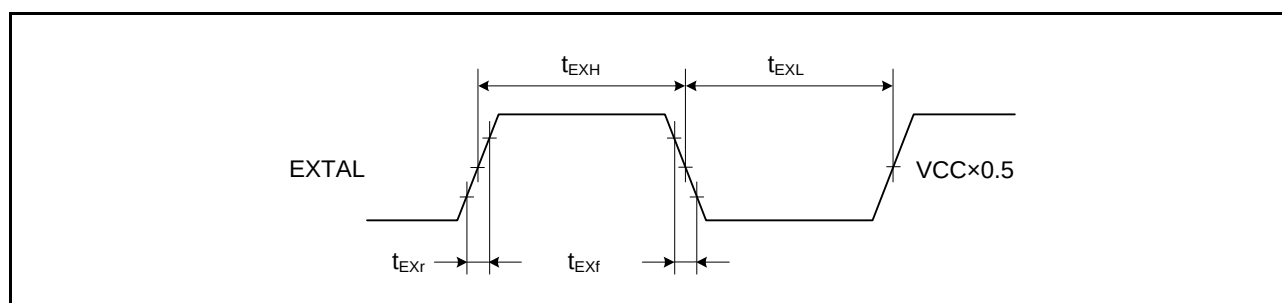


Figure 5.4 EXTAL External Input Clock Timing

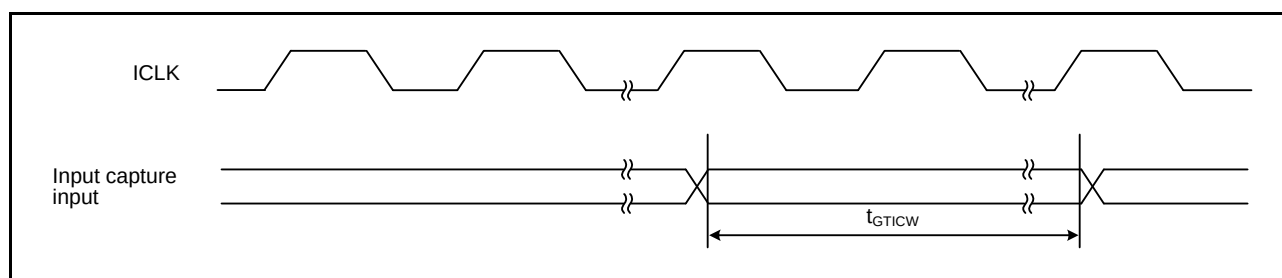


Figure 5.18 GPT Input/Output Timing

Table 5.13 Timing of On-Chip Peripheral Modules (5)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
POE3	POE# input pulse width	t _{POEW}	1.5	-	t _{Pcyc}	Figure 5.19

Note: • t_{Pcyc}: PCLK cycle

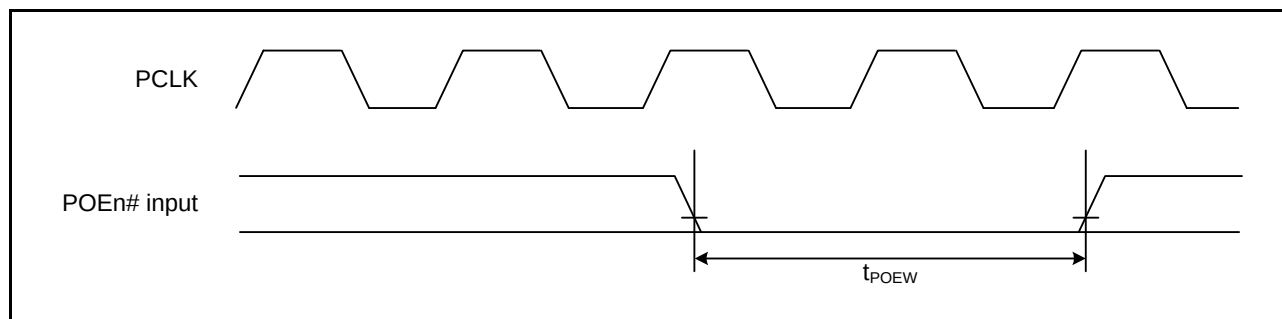


Figure 5.19 POE3# Clock Timing

5.3.4 Timing of PWM Delay Generation Circuit

Table 5.14 Timing of the PWM Delay Generation Circuit

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS = VREL0 = 0 V

AVCC = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	ICLK = 100 MHz
DNL *1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

5.5 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Table 5.19 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

$T_a = T_{opr}$. T_a is the same under conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	2.48	2.60	2.72	V	Figure 5.20
	Voltage detection circuit (LVD)	V _{det1}	2.68	2.80	2.92		Figure 5.21
		V _{det2}	2.98	3.10	3.22		Figure 5.22
Internal reset time		t _{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time ^{*1}		t _{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		t _{det}	-	-	200	us	

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

$$T_a = T_{opr}$$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	3.70	3.90	4.10	V	Figure 5.20
	Voltage detection circuit (LVD)	V _{det1}	3.95	4.15	4.35		Figure 5.21
		V _{det2}	4.40	4.60	4.80		Figure 5.22
Internal reset time		t _{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time*1		t _{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		t _{det}	-	-	200	us	

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for the POR/ LVD.

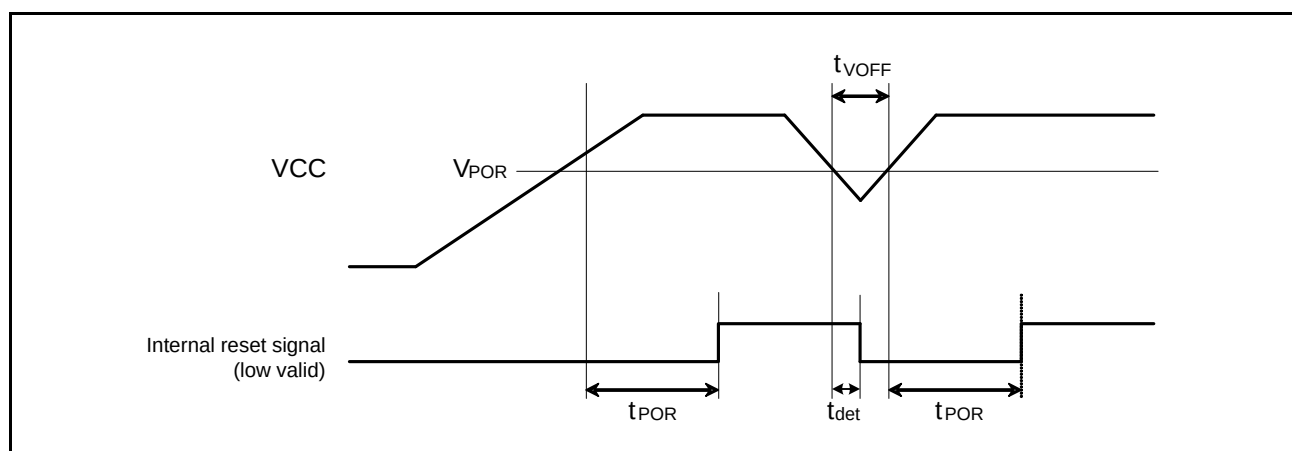


Figure 5.20 Power-on Reset Timing

5.6 Oscillation Stop Detection Timing

Table 5.20 Oscillation Stop Detection Circuit Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t _{dr}	-	-	1.0	ms	Figure 5.23
Internal oscillation frequency when oscillation stop is detected	f _{MAIN}	0.5	-	7.0	MHz	

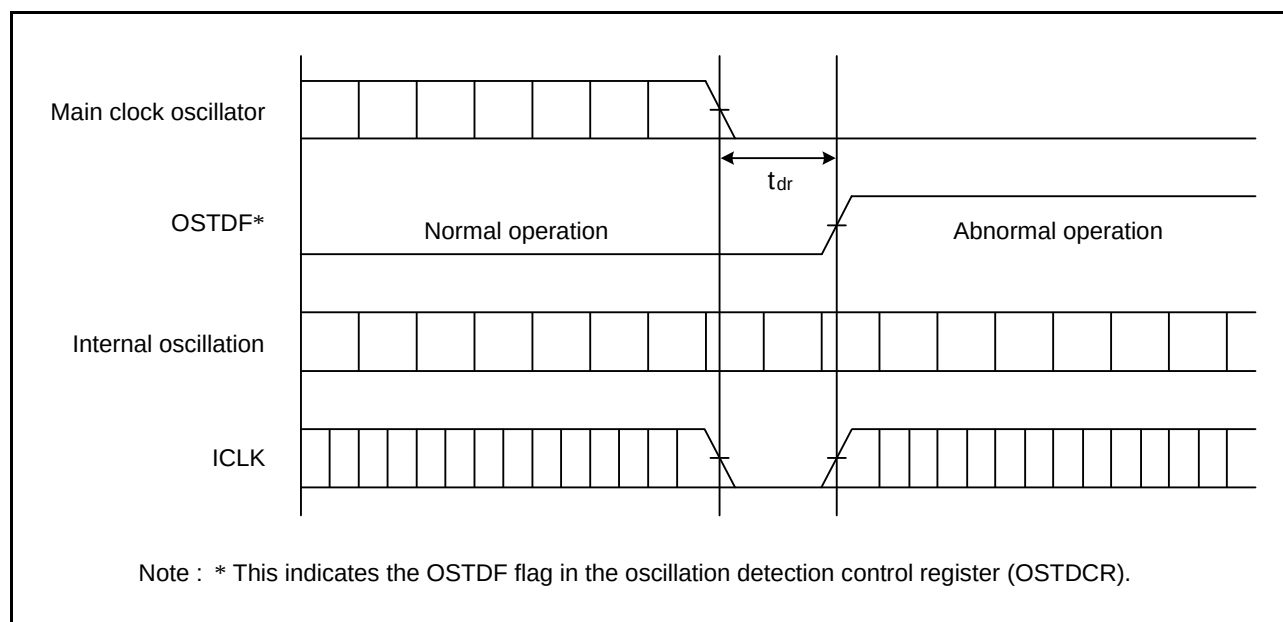


Figure 5.23 Oscillation Stop Detection Timing

5.8 Data Flash (Flash Memory for Data Storage) Characteristics

Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle* ¹	N _{DPEC}	30000	—	—	Times	
Data hold time	t _{DDRP}	30* ²	—	—	Year	Ta = +85C°

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	—	0.4	2	ms	PCLK = 50 MHz
	128 bytes	t _{DP128}	—	1	5	ms	
Erase time	2 Kbytes	t _{DE2K}	—	70	250	ms	PCLK = 50 MHz
Blank check time	8 bytes	t _{DBC8}	—	—	30	μs	PCLK = 50 MHz
	2 Kbytes	t _{DBC2K}	—	—	0.7	ms	
Suspend delay time during writing		t _{DSPD}	—	—	120	μs	Figure 5.24 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t _{DSESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t _{DSESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t _{DSEED}	—	—	1.7	ms	

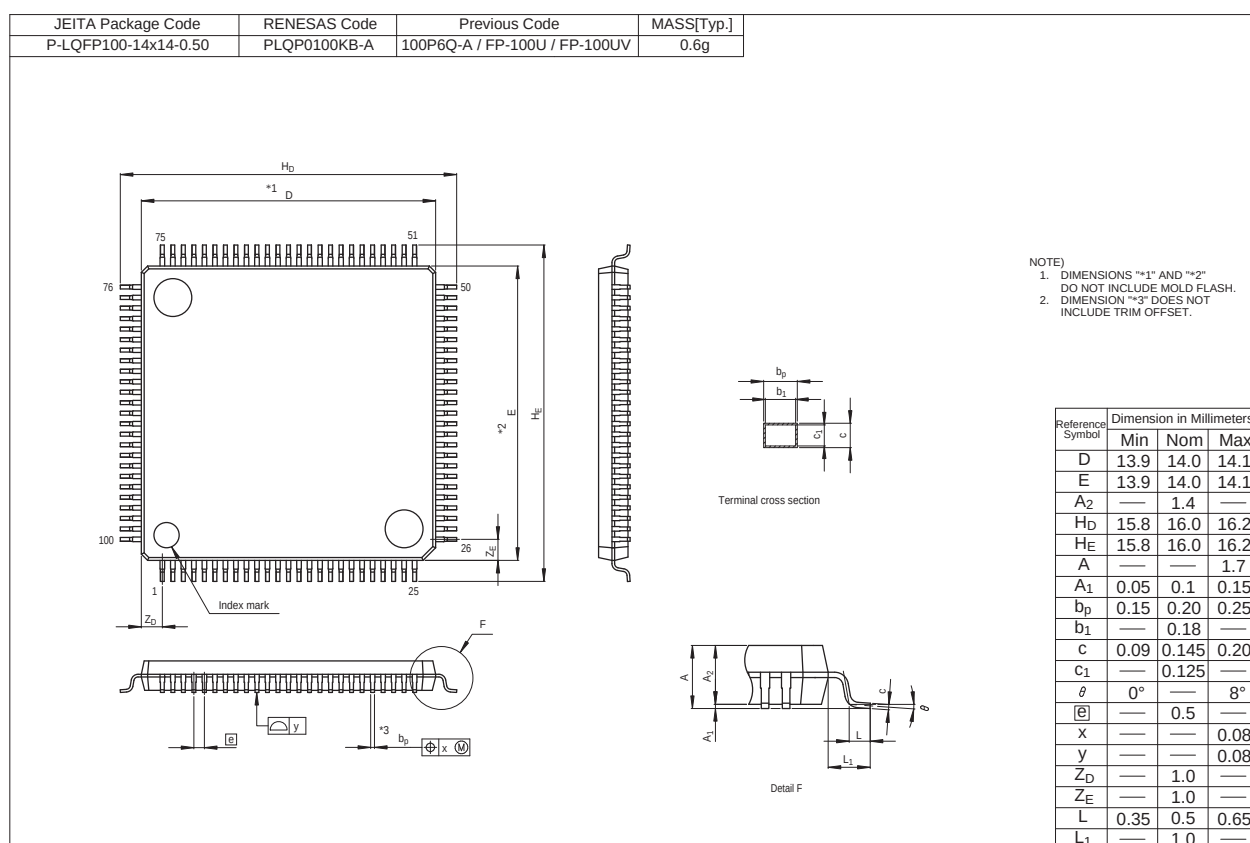


Figure B 100-Pin LQFP (PLQP0100KB-A) Package Dimensions

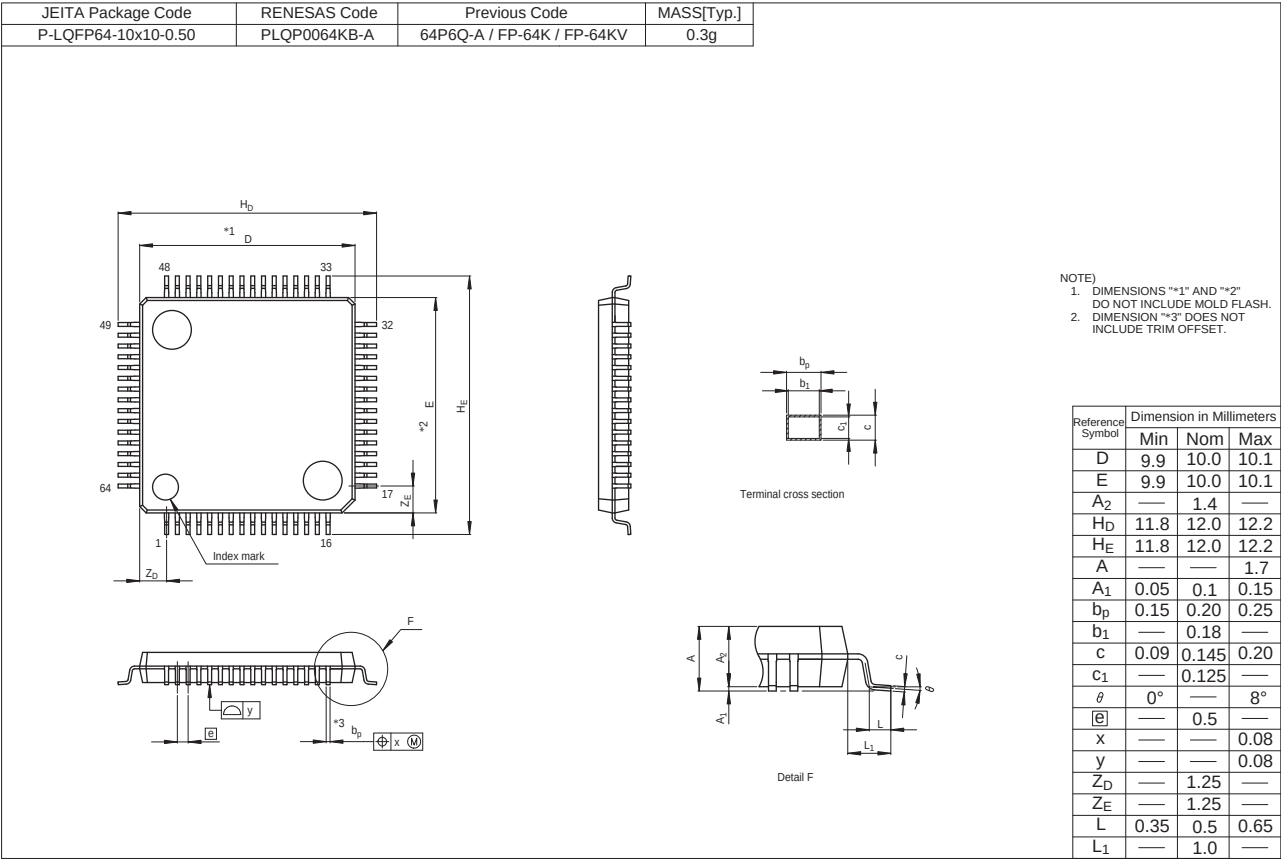


Figure D 64-Pin LQFP (PLQP0064KB-A) Package Dimensions

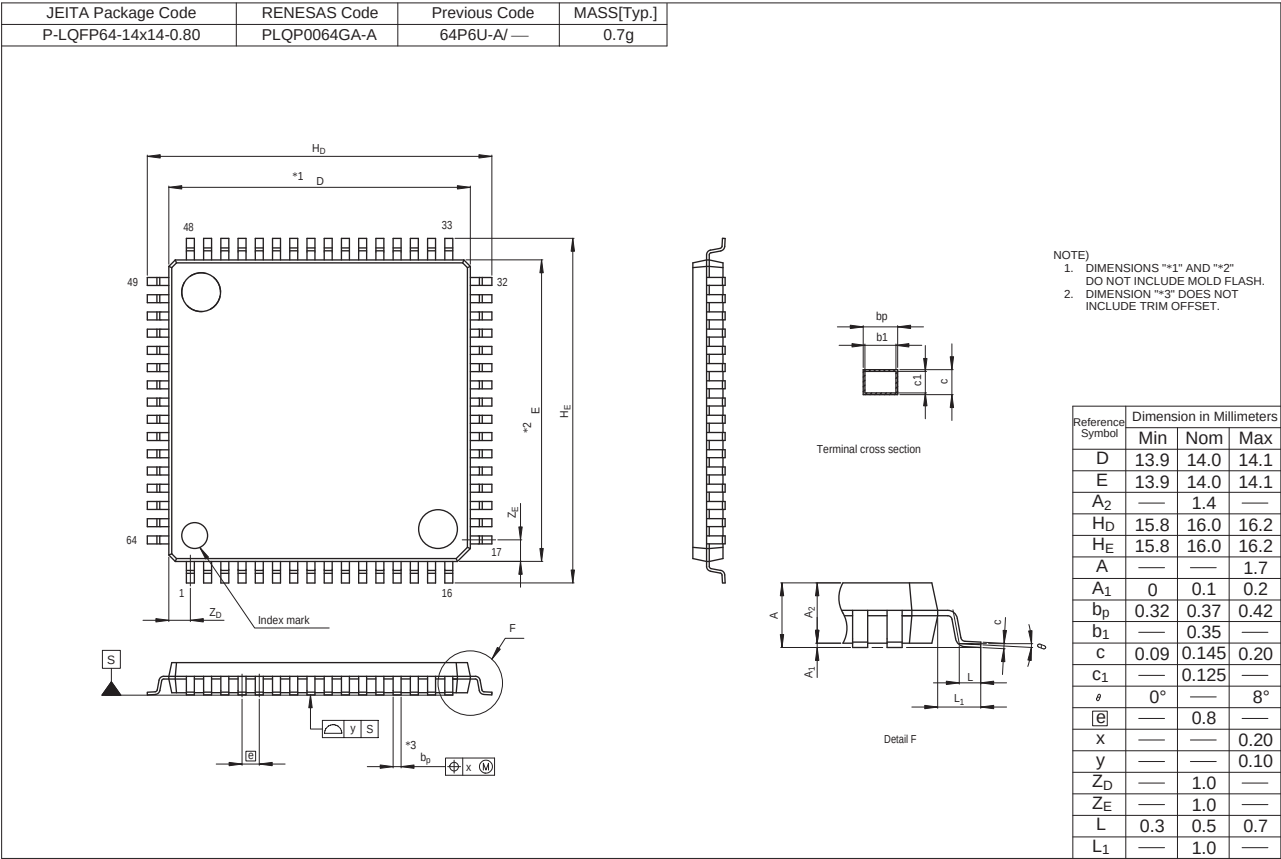


Figure E 64-Pin LQFP (PLQP0064GA-A) Package Dimensions