Renesas Electronics America Inc - R5F562TAEDFH#V3 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	61
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562taedfh-v3

Table 1.1 Outline of Specifications (2 / 5)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICU)	• Peripheral function interrupts: 101 sources • External interrupts: 9 (NMI and IRQ0 to IRQ7 pins) • Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt) • 16 levels specifiable for the order of priority
Data transfer	Data transfer controller (DTC)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	I/O port pins for devices in the 112-pin LQFP/100-pin LQFP/ 80-pin LQFP (R5F562TxGDFF)/80-pin LQFP (except R5F562TxGDFF)/64-pin LQFP • I/O: 61/55/44/44/37 • Input only: 21/21/13/13/9 • Open-drain outputs: 2/2/2/2/2 (I^2C bus interface pins) • Large-current outputs: 12/12/12/6/6(0) (MTU3 and GPT pins) The 5-V version of the 64-pin product does not have large-current outputs. • Reading out the states of pins is always possible.
Timers	Multi-function timer pulse unit 3 (MTU3)	• 16 bits x 8 channels • Up to 24 pulse inputs/outputs and three pulse inputs • Select from among six to eight counter-input clock signals for each channel (ICLK/1, ICLK/4, ICLK/16, ICLK/64, ICLK/256, ICLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • 24 output compare or input capture registers • Counter clearing (clearing is synchronizable with compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Input to and output from all registers in synchronization with counter operation • Buffered operation • Cascade-connected operation • 38 kinds of interrupt source • Automatic transfer of register data • Pulse output modes Toggled, PWM, complementary PWM, and reset synchronous PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins 5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11 Initiation on detection of short-circuited outputs (detection of simultaneous switching of large-current pins to the active level) Initiation by comparator-detection of analog level input to the 12-bit A/D converter Initiation by oscillation-stoppage detection Initiation by software • Selection of which output pins should be placed in the high-impedance state at the time of each POE input or comparator detection

Table 1.1 Outline of Specifications (4 / 5)

Classification	Module/Function	Description
Communications	CAN module (CAN) (as an optional function)	• 1 channel • 32 mailboxes
	Serial peripheral interface (RSPI)	• 1 unit • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure • Double buffers for both transmission and reception
	LIN module (LIN)	• 1 channel (LIN master) • Supports revisions 1.3, 2.0, and 2.1 of the LIN protocol
A/D converter	12-bit A/D converter (S12ADA)	• 12 bits (2 units x 4 channels) • 12-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC0 = 3.0 to 3.6 V • Two basic operating modes Single mode and scan mode • Scan mode One-cycle scan mode Continuous scan mode 2-channel scan mode (Input ports of the A/D unit are divided into two groups in this mode, and the activation sources are separately selectable for each group.) • Sample-and-hold function A common sample-and-hold circuit for both units is included. Additionally, sample-and-hold circuit for each unit is included. (three channels per unit) • A/D-conversion register settings for each input pin. • Two registers for the result of conversion are provided for a single analog input pin of each unit (AN000 and AN100). • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8- or 10-bit precision output Right-shifting of the results of conversion for output by two or four bits is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0). • Amplification of input signals by a programmable gain amplifier (three channels per unit) Amplification rate: 2.0-, 2.5-, 3.077-, 3.636-, 4.0-, 4.444-, 5.0-, 5.714-, 6.667-, 10.0-, or 13.333-times amplification (a total of 11 steps) • Window comparators (three channels per unit)

Table 1.1 Outline of Specifications (5 / 5)

Classification	Module/Function	Description
A/D converter	10-bit A/D converter (ADA)	• 10 bits (1 unit x 12 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V • Two basic operating modes Single mode and scan mode • Scan mode One-cycle scan mode Continuous scan mode • Sample-and-hold function A common sample-and-hold circuit for both units is included. • A/D-conversion register settings for each input pin • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8-bit precision output Right-shifting the results of conversion for output by two bits is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF).
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Operating frequency		ICLK: 8 to 100 MHz PCLK: 8 to 50 MHz
Power supply voltage		• 3-V version VCC = PLLVCC = 2.7 to 3.6V AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 VREF = 3.0 to AVCC, or 4.0 to AVCC • 5-V version VCC = PLLVCC = 4.0 to 5.5V AVCC0 = AVCC = 4.0 to 5.5V VREFH0 = 4.0 to AVCC0 VREF = 4.0 to AVCC
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Packages		112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch) 100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch) 80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch) 64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch) 64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
77		P60	AN0					
78		P55	AN11					
79		P54	AN10					
80		P53	AN9					
81		P52	AN8					
82		P51	AN7					
83		P50	AN6					
84		P47	AN103/ CVREFH					
85		P46	AN102					
86		P45	AN101					
87		P44	AN100					
88		P43	AN003/ CVREFL					
89		P42	AN002					
90		P41	AN001					
91		P40	AN000					
92	AVCC0							
93	VREFH0							
94	VREFL0							
95	AVSS0							
96		P82		MTIC5U	SCK2-B			
97		P81		MTIC5V	TXD2-B			
98		P80		MTIC5W	RXD2-B			
99		P11		MTCLKC-B		IRQ1-A		
100		P10		MTCLKD-B		IRQ0-A		

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
1	EMLE							
2	VSS							
3	MDE							
4	VCL							
5	MD1							
6	MD0							
7		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
8		PE3		MTCLKD-C		IRQ2-A	POE11#	
9	RES#							
10	XTAL							
11	VSS							
12	EXTAL							
13	VCC							
14		PE2				NMI	POE10#-A	
15		PE0			CRX-C			
16		PD7		GTIOC0A-B	CTX-C			TRST#
17		PD6		GTIOC0B-B				TMS
18		PD5		GTIOC1A-B	RXD1			TDI
19		PD4		GTIOC1B-B	SCK1			TCK
20		PD3		GTIOC2A-B	TXD1			TDO
21		PB7			SCK2-A			
22		PB6			CRX-A/ RXD2-A			
23		PB5			CTX-A/ TXD2-A			
24	PLLVCC							
25		PB4		GTETRG		IRQ3	POE8#	
26	PLLVSS							
27		PB3		MTIOC0A-A	SCK0			
28		PB2		MTIOC0B-A	TXD0/SDA			
29		PB1		MTIOC0C	RXD0/SCL			
30		PB0		MTIOC0D	MOSI-B			
31		PA3		MTIOC2A	SSL0-B			
32		PA2		MTIOC2B	SSL1-B			
33	VCC							
34		P96				IRQ4	POE4#	
35	VSS							
36		P95		MTIOC6B				
37		P94		MTIOC7A				
38		P93		MTIOC7B				
39		P92		MTIOC6D				
40		P91		MTIOC7C				
41		P76		MTIOC4D/ GTIOC2B-A				

Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No. (64-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debuggi ng
40		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
41		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
42	VCC							
43		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
44	VSS							
45		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
46		P24			RSPCK-A			
47		P23			CTX-B/ LTX/ MOSI-A			
48		P22			CRX-B/ LRX/ MISO-A			
49		P47	AN103/ CVREFH					
50		P46	AN102					
51		P45	AN101					
52		P44	AN100					
53		P43	AN003/ CVREFL					
54		P42	AN002					
55		P41	AN001					
56		P40	AN000					
57	AVCC0							
58	VREFH0							
59	VREFL0							
60	AVSS0							
61		P11		MTCLKC-B		IRQ1-A		
62		P10		MTCLKD-B		IRQ0-A		
63		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
64		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			

1.5 Pin Functions

Table 1.9 lists the pin functions.

Table 1.9 Pin Functions (1 / 4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	PLLVCC	Input	Power supply pin for the PLL circuit. Connect it to the system power supply.
	PLLVSS	Input	Ground pin for the PLL circuit.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
Operating mode control	MD0 MD1 MDE	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
On-chip emulator	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data. Not included in the 80-/64-pin versions.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid. Not included in the 80-/64-pin versions.
	TRDATA0 to TRDATA3	Output	These pins output the trace information. Not included in the 80-/64-pin versions.
Interrupt (ICU)	NMI	Input	Non-maskable interrupt request signal.
	IRQ0-A/IRQ0-B/IRQ0-C IRQ1-A/IRQ1-B/IRQ1-C IRQ2-A/IRQ2-B IRQ3 to IRQ7	Input	Interrupt request signals. The IRQ0-C/IRQ1-C/IRQ2-B pin is not included in the 100-pin version. The IRQ0-B/IRQ0-C/IRQ1-C/IRQ2-B pin is not included in the 80-pin version. The IRQ0-B/IRQ0-C/IRQ1-B/IRQ1-/IRQ2-A/IRQ2-B/IRQ4/IRQ6/IRQ7 pin is not included in the 64-pin version.

Table 1.9 Pin Functions (2 / 4)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3 (MTU3)	MTIOC0A-A/MTIOC0A-B MTIOC0B-A/MTIOC0B-B MTIOC0C, MTIOC0D	I/O	The MTU0.TGRA to MTU0.TGRD input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The MTU1.TGRA and MTU1.TGRB input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The MTU2.TGRA and MTU2.TGRB input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The MTU3.TGRA and MTU3.TGRD input capture input/output compare output/PWM output pins. Pins MTIOC3B and MTIOC3D can be used for large-current output.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The MTU4.TGRA and MTU4.TGRD input capture input/output compare output/PWM output pins. These pins can be used for large-current output.
	MTIC5U, MTIC5V, MTIC5W	Input	The MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW input capture input/dead time compensation input pins. Not included in the 80-/64-pin versions.
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The MTU6.TGRA to MTU6.TGRD input capture input/output compare output/PWM output pins. Pins MTIOC6B and MTIOC6D can be used for large-current output. The MTIOC6A/MTIOC6C pin is not included in the 80-pin version. The MTIOC6A/MTIOC6B/MTIOC6C pin is not included in the 64-pin version.
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The MTU7.TGRA to MTU7.TGRD input capture input/output compare output/PWM output pins. These pins can be used for large-current output. The MTIOC7D pin is not included in the 80-/64-pin versions.
	MTCLKA-A/MTCLKA-B MTCLKB-A/MTCLKB-B MTCLKC-A/MTCLKC-B/ MTCLKC-C MTCLKD-A/MTCLKD-B/ MTCLKD-C	Input	Input pins for external clock signals. The MTCLKA-B/MTCLKB-B/MTCLKC-C/MTCLKD-C pin is not included in the 64-pin version.
General PWM timer (GPT)	GTIOC0A-A/GTIOC0A-B GTIOC0B-A/GTIOC0B-B	I/O	The GPT0.GTCCRA and GPT0.GTCCRB CCRB input capture input/output compare output/PWM output pins. Pins GTIOC0A-A and GTIOC0B-A can be used for large-current output.
	GTIOC1A-A/GTIOC1A-B GTIOC1B-A/GTIOC1B-B	I/O	The GPT1.GTCCRA and GPT1.GTCCRB input capture input/output compare output/PWM output pins. Pins GTIOC1A-A and GTIOC1B-A can be used for large-current output.
	GTIOC2A-A/GTIOC2A-B GTIOC2B-A/GTIOC2B-B	I/O	The GPT2.GTCCRA and GPT2.GTCCRB input capture input/output compare output/PWM output pins. Pins GTIOC2A-A and GTIOC2B-A can be used for large-current output. The GTIOC2B-B pin is not included in the 80-pin version.
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTCCRA and GPT3.GTCCRB input capture input/output compare output/PWM output pins. Not included in the 80-/64-pin versions.
	GTETRG	Input	External trigger input pin for the GPT
Port output enable 3 (POE3)	POE0#, POE4#, POE8# POE10#-A/POE10#-B POE11#	Input	Input pins for request signals to place the MTU3 and GPT large-current pins in the high impedance state. The POE4#/POE10#-B/POE11# pin is not included in the 64-pin version.
Watchdog timer (WDT)	WDTOVF#	Output	Output pin for the counter-overflow signal in watchdog-timer mode. Not included in the 100-/80-/64-pin versions.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	16	16	3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region 0 start page-number register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region 0 end page-number register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region 1 start page-number register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region 1 end page-number register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region 2 start page-number register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region 2 end page-number register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region 3 start page-number register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region 3 end page-number register	REPAGE3	32	32	1 ICLK
0008 6420h	MPU	Region 4 start page-number register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region 4 end page-number register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region 5 start page-number register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region 5 end page-number register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region 6 start page-number register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region 6 end page-number register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region 7 start page-number register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region 7 end page-number register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background access control register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region search address register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region search operation register	MPOPS	16	16	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (12 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 90A4h	S12AD1	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 90A6h	S12AD1	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 90B0h	S12AD1	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 90E0h	S12AD1	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 C001h	PORT1	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C002h	PORT2	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C003h	PORT3	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C007h	PORT7	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C008h	PORT8	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C009h	PORT9	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Ah	PORTA	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Bh	PORTB	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Dh	PORTD	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Eh	PORTE	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C010h	PORTG	Data direction register	DDR*1	8	8	2, 3 PCLK*3
0008 C021h	PORT1	Data register	DR	8	8	2, 3 PCLK*3
0008 C022h	PORT2	Data register	DR	8	8	2, 3 PCLK*3
0008 C023h	PORT3	Data register	DR	8	8	2, 3 PCLK*3
0008 C027h	PORT7	Data register	DR	8	8	2, 3 PCLK*3
0008 C028h	PORT8	Data register	DR	8	8	2, 3 PCLK*3
0008 C029h	PORT9	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Ah	PORTA	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Bh	PORTB	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Dh	PORTD	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Eh	PORTE	Data register	DR	8	8	2, 3 PCLK*3
0008 C030h	PORTG	Data register	DR*1	8	8	2, 3 PCLK*3
0008 C041h	PORT1	Data register	PORT	8	8	2, 3 PCLK*3
0008 C042h	PORT2	Data register	PORT	8	8	2, 3 PCLK*3
0008 C043h	PORT3	Data register	PORT	8	8	2, 3 PCLK*3
0008 C044h	PORT4	Data register	PORT	8	8	2, 3 PCLK*3
0008 C045h	PORT5	Data register	PORT	8	8	2, 3 PCLK*3
0008 C046h	PORT6	Data register	PORT	8	8	2, 3 PCLK*3
0008 C047h	PORT7	Data register	PORT	8	8	2, 3 PCLK*3
0008 C048h	PORT8	Data register	PORT	8	8	2, 3 PCLK*3
0008 C049h	PORT9	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Ah	PORTA	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Bh	PORTB	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Dh	PORTD	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Eh	PORTE	Data register	PORT	8	8	2, 3 PCLK*3
0008 C050h	PORTG	Port register	PORT*1	8	8	2, 3 PCLK*3
0008 C061h	PORT1	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C062h	PORT2	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C063h	PORT3	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C064h	PORT4	Input buffer control register	ICR	8	8	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (13 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C065h	PORT5	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C066h	PORT6	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C067h	PORT7	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C068h	PORT8	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C069h	PORT9	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Ah	PORTA	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Bh	PORTB	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Dh	PORTD	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Eh	PORTE	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C070h	PORTG	Input buffer control register	ICR*1	8	8	2, 3 PCLK*3
0008 C108h	IOPORT	Port function register 8	PF8IRQ	8	8	2, 3 PCLK*3
0008 C109h	IOPORT	Port function register 9	PF9IRQ	8	8	2, 3 PCLK*3
0008 C10Ah	IOPORT	Port function register A	PFAADC	8	8	2, 3 PCLK*3
0008 C10Ch	IOPORT	Port function register C	PFCMTU	8	8	2, 3 PCLK*3
0008 C10Dh	IOPORT	Port function register D	PFDGPT	8	8	2, 3 PCLK*3
0008 C10Fh	IOPORT	Port function register F	PFFSCI	8	8	2, 3 PCLK*3
0008 C110h	IOPORT	Port function register G	PFGSPI	8	8	2, 3 PCLK*3
0008 C111h	IOPORT	Port function register H	PFHSPI	8	8	2, 3 PCLK*3
0008 C113h	IOPORT	Port function register J	PFJCAN	8	8	2, 3 PCLK*3
0008 C114h	IOPORT	Port function register K	PFKLIN	8	8	2, 3 PCLK*3
0008 C116h	IOPORT	Port function register M	PFMPOE	8	8	2, 3 PCLK*3
0008 C117h	IOPORT	Port function register N	PFNPOE	8	8	2, 3 PCLK*3
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLK*3
0008 C281h	SYSTEM	Deep standby wait control register	DPSWCR	8	8	4, 5 PCLK*3
0008 C282h	SYSTEM	Deep standby interrupt enable register	DPSIER	8	8	4, 5 PCLK*3
0008 C283h	SYSTEM	Deep standby interrupt flag register	DPSIFR	8	8	4, 5 PCLK*3
0008 C284h	SYSTEM	Deep standby interrupt edge register	DPSIEGR	8	8	4, 5 PCLK*3
0008 C285h	SYSTEM	Reset status register	RSTSR	8	8	4, 5 PCLK*3
0008 C289h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLK*3
0008 C28Ch	SYSTEM	Key code register for low-voltage detection control register	LVDKEYR	8	8	4, 5 PCLK*3
0008 C28Dh	SYSTEM	Voltage detection control register	LVDCR	8	8	4, 5 PCLK*3
0008 C290h	SYSTEM	Deep standby backup register 0	DPSBKR0	8	8	4, 5 PCLK*3
0008 C291h	SYSTEM	Deep standby backup register 1	DPSBKR1	8	8	4, 5 PCLK*3
0008 C292h	SYSTEM	Deep standby backup register 2	DPSBKR2	8	8	4, 5 PCLK*3
0008 C293h	SYSTEM	Deep standby backup register 3	DPSBKR3	8	8	4, 5 PCLK*3
0008 C294h	SYSTEM	Deep standby backup register 4	DPSBKR4	8	8	4, 5 PCLK*3
0008 C295h	SYSTEM	Deep standby backup register 5	DPSBKR5	8	8	4, 5 PCLK*3
0008 C296h	SYSTEM	Deep standby backup register 6	DPSBKR6	8	8	4, 5 PCLK*3
0008 C297h	SYSTEM	Deep standby backup register 7	DPSBKR7	8	8	4, 5 PCLK*3
0008 C298h	SYSTEM	Deep standby backup register 8	DPSBKR8	8	8	4, 5 PCLK*3
0008 C299h	SYSTEM	Deep standby backup register 9	DPSBKR9	8	8	4, 5 PCLK*3
0008 C29Ah	SYSTEM	Deep standby backup register 10	DPSBKR10	8	8	4, 5 PCLK*3
0008 C29Bh	SYSTEM	Deep standby backup register 11	DPSBKR11	8	8	4, 5 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (17 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 123Ah	MTU	Timer interrupt skipping mode register A	TITMRA	8	8	5 ICLK
000C 123Bh	MTU	Timer interrupt skipping set register 2A	TITCR2A	8	8	5 ICLK
000C 123Ch	MTU	Timer interrupt skipping counter 2A	TITCNT2A	8	8	5 ICLK
000C 1240h	MTU4	Timer A/D converter start request control register	TADCR	16	16	5 ICLK
000C 1244h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	5 ICLK
000C 1246h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	5 ICLK
000C 1248h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	5 ICLK
000C 124Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	5 ICLK
000C 1260h	MTU	Timer waveform control register A	TWCRA	8	8	5 ICLK
000C 1270h	MTU3	Timer mode register 2A	TMDR2A	8	8	5 ICLK
000C 1272h	MTU3	Timer general register E	TGRE	16	16	5 ICLK
000C 1274h	MTU4	Timer general register E	TGRE	16	16	5 ICLK
000C 1276h	MTU4	Timer general register F	TGRF	16	16	5 ICLK
000C 1280h	MTU	Timer start register A	TSTRA	8	8, 16	5 ICLK
000C 1281h	MTU	Timer synchronous register A	TSYRA	8	8	5 ICLK
000C 1282h	MTU	Timer counter synchronous start register	TCSYSTR	8	8	5 ICLK
000C 1284h	MTU	Timer read/write enable register A	TRWERA	8	8	5 ICLK
000C 1300h	MTU0	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1301h	MTU0	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1302h	MTU0	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1303h	MTU0	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1304h	MTU0	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1305h	MTU0	Timer status register	TSR	8	8	5 ICLK
000C 1306h	MTU0	Timer counter	TCNT	16	16	5 ICLK
000C 1308h	MTU0	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 130Ah	MTU0	Timer general register B	TGRB	16	16	5 ICLK
000C 130Ch	MTU0	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 130Eh	MTU0	Timer general register D	TGRD	16	16	5 ICLK
000C 1320h	MTU0	Timer general register E	TGRE	16	16, 32	5 ICLK
000C 1322h	MTU0	Timer general register F	TGRF	16	16	5 ICLK
000C 1324h	MTU0	Timer interrupt enable register 2	TIER2	8	8, 16	5 ICLK
000C 1325h	MTU0	Timer status register 2	TSR2	8	8	5 ICLK
000C 1326h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK
000C 1380h	MTU1	Timer control register	TCR	8	8, 16	5 ICLK
000C 1381h	MTU1	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1382h	MTU1	Timer I/O control register	TIOR	8	8	5 ICLK
000C 1384h	MTU1	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1385h	MTU1	Timer status register	TSR	8	8	5 ICLK
000C 1386h	MTU1	Timer counter	TCNT	16	16	5 ICLK
000C 1388h	MTU1	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 138Ah	MTU1	Timer general register B	TGRB	16	16	5 ICLK

Table 4.1 List of I/O Registers (Address Order) (24 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 22B6h	GPT3	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK*4
000C 22B8h	GPT3	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK*4
000C 22BAh	GPT3	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK*4
000C 22BCh	GPT3	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK*4
000C 22BEh	GPT3	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK*4
000C 22C0h	GPT3	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK*4
000C 22C2h	GPT3	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK*4
000C 2300h	GPT0	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2302h	GPT1	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2304h	GPT2	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2306h	GPT3	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2318h	GPT0	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 231Ah	GPT0	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 231Ch	GPT1	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 231Eh	GPT1	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2320h	GPT2	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 2322h	GPT2	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2324h	GPT3	GTIOCA falling output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 2326h	GPT3	GTIOCB falling output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2328h	GPT0	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 232Ah	GPT0	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 232Ch	GPT1	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 232Eh	GPT1	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 2330h	GPT2	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 2332h	GPT2	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 2334h	GPT3	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 2336h	GPT3	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 PCLK*3
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 PCLK*3
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 PCLK*3
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 PCLK*3
007F C440h	FLASH	Data flash read enable register 0	DFLRE0	16	16	2, 3 PCLK*3
007F C442h	FLASH	Data flash read enable register 1	DFLRE1	16	16	2, 3 PCLK*3
007F C450h	FLASH	Data flash programming/erasure enable register 0	DFLWE0	16	16	2, 3 PCLK*3
007F C452h	FLASH	Data flash programming/erasure enable register 1	DFLWE1	16	16	2, 3 PCLK*3
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 PCLK*3
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 PCLK*3
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 PCLK*3
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 PCLK*3
007F FFB4h	FLASH	Flash protect register	FPROTR	16	16	2, 3 PCLK*3
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 PCLK*3

Table 4.2 List of I/O Registers (Bit Order) (9 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IRQCR0	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR1	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR2	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR3	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR4	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR5	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR6	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR7	—	—	—	—	IRQMD[1:0]		—	—
ICU	NMISR	—	—	—	—	—	OSTST	LVDST	NMIST
ICU	NMIER	—	—	—	—	—	OSTEN	LVDEN	NMIEN
ICU	NMICLR	—	—	—	—	—	OSTCLR	—	NMICLR
ICU	NMICR	—	—	—	—	NMIMD	—	—	—
CMT	CMSTR0	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR1	STR0
CMT0	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT0	CMCNT								
CMT0	CMCOR								
CMT1	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT1	CMCNT								
CMT1	CMCOR								
CMT	CMSTR1	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR3	STR2
CMT2	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT2	CMCNT								
CMT2	CMCOR								
CMT3	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT3	CMCNT								
CMT3	CMCOR								
WDT	TCSR	—	TMS	TME	—	—		CKS[2:0]	
WDT	WINA								
WDT	TCNT								
WDT	WINB								
WDT	RSTCSR	WOVF	RSTE	—	—	—	—	—	—
IWDT	IWDTCR	—	—	—	—	—	—	—	—
			CKS[3:0]			—	—	TOPS[1:0]	
IWDT	IWDTSR	—	UNDFF			CNTVAL[13:0]			
					CNTVAL[13:0]				
AD0	ADDRA*1	—	—	—	—	—	—		

Table 4.2 List of I/O Registers (Bit Order) (16 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
POE	POECR2	—	—	—	—	—	MTU3BDZE	MTU4ACZE	MTU4BDZE
		—	—	—	—	—	MTU6BDZE	MTU7ACZE	MTU7BDZE
POE	POECR3	—	—	—	—	—	—	GPT3ABZE	GPT2ABZE
		—	—	—	—	—	—	GPT1ABZE	GPT0ABZE
POE	POECR4	—	—	IC5ADDMT67ZE	IC4ADDMT67ZE	IC3ADDMT67ZE	—	IC1ADDMT67ZE	CMADDMT67ZE
		—	—	IC5ADDMT34ZE	IC4ADDMT34ZE	IC3ADDMT34ZE	IC2ADDMT34ZE	—	CMADDMT34ZE
POE	POECR5	—	—	—	—	—	—	—	—
		—	—	IC5ADDMT0ZE	IC4ADDMT0ZE	—	IC2ADDMT0ZE	IC1ADDMT0ZE	CMADDMT0ZE
POE	POECR6	—	—	—	IC4ADDGPT23ZE	IC3ADDGPT23ZE	IC2ADDGPT23ZE	IC1ADDGPT23ZE	CMADDGPT23ZE
		—	—	IC5ADDGPT01ZE	—	IC3ADDGPT01ZE	IC2ADDGPT01ZE	IC1ADDGPT01ZE	CMADDGPT01ZE
POE	ICSR4	—	—	—	POE10F	—	—	POE10E	PIE4
		—	—	—	—	—	—	POE10M[1:0]	
POE	ALR1	—	—	—	—	—	—	—	—
		OLSEN	—	OLSG2B	OLSG2A	OLSG1B	OLSG1A	OLSG0B	OLSG0A
POE	ICSR5	—	—	—	POE11F	—	—	POE11E	PIE5
		—	—	—	—	—	—	POE11M[1:0]	
CAN0*3	MB.ID	IDE	RTR	—			SID[10:0]		
				SID[10:0]				EID[17:0]	
					EID[17:0]				
					EID[17:0]				
	MB.DLC	—	—	—	—	—	—	—	—
		—	—	—	—		DLC[3:0]		
	MB.DATA 0 to 7								
	MB.TS				TSH[7:0]				
					TSL[7:0]				
CAN0*3	MKR0	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR1	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR2	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR3	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR4	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				

Table 5.11 Timing of On-Chip Peripheral Modules (3)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	4	4096	t_{Pcyc}	Figure 5.11
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2-3	-	ns	
		Slave		(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2-3	-	ns	
		Slave		(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2	-		
	RSPCK clock rise/fall time	Output	t_{SPCKR} t_{SPCKF}	-	5	ns	
		Input		-	1	µs	
	Data input setup time	Master	t_{SU}	25	-	ns	Figure 5.12 to Figure 5.15
		Slave		0	-		
	Data input hold time	Master	t_H	0	-	ns	
		Slave		20+2×t_{Pcyc}	-		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	-	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	-	t_{Pcyc}	
	Data output delay time	Master	t_{OD}	-	20	ns	
		Slave		-	3×t_{Pcyc} +40		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay time	Master	t_{TD}	t_{SPcyc}+2×t_{Pcyc}	8×t_{SPcyc} +2×t_{Pcyc}	ns	
		Slave		4×t_{Pcyc}	-		
	MOSI, MISO rise/fall time	Output	t_{DR} t_{DF}	-	15	ns	Figure 5.12 to Figure 5.15
		Input		-	1	µs	
	SSL rise/fall time	Output	t_{SSLR} t_{SSLF}	-	15	ns	
		Input		-	1	µs	
	Slave access time		t_{SA}	-	4	t_{Pcyc}	Figure 5.12 to Figure 5.15
	Slave output release time		t_{REL}	-	3	t_{Pcyc}	

Note: • Note 1: t_{Pcyc}: PCLK cycle

Table 5.12 Timing of On-Chip Peripheral Modules (4)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
MTU3	Input capture input pulse width (single-edge setting)	t_{TICW}	3.0	-	t_{Icyc}	Figure 5.16
	Input capture input pulse width (both-edge setting)	t_{TICW}	5.0	-	t_{Icyc}	
	Timer clock pulse width (single-edge setting)	$t_{TCKWH/L}$	3.0	-	t_{Icyc}	Figure 5.17
	Timer clock pulse width (both-edge setting)	$t_{TCKWH/L}$	5.0	-	t_{Icyc}	
	Timer clock pulse width (phase coefficient mode)	$t_{TCKWH/L}$	5.0	-	t_{Icyc}	
GPT	Input capture input pulse width (single-edge setting)	t_{GTICW}	3.0	-	t_{Icyc}	Figure 5.18
	Input capture input pulse width (both-edge setting)	t_{GTICW}	5.0	-	t_{Icyc}	

Note: • t_{Icyc}: ICLK cycle

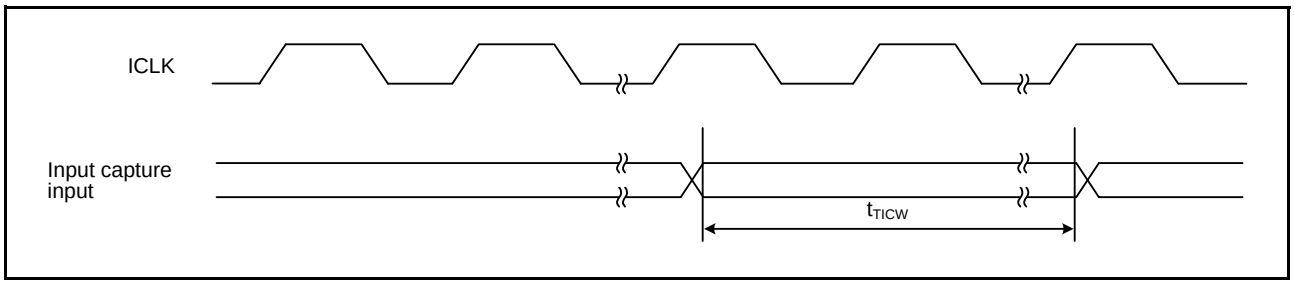

Figure 5.16 MTU3 Input/Output Timing

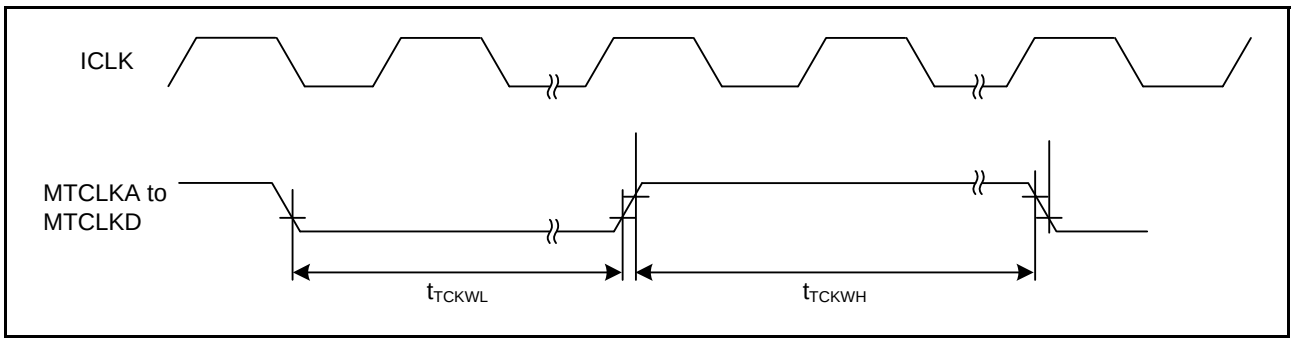

Figure 5.17 MTU3 Clock Input Timing

5.4 A/D Conversion Characteristics

Table 5.15 10-Bit A/D Conversion Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Ta = Topr

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 25-MHz operation)	2.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 2 and 3.

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 50-MHz operation)	1.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.16 12-Bit A/D Conversion Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Ta = Topr, ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (AD clock = 25-MHz operation)		2.0	-	-	µs	Sampling 20 states
Analog input capacitance		-	-	6	pF	
Integral nonlinearity error		-	-	±4.0	LSB	
Offset error		-	-	±7.5	LSB	
Full-scale error		-	-	±7.5	LSB	
Quantization error		-	±0.5	-	LSB	
Absolute accuracy	When a sample-and-hold circuit is in use	-	-	±8.0	LSB	AVin = 0.25 to AV_{REFH} - 0.25
	When a sample-and-hold circuit is not in use	-	-	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		-	-	3.0	kΩ	

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 2 and 3. ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz.

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (AD clock = 25-MHz operation)		1.0	-	-	µs	Sampling 20 states
Analog input capacitance		-	-	6	pF	
Integral nonlinearity error		-	-	±4.0	LSB	
Offset error		-	-	±7.5	LSB	
Full-scale error		-	-	±7.5	LSB	
Quantization error		-	±0.5	-	LSB	
Absolute accuracy	When a sample-and-hold circuit is in use	-	-	±8.0	LSB	AVin = 0.25 to AV_{REFH} - 0.25
	When a sample-and-hold circuit is not in use	-	-	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		-	-	3.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

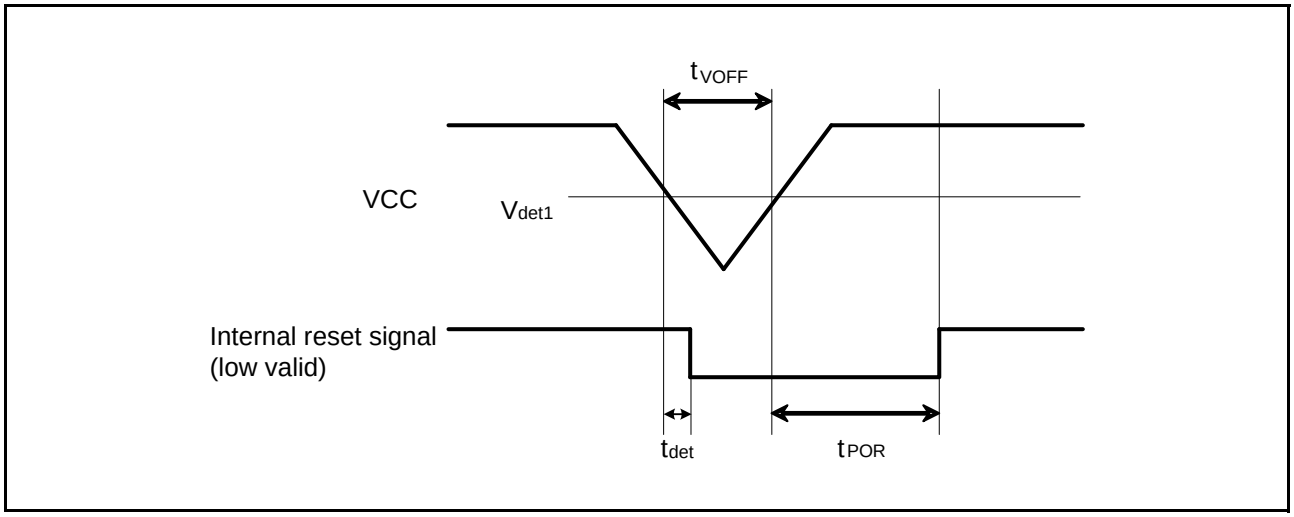

Figure 5.21 Voltage Detection Circuit Timing (Vdet1)

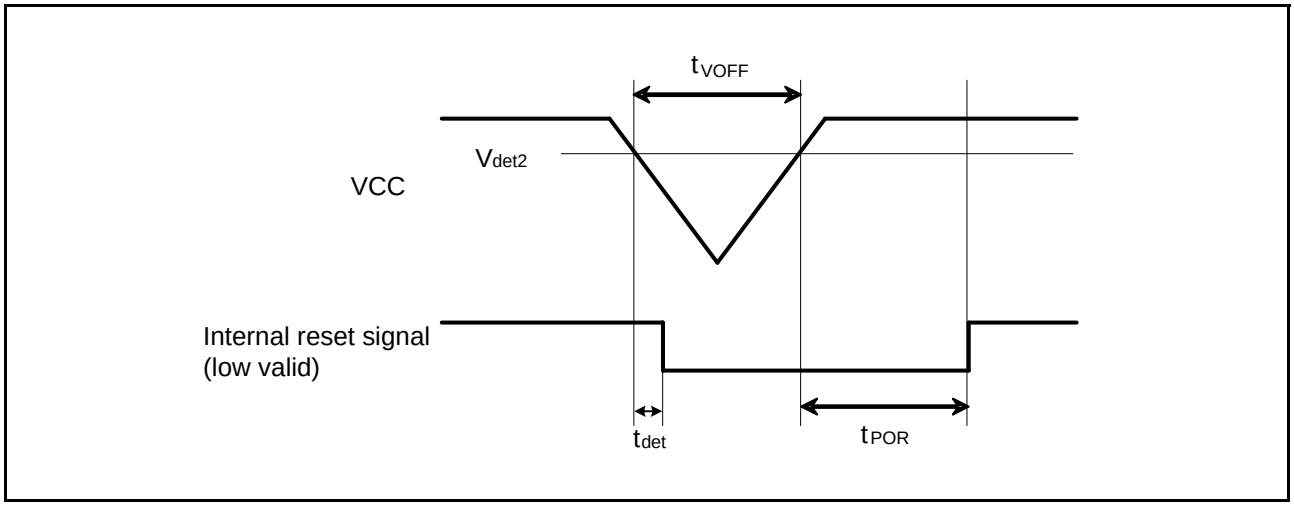

Figure 5.22 Voltage Detection Circuit Timing (Vdet2)