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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | I²C, LINbus, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562taedfm-v3 |

**Table 1.1 Outline of Specifications (4 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| Communications | CAN module (CAN) (as an optional function) | • 1 channel<br>• 32 mailboxes |
| | Serial peripheral interface (RSPI) | • 1 unit<br>• RSPI transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>Capable of handling serial transfer as a master or slave<br>• Data formats<br>Switching between MSB first and LSB first<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>• Buffered structure<br>• Double buffers for both transmission and reception |
| | LIN module (LIN) | • 1 channel (LIN master)<br>• Supports revisions 1.3, 2.0, and 2.1 of the LIN protocol |
| A/D converter | 12-bit A/D converter (S12ADA) | • 12 bits (2 units x 4 channels)<br>• 12-bit resolution<br>• Conversion time:<br>1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC = 4.0 to 5.5 V<br>2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC0 = 3.0 to 3.6 V<br>• Two basic operating modes<br>Single mode and scan mode<br>• Scan mode<br>One-cycle scan mode<br>Continuous scan mode<br>2-channel scan mode (Input ports of the A/D unit are divided into two groups in this mode, and the activation sources are separately selectable for each group.)<br>• Sample-and-hold function<br>A common sample-and-hold circuit for both units is included.<br>Additionally, sample-and-hold circuit for each unit is included. (three channels per unit)<br>• A/D-conversion register settings for each input pin.<br>• Two registers for the result of conversion are provided for a single analog input pin of each unit (AN000 and AN100).<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal.<br>• Functionality for 8- or 10-bit precision output<br>Right-shifting of the results of conversion for output by two or four bits is selectable.<br>• Self-diagnostic function<br>The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0).<br>• Amplification of input signals by a programmable gain amplifier (three channels per unit)<br>Amplification rate: 2.0-, 2.5-, 3.077-, 3.636-, 4.0-, 4.444-, 5.0-, 5.714-, 6.667-, 10.0-, or 13.333-times amplification (a total of 11 steps)<br>• Window comparators (three channels per unit) |

**Table 1.1 Outline of Specifications (5 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| A/D converter | 10-bit A/D converter (ADA) | • 10 bits (1 unit x 12 channels)<br>• 10-bit resolution<br>• Conversion time:<br>1.0 µs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V<br>2.0 µs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V<br>• Two basic operating modes<br>Single mode and scan mode<br>• Scan mode<br>One-cycle scan mode<br>Continuous scan mode<br>• Sample-and-hold function<br>A common sample-and-hold circuit for both units is included.<br>• A/D-conversion register settings for each input pin<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal.<br>• Functionality for 8-bit precision output<br>Right-shifting the results of conversion for output by two bits is selectable.<br>• Self-diagnostic function<br>The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF). |
| CRC calculator (CRC) | | • CRC code generation for arbitrary amounts of data in 8-bit units<br>• Select any of three generating polynomials:<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$.<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable. |
| Operating frequency | | ICLK: 8 to 100 MHz<br>PCLK: 8 to 50 MHz |
| Power supply voltage | | • 3-V version<br>VCC = PLLVCC = 2.7 to 3.6V<br>AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V<br>VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0<br>VREF = 3.0 to AVCC, or 4.0 to AVCC<br>• 5-V version<br>VCC = PLLVCC = 4.0 to 5.5V<br>AVCC0 = AVCC = 4.0 to 5.5V<br>VREFH0 = 4.0 to AVCC0<br>VREF = 4.0 to AVCC |
| Operating temperature | | D version: -40 to +85°C, G version: -40 to +105°C*1 |
| Packages | | 112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch)<br>100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch)<br>80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch)<br>64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch)<br>64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch) |

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

**Table 1.2 Functions of RX62T Group and RX62G Group Products (2 / 2)**

| Functions | RX62G Group | | RX62T Group | | | | |
|---|---|---|---|---|---|---|---|
| Pin number | 112 Pins | 100 Pins | 112 Pins | 100 Pins | 80 Pins (R5F562T xGDFF) | 80 Pins | 64 Pins |
| Package | LQFP2020 (0.65-mm pitch) | LQFP1414 (0.5-mm pitch) | LQFP2020 (0.65-mm pitch) | LQFP1414 (0.5-mm pitch) | LQFP1414 (0.65-mm pitch) | LQFP1414 (0.65-mm pitch) | LQFP1010 (0.5-mm pitch)<br>LQFP1414 (0.8-mm pitch) |

O: Supported, —: Not supported

Note 1. For the MTU and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details. In addition, the CAN module is an optional function. See Table 1.3 for details.

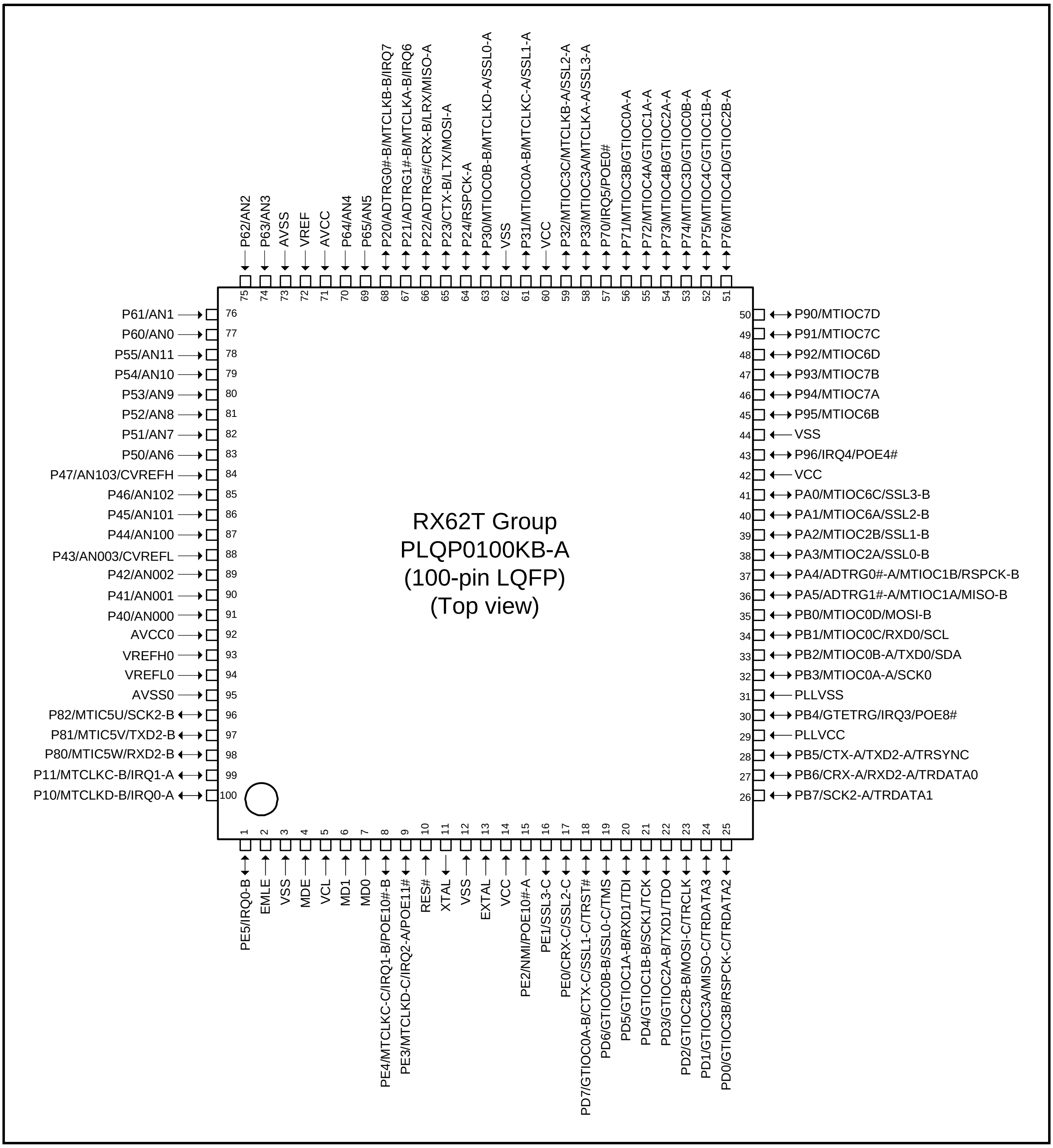



**Figure 1.4 Pin Assignment of the 100-Pin LQFP**

**Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 41 | | PA0 | | MTIOC6C | SSL3-B | | | |
| 42 | VCC | | | | | | | |
| 43 | | P96 | | | | IRQ4 | POE4# | |
| 44 | VSS | | | | | | | |
| 45 | | P95 | | MTIOC6B | | | | |
| 46 | | P94 | | MTIOC7A | | | | |
| 47 | | P93 | | MTIOC7B | | | | |
| 48 | | P92 | | MTIOC6D | | | | |
| 49 | | P91 | | MTIOC7C | | | | |
| 50 | | P90 | | MTIOC7D | | | | |
| 51 | | P76 | | MTIOC4D/ GTIOC2B-A | | | | |
| 52 | | P75 | | MTIOC4C/ GTIOC1B-A | | | | |
| 53 | | P74 | | MTIOC3D/ GTIOC0B-A | | | | |
| 54 | | P73 | | MTIOC4B/ GTIOC2A-A | | | | |
| 55 | | P72 | | MTIOC4A/ GTIOC1A-A | | | | |
| 56 | | P71 | | MTIOC3B/ GTIOC0A-A | | | | |
| 57 | | P70 | | | | IRQ5 | POE0# | |
| 58 | | P33 | | MTIOC3A/ MTCLKA-A | SSL3-A | | | |
| 59 | | P32 | | MTIOC3C/ MTCLKB-A | SSL2-A | | | |
| 60 | VCC | | | | | | | |
| 61 | | P31 | | MTIOC0A-B/ MTCLKC-A | SSL1-A | | | |
| 62 | VSS | | | | | | | |
| 63 | | P30 | | MTIOC0B-B/ MTCLKD-A | SSL0-A | | | |
| 64 | | P24 | | | RSPCK-A | | | |
| 65 | | P23 | | | CTX-B/ LTX/ MOSI-A | | | |
| 66 | | P22 | ADTRG# | | CRX-B/ LRX/ MISO-A | | | |
| 67 | | P21 | ADTRG1#-B | MTCLKA-B | | IRQ6 | | |
| 68 | | P20 | ADTRG0#-B | MTCLKB-B | | IRQ7 | | |
| 69 | | P65 | AN5 | | | | | |
| 70 | | P64 | AN4 | | | | | |
| 71 | AVCC | | | | | | | |
| 72 | VREF | | | | | | | |
| 73 | AVSS | | | | | | | |
| 74 | | P63 | AN3 | | | | | |
| 75 | | P62 | AN2 | | | | | |
| 76 | | P61 | AN1 | | | | | |

**Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 77 | | P60 | AN0 | | | | | |
| 78 | | P55 | AN11 | | | | | |
| 79 | | P54 | AN10 | | | | | |
| 80 | | P53 | AN9 | | | | | |
| 81 | | P52 | AN8 | | | | | |
| 82 | | P51 | AN7 | | | | | |
| 83 | | P50 | AN6 | | | | | |
| 84 | | P47 | AN103/ CVREFH | | | | | |
| 85 | | P46 | AN102 | | | | | |
| 86 | | P45 | AN101 | | | | | |
| 87 | | P44 | AN100 | | | | | |
| 88 | | P43 | AN003/ CVREFL | | | | | |
| 89 | | P42 | AN002 | | | | | |
| 90 | | P41 | AN001 | | | | | |
| 91 | | P40 | AN000 | | | | | |
| 92 | AVCC0 | | | | | | | |
| 93 | VREFH0 | | | | | | | |
| 94 | VREFL0 | | | | | | | |
| 95 | AVSS0 | | | | | | | |
| 96 | | P82 | | MTIC5U | SCK2-B | | | |
| 97 | | P81 | | MTIC5V | TXD2-B | | | |
| 98 | | P80 | | MTIC5W | RXD2-B | | | |
| 99 | | P11 | | MTCLKC-B | | IRQ1-A | | |
| 100 | | P10 | | MTCLKD-B | | IRQ0-A | | |

**Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (1 / 3)**

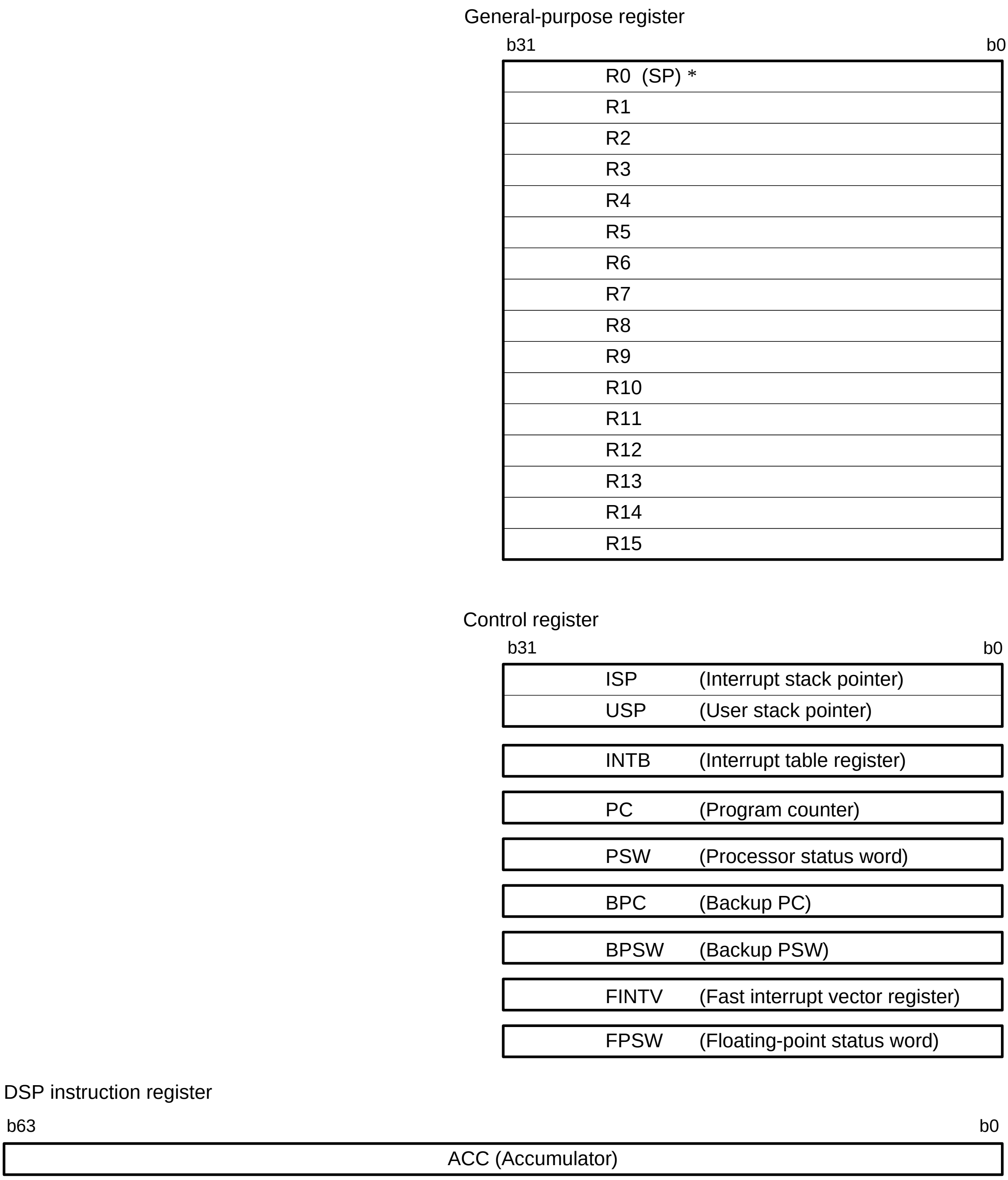
| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 1 | EMLE | | | | | | | |
| 2 | VSS | | | | | | | |
| 3 | MDE | | | | | | | |
| 4 | VCL | | | | | | | |
| 5 | MD1 | | | | | | | |
| 6 | MD0 | | | | | | | |
| 7 | | PE4 | | MTCLKC-C | | IRQ1-B | POE10#-B | |
| 8 | | PE3 | | MTCLKD-C | | IRQ2-A | POE11# | |
| 9 | RES# | | | | | | | |
| 10 | XTAL | | | | | | | |
| 11 | VSS | | | | | | | |
| 12 | EXTAL | | | | | | | |
| 13 | VCC | | | | | | | |
| 14 | | PE2 | | | | NMI | POE10#-A | |
| 15 | | PE0 | | | CRX-C | | | |
| 16 | | PD7 | | GTIOC0A-B | CTX-C | | | TRST# |
| 17 | | PD6 | | GTIOC0B-B | | | | TMS |
| 18 | | PD5 | | GTIOC1A-B | RXD1 | | | TDI |
| 19 | | PD4 | | GTIOC1B-B | SCK1 | | | TCK |
| 20 | | PD3 | | GTIOC2A-B | TXD1 | | | TDO |
| 21 | | PB7 | | | SCK2-A | | | |
| 22 | | PB6 | | | CRX-A/ RXD2-A | | | |
| 23 | | PB5 | | | CTX-A/ TXD2-A | | | |
| 24 | PLLVCC | | | | | | | |
| 25 | | PB4 | | GTETRG | | IRQ3 | POE8# | |
| 26 | PLLVSS | | | | | | | |
| 27 | | PB3 | | MTIOC0A-A | SCK0 | | | |
| 28 | | PB2 | | MTIOC0B-A | TXD0/SDA | | | |
| 29 | | PB1 | | MTIOC0C | RXD0/SCL | | | |
| 30 | | PB0 | | MTIOC0D | MOSI-B | | | |
| 31 | | PA3 | | MTIOC2A | SSL0-B | | | |
| 32 | | PA2 | | MTIOC2B | SSL1-B | | | |
| 33 | VCC | | | | | | | |
| 34 | | P96 | | | | IRQ4 | POE4# | |
| 35 | VSS | | | | | | | |
| 36 | | P95 | | MTIOC6B | | | | |
| 37 | | P94 | | MTIOC7A | | | | |
| 38 | | P93 | | MTIOC7B | | | | |
| 39 | | P92 | | MTIOC6D | | | | |
| 40 | | P91 | | MTIOC7C | | | | |
| 41 | | P76 | | MTIOC4D/ GTIOC2B-A | | | | |

**Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)**

| Pin No. (64-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 40 | | P33 | | MTIOC3A/<br>MTCLKA-A | SSL3-A | | | |
| 41 | | P32 | | MTIOC3C/<br>MTCLKB-A | SSL2-A | | | |
| 42 | VCC | | | | | | | |
| 43 | | P31 | | MTIOC0A-B/<br>MTCLKC-A | SSL1-A | | | |
| 44 | VSS | | | | | | | |
| 45 | | P30 | | MTIOC0B-B/<br>MTCLKD-A | SSL0-A | | | |
| 46 | | P24 | | | RSPCK-A | | | |
| 47 | | P23 | | | CTX-B/<br>LTX/<br>MOSI-A | | | |
| 48 | | P22 | | | CRX-B/<br>LRX/<br>MISO-A | | | |
| 49 | | P47 | AN103/<br>CVREFH | | | | | |
| 50 | | P46 | AN102 | | | | | |
| 51 | | P45 | AN101 | | | | | |
| 52 | | P44 | AN100 | | | | | |
| 53 | | P43 | AN003/<br>CVREFL | | | | | |
| 54 | | P42 | AN002 | | | | | |
| 55 | | P41 | AN001 | | | | | |
| 56 | | P40 | AN000 | | | | | |
| 57 | AVCC0 | | | | | | | |
| 58 | VREFH0 | | | | | | | |
| 59 | VREFL0 | | | | | | | |
| 60 | AVSS0 | | | | | | | |
| 61 | | P11 | | MTCLKC-B | | IRQ1-A | | |
| 62 | | P10 | | MTCLKD-B | | IRQ0-A | | |
| 63 | | PA5 | ADTRG1#-A | MTIOC1A | MISO-B | | | |
| 64 | | PA4 | ADTRG0#-A | MTIOC1B | RSPCK-B | | | |

# 2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.




Note: * The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

**Figure 2.1 Register Set of the CPU**

## 2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

## 2.2 Control Registers

### (1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

### (2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.
Set INTB to a multiple of four.

### (3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

### (4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

### (5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

### (6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

### (7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

### (8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

### (9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

(a) Write to an I/O register.

(b) Read the value from the I/O register to a general register.

(c) Execute the operation using the value read.

(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

**Table 4.1 List of I/O Registers (Address Order) (11 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8383h | RSPI | RSPI status register | SPSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8384h | RSPI | RSPI data register | SPDR | 16, 32 | 16, 32 | 2, 3 PCLK*3 |
| 0008 8388h | RSPI | RSPI sequence control register | SPSCR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8389h | RSPI | RSPI sequence status register | SPSSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Ah | RSPI | RSPI bit rate register | SPBR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Bh | RSPI | RSPI data control register | SPDCR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Ch | RSPI | RSPI clock delay register | SPCKD | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Dh | RSPI | RSPI slave select negation delay register | SSLND | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Eh | RSPI | RSPI next-access delay register | SPND | 8 | 8 | 2, 3 PCLK*3 |
| 0008 838Fh | RSPI | RSPI control register 2 | SPCR2 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 8390h | RSPI | RSPI command register 0 | SPCMD0 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8392h | RSPI | RSPI command register 1 | SPCMD1 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8394h | RSPI | RSPI command register 2 | SPCMD2 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8396h | RSPI | RSPI command register 3 | SPCMD3 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 8398h | RSPI | RSPI command register 4 | SPCMD4 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 839Ah | RSPI | RSPI command register 5 | SPCMD5 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 839Ch | RSPI | RSPI command register 6 | SPCMD6 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 839Eh | RSPI | RSPI command register 7 | SPCMD7 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9000h | S12AD0 | A/D control register | ADCSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 9004h | S12AD0 | A/D channel select register | ADANS | 16 | 16 | 2, 3 PCLK*3 |
| 0008 900Ah | S12AD0 | A/D programmable gain amplifier register | ADPG | 16 | 16 | 2, 3 PCLK*3 |
| 0008 900Eh | S12AD0 | A/D control extended register | ADCER | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9010h | S12AD0 | A/D start trigger select register | ADSTRGR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9012h | S12AD | Comparator operating mode select register 0 | ADCMPMD0 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9014h | S12AD | Comparator operating mode select register 1 | ADCMPMD1 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9016h | S12AD | Comparator filter mode register 0 | ADCMPNR0 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9018h | S12AD | Comparator filter mode register 1 | ADCMPNR1 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 901Ah | S12AD | Comparator detection flag register | ADCMPFR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 901Ch | S12AD | Comparator interrupt select register | ADCMPSEL | 16 | 16 | 2, 3 PCLK*3 |
| 0008 901Eh | S12AD0 | A/D data register Diag | ADRD | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9020h | S12AD0 | A/D data register 0A | ADDR0A | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9022h | S12AD0 | A/D data register 1 | ADDR1 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9024h | S12AD0 | A/D data register 2 | ADDR2 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9026h | S12AD0 | A/D data register 3 | ADDR3 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9030h | S12AD0 | A/D data register 0B | ADDR0B | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9060h | S12AD0 | A/D sampling state register | ADSSTR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 9080h | S12AD1 | A/D control register | ADCSR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 9084h | S12AD1 | A/D channel select register | ADANS | 16 | 16 | 2, 3 PCLK*3 |
| 0008 908Ah | S12AD1 | A/D programmable gain amplifier register | ADPG | 16 | 16 | 2, 3 PCLK*3 |
| 0008 908Eh | S12AD1 | A/D control extended register | ADCER | 16 | 16 | 2, 3 PCLK*3 |
| 0008 9090h | S12AD1 | A/D start trigger select register | ADSTRGR | 16 | 16 | 2, 3 PCLK*3 |
| 0008 909Eh | S12AD1 | A/D data register Diag | ADRD | 16 | 16 | 2, 3 PCLK*3 |
| 0008 90A0h | S12AD1 | A/D data register 0A | ADDR0A | 16 | 16 | 2, 3 PCLK*3 |
| 0008 90A2h | S12AD1 | A/D data register 1 | ADDR1 | 16 | 16 | 2, 3 PCLK*3 |

**Table 4.2 List of I/O Registers (Bit Order) (3 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| MPU | RSPAGE7 | RSPN[27:0] | | | | | | | |
| | | RSPN[27:0] | | | | | | | |
| | | RSPN[27:0] | | | | | | | |
| | | RSPN[27:0] | | | | — | — | — | — |
| MPU | REPAGE7 | REPN[27:0] | | | | | | | |
| | | REPN[27:0] | | | | | | | |
| | | REPN[27:0] | | | | | | | |
| | | REPN[27:0] | | | | UAC[2:0] | | | V |
| MPU | MPEN | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | MPEN |
| MPU | MPBAC | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | UBAC[2:0] | | | — |
| MPU | MPECLR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | CLR |
| MPU | MPESTS | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | DRW | DA | IA |
| MPU | MPDEA | DEA[31:0] | | | | | | | |
| | | DEA[31:0] | | | | | | | |
| | | DEA[31:0] | | | | | | | |
| | | DEA[31:0] | | | | | | | |
| MPU | MPSA | SA[31:0] | | | | | | | |
| | | SA[31:0] | | | | | | | |
| | | SA[31:0] | | | | | | | |
| | | SA[31:0] | | | | | | | |
| MPU | MPOPS | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | S |
| MPU | MPOPI | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | INV |
| MPU | MHITI | — | — | — | — | — | — | — | — |
| | | HITI[7:0] | | | | | | | |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | UHACI[2:0] | | | — |
| MPU | MHITD | — | — | — | — | — | — | — | — |
| | | HITD[7:0] | | | | | | | |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | UHACD[2:0] | | | — |
| ICU | IR016 | — | — | — | — | — | — | — | IR |
| ICU | IR021 | — | — | — | — | — | — | — | IR |
| ICU | IR023 | — | — | — | — | — | — | — | IR |
| ICU | IR027 | — | — | — | — | — | — | — | IR |
| ICU | IR028 | — | — | — | — | — | — | — | IR |
| ICU | IR029 | — | — | — | — | — | — | — | IR |
| ICU | IR030 | — | — | — | — | — | — | — | IR |
| ICU | IR031 | — | — | — | — | — | — | — | IR |

### Table 4.2 List of I/O Registers (Bit Order) (11 / 30)

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| SCI1 | SEMR | — | — | NFEN | ABCS | — | — | — | — |
| SMCI1 | SMR | GM | BLK | PE | PM | (BCP[1:0]) | | CKS[1:0] | |
| SMCI1 | BRR | | | | | | | | |
| SMCI1 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SMCI1 | TDR | | | | | | | | |
| SMCI1 | SSR | TDRE | RDRF | ORER | ERS | PER | TEND | MPB | MPBT |
| SMCI1 | RDR | | | | | | | | |
| SMCI1 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| SCI2 | SMR | CM | CHR | PE | PM | STOP | MP | CKS[1:0] | |
| SCI2 | BRR | | | | | | | | |
| SCI2 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SCI2 | TDR | | | | | | | | |
| SCI2 | SSR | TDRE | RDRF | ORER | FER | PER | TEND | MPB | MPBT |
| SCI2 | RDR | | | | | | | | |
| SCI2 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| SMCI2 | SMR | GM | BLK | PE | PM | (BCP[1:0]) | | CKS[1:0] | |
| SMCI2 | BRR | | | | | | | | |
| SMCI2 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SMCI2 | TDR | | | | | | | | |
| SMCI2 | SSR | TDRE | RDRF | ORER | ERS | PER | TEND | MPB | MPBT |
| SMCI2 | RDR | | | | | | | | |
| SMCI2 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| CRC | CRCCR | DORCLR | — | — | — | — | LMS | GPS[1:0] | |
| CRC | CRCDIR | | | | | | | | |
| CRC | CRCDOR | | | | | | | | |
| RIIC0 | ICCR1 | ICE | IICRST | CLO | SOWP | SCLO | SDAO | SCLI | SDAI |
| RIIC0 | ICCR2 | BBSY | MST | TRS | — | SP | RS | ST | — |
| RIIC0 | ICMR1 | MTWP | CKS[2:0] | | | BCWP | BC[2:0] | | |
| RIIC0 | ICMR2 | DLCS | SDDL[2:0] | | | TMWE | TMOH | TMOL | TMOS |
| RIIC0 | ICMR3 | SMBS | WAIT | RDRFS | ACKWP | ACKBT | ACKBR | NF[1:0] | |
| RIIC0 | ICFER | — | SCLE | NFE | NACKE | SALE | NALE | MALE | TMOE |
| RIIC0 | ICSER | HOAE | — | DIDE | — | GCAE | SAR2E | SAR1E | SAR0E |
| RIIC0 | ICIER | TIE | TEIE | RIE | NAKIE | SPIE | STIE | ALIE | TMOIE |
| RIIC0 | ICSR1 | HOA | — | DID | — | GCA | AAS2 | AAS1 | AAS0 |
| RIIC0 | ICSR2 | TDRE | TEND | RDRF | NACKF | STOP | START | AL | TMOF |
| RIIC0 | SARL0 | SVA[6:0] | | | | | | | SVA0 |
| RIIC0 | TMOCNTL | | | | | | | | |
| RIIC0 | SARU0 | — | — | — | — | — | SVA[1:0] | | FS |
| RIIC0 | TMOCNTU | | | | | | | | |
| RIIC0 | SARL1 | SVA[6:0] | | | | | | | SVA0 |
| RIIC0 | SARU1 | — | — | — | — | — | SVA[1:0] | | FS |
| RIIC0 | SARL2 | SVA[6:0] | | | | | | | SVA0 |
| RIIC0 | SARU2 | — | — | — | — | — | SVA[1:0] | | FS |
| RIIC0 | ICBRL | — | — | — | BRL[4:0] | | | | |
| RIIC0 | ICBRH | — | — | — | BRH[4:0] | | | | |
| RIIC0 | ICDRT | | | | | | | | |
| RIIC0 | ICDRR | | | | | | | | |
| RSPI0 | SPCR | SPRIE | SPE | SPTIE | SPEIE | MSTR | MODFEN | TXMD | SPMS |

## Table 4.2 List of I/O Registers (Bit Order) (17 / 30)

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| CAN0*3 | MKR5 | — | — | — | SID[10:0] | | | | |
| | | SID[10:0] | | | | | | EID[17 0] | |
| | | EID[17:0] | | | | | | | |
| | | EID[17:0] | | | | | | | |
| CAN0*3 | MKR6 | — | — | — | SID[10:0] | | | | |
| | | SID[10:0] | | | | | | EID[17 0] | |
| | | EID[17:0] | | | | | | | |
| | | EID[17:0] | | | | | | | |
| CAN0*3 | MKR7 | — | — | — | SID[10:0] | | | | |
| | | SID[10:0] | | | | | | EID[17 0] | |
| | | EID[17:0] | | | | | | | |
| | | EID[17:0] | | | | | | | |
| CAN0*3 | FIDCR0 | IDE | RTR | — | SID[10:0] | | | | |
| | | SID[10:0] | | | | | | EID[17:0] | |
| | | EID[17:0] | | | | | | | |
| | | EID[17:0] | | | | | | | |
| CAN0*3 | FIDCR1 | IDE | RTR | — | SID[10:0] | | | | |
| | | SID[10:0] | | | | | | EID[17:0] | |
| | | EID[17:0] | | | | | | | |
| | | EID[17:0] | | | | | | | |
| CAN0*3 | MKIVLR | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| CAN0*3 | MIER | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| CAN0*3 | MCTL.TX | TRMREQ | RECREQ | — | ONESHOT | — | TRMABT | TRMACTIVE | SENTDATA |
| | MCTL.RX | TRMREQ | RECREQ | — | ONESHOT | — | MSGLOST | INVALDATA | NEWDATA |
| CAN0*3 | CTLR | — | — | RBOC | BOM[1:0] | | SLPM | CANM[1:0] | |
| | | TSPS[1:0] | | TSRC | TPM | MLM | IDFM[1:0] | | MBM |
| CAN0*3 | STR | — | RECST | TRMST | BOST | EPST | SLPST | HLTST | RSTST |
| | | EST | TABST | FMLST | NMLST | TFST | RFST | SDST | NDST |
| CAN0*3 | BCR | TSEG1[3:0] | | | | — | — | BRP[9:0] | |
| | | BRP[9:0] | | | | | | | |
| | | — | — | SJW[1:0] | | — | TSEG2[2:0] | | |
| | | — | — | — | — | — | — | — | — |
| CAN0*3 | RFCR | RFEST | RFWST | RFFST | RFMLF | RFUST[2:0] | | | RFE |
| CAN0*3 | RFPCR | — | — | — | — | — | — | — | — |
| CAN0*3 | TFCR | TFEST | TFFST | — | — | TFUST[2:0] | | | TFE |
| CAN0*3 | TFPCR | — | — | — | — | — | — | — | — |
| CAN0*3 | EIER | BLIE | OLIE | ORIE | BORIE | BOEIE | EPIE | EWIE | BEIE |
| CAN0*3 | EIFR | BLIF | OLIF | ORIF | BORIF | BOEIF | EPIF | EWIF | BEIF |
| CAN0*3 | RECR | — | — | — | — | — | — | — | — |
| CAN0*3 | TECR | — | — | — | — | — | — | — | — |
| CAN0*3 | ECSR | EDPM | ADEF | BE0F | BE1F | CEF | AEF | FEF | SEF |
| CAN0*3 | CSSR | — | — | — | — | — | — | — | — |
| CAN0*3 | MSSR | SEST | — | — | MBNST[4:0] | | | | |
| CAN0*3 | MSMR | — | — | — | — | — | — | MBSM[1:0] | |
| CAN0*3 | TSR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |

**Table 4.2 List of I/O Registers (Bit Order) (19 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| MTU3 | TGRA | | | | | | | | |
| MTU3 | TGRB | | | | | | | | |
| MTU4 | TGRA | | | | | | | | |
| MTU4 | TGRB | | | | | | | | |
| MTU | TCNTSA | | | | | | | | |
| MTU | TCBRA | | | | | | | | |
| MTU3 | TGRC | | | | | | | | |
| MTU3 | TGRD | | | | | | | | |
| MTU4 | TGRC | | | | | | | | |
| MTU4 | TGRD | | | | | | | | |
| MTU3 | TSR | TCFD | — | — | TCFV | TGFD | TGFC | TGFB | TGFA |
| MTU4 | TSR | TCFD | — | — | TCFV | TGFD | TGFC | TGFB | TGFA |
| MTU | TITCR1A | T3AEN | | T3ACOR[2:0] | | T4VEN | | T4VCOR[2:0] | |
| MTU | TBTERA | — | | T3ACOR[2:0] | | — | | T4VCNT[2:0]] | |
| MTU | TBTERA | — | — | — | — | — | — | BTE[1:0] | |
| MTU | TDERA | — | — | — | — | — | — | — | TDER |
| MTU | TOLBRA | — | — | OLS3N | OLS3P | OLS2N | OLS2P | OLS1N | OLS1P |
| MTU3 | TBTM | — | — | — | — | — | — | TTSB | TTSA |
| MTU4 | TBTM | — | — | — | — | — | — | TTSB | TTSA |
| MTU | TITMRA | — | — | — | — | — | — | — | TITM |
| MTU | TITCR2A | — | — | — | — | — | | TRG4COR[2:0] | |
| MTU | TITCNT2A | — | — | — | — | — | | TRG4COR[2:0] | |
| MTU4 | TADCR | BF[1:0] | | — | — | — | — | — | — |
| | | UT4AE | DT4AE | UT4BE | DT4BE | ITA3AE | ITA4VE | ITB3AE | ITB4VE |
| MTU4 | TADCORA | | | | | | | | |
| MTU4 | TADCORB | | | | | | | | |
| MTU4 | TADCOBRA | | | | | | | | |
| MTU4 | TADCOBRB | | | | | | | | |
| MTU | TWCRA | CCE | — | — | — | — | — | — | WRE |
| MTU | TMDR2A | — | — | — | — | — | — | — | DRS |
| MTU3 | TGRE | | | | | | | | |
| MTU4 | TGRE | | | | | | | | |
| MTU4 | TGRF | | | | | | | | |
| MTU | TSTRA | CST4 | CST3 | — | — | — | CST2 | CST1 | CST0 |
| MTU | TSYRA | SYNC4 | SYNC3 | — | — | — | SYNC2 | SYNC1 | SYNC0 |
| MTU | TCSYSTR | SCH0 | SCH1 | SCH2 | SCH3 | SCH4 | — | SCH6 | SCH7 |
| MTU | TRWERA | — | — | — | — | — | — | — | RWE |
| MTU0 | TCR | | CCLR[2:0] | | CKEG[1:0] | | | TPSC[2:0] | |

**Table 4.2 List of I/O Registers (Bit Order) (25 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| GPT0 | GTDBU | | | | | | | | |
| | | | | | | | | | |
| GPT0 | GTDBD | | | | | | | | |
| | | | | | | | | | |
| GPT0 | GTSOS | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | SOS[1:0] | |
| GPT0 | GTSOTR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | SOTR |
| GPT1 | GTIOR | OBHLD | OBDFLT | GTIOB[5:0] | | | | | |
| | | OAHLD | OADFLT | GTIOA[5:0] | | | | | |
| GPT1 | GTINTAD | ADTRBDEN | ADTRBUEN | ADTRADEN | ADTRAUEN | EINT | — | — | — |
| | | GTINTPR[1:0] | | GTINTF | GTINTE | GTINTD | GTINTC | GTINTB | GTINTA |
| GPT1 | GTCR | — | — | CCLR[1:0] | | — | — | TPCS[1:0] | |
| | | — | — | — | — | — | MD[2:0] | | |
| GPT1 | GTBER | — | ADTDB | ADTTB[1:0] | | — | ADTDA | ADTTA[1:0] | |
| | | — | CCRSWT | PR[1:0] | | CCRB[1:0] | | CCRA[1:0] | |
| GPT1 | GTUDC | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | UDF | UD |
| GPT1 | GTITC | — | ADTBL | — | ADTAL | — | IVTT[2:0] | | |
| | | IVTC[1:0] | | ITLF | ITLE | ITLD | ITLC | ITLB | ITLA |
| GPT1 | GTST | TUCF | — | — | — | DTEF | ITCNT[2:0] | | |
| | | TCFPU | TCFPO | TCFF | TCFE | TCFD | TCFC | TCFB | TCFA |
| GPT1 | GTCNT | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRA | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRB | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRC | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRD | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRE | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRF | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTPR | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTPBR | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTPDBR | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTADTRA | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTADTBRA | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTADTDBRA | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTADTRB | | | | | | | | |
| | | | | | | | | | |

## 5.2 DC Characteristics

**Table 5.2 DC Characteristics (1) (1 / 3)**

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

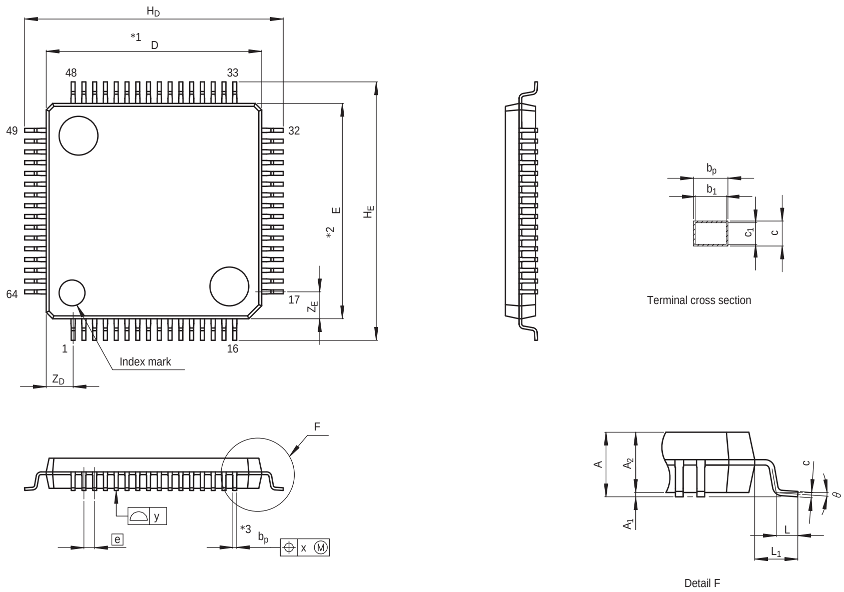
Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | CAN input pin<br>IRQ input pin<br>MTU3 input pin<br>POE3 input pin<br>SCI input pin<br>A/D trigger input pin<br>NMI input pin<br>GPT input pin<br>LIN input pin<br>RES# | $V_{IH}$ | VCC×0.8 | - | VCC+0.3 | V | |
| | | $V_{IL}$ | -0.3 | - | VCC×0.2 | | |
| | | $\Delta V_T$ | VCC ×0.06 | - | - | | |
| | RIIC input pin (IICBus) | $V_{IH}$ | VCC×0.7 | - | VCC+0.3 | | |
| | | $V_{IL}$ | -0.3 | - | VCC×0.3 | | |
| | | $\Delta V_T$ | VCC ×0.05 | - | - | | |
| | Port 4*1 (also usable as an analog port) | $V_{IH}$ | AVCC0 ×0.8 | - | AVCC0 +0.3 | | |
| | | $V_{IL}$ | - 0.3 | - | AVCC0 ×0.2 | | |
| | | $\Delta V_T$ | AVCC0 ×0.06 | - | - | | |
| | Ports 5 and 6*1 (also usable as analog ports) | $V_{IH}$ | AVCC ×0.8 | - | AVCC +0.3 | | |
| | | $V_{IL}$ | -0.3 | - | AVCC ×0.2 | | |
| | | $\Delta V_T$ | AVCC ×0.06 | - | - | | |
| | Ports 1 to 3*1<br>Ports 7 to B*1<br>Ports D, E, and G*1 | $V_{IH}$ | VCC×0.8 | - | VCC+0.3 | | |
| | | $V_{IL}$ | -0.3 | - | VCC×0.2 | | |
| | | $\Delta V_T$ | VCC ×0.06 | - | - | | |
| Input high voltage (except Schmitt trigger input pin) | MD pin, EMLE | $V_{IH}$ | VCC×0.9 | - | VCC+0.3 | V | |
| | EXTAL<br>RSPI input pin | | VCC×0.8 | | VCC+0.3 | | |
| | RIIC input pin (SMBus) | | 2.1 | | VCC+0.3 | | Conditions 1 and 2 |
| Input low voltage (except Schmitt trigger input pin) | MD pin, EMLE | $V_{IL}$ | -0.3 | - | VCC×0.1 | V | |
| | EXTAL<br>RSPI input pin | | -0.3 | - | VCC×0.2 | | |
| | RIIC input pin (SMBus) | | -0.3 | - | 0.8 | | Conditions 1 and 2 |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP64-10x10-0.50 | PLQP0064KB-A | 64P6Q-A / FP-64K / FP-64KV | 0.3g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure D 64-Pin LQFP (PLQP0064KB-A) Package Dimensions