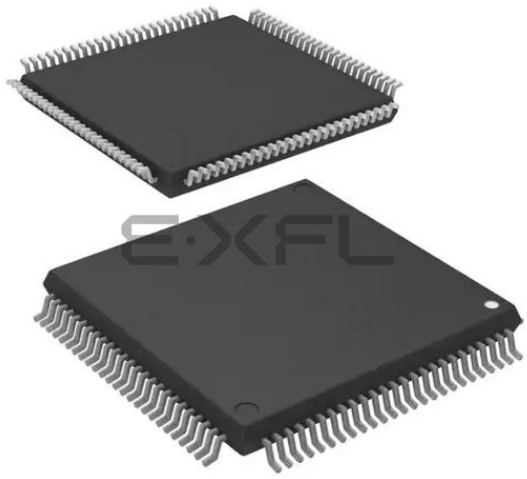
Renesas Electronics America Inc - R5F562TAEDFP#V3 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562taedfp-v3

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.

Table 1.1 Outline of Specifications (1 / 5)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU • General purpose: Sixteen 32-bit registers • Control: Nine 32-bit registers • Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement • Instructions: Little endian • Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• ROM capacity: 256 Kbytes (max.) • Two on-board programming modes • Boot mode (The user MAT is programmable via the SCI) • User program mode • Off-board programming • A PROM programmer can be used to program the user mat.
	RAM	• RAM capacity: 16 Kbytes (max.)
	Data flash	• Data flash capacity: 32 Kbytes (max.) • Supports background operations (BGO)
MCU operating mode		• Single-chip mode
Clock	Clock generation circuit	• One circuit: Main clock oscillator • Internal oscillator: Low-speed on-chip oscillator dedicated to IWDT • Structure of a PLL frequency synthesizer and frequency divider for selectable operating frequency • Oscillation stoppage detection • Independent frequency-division and multiplication settings for the system clock (ICLK) and peripheral module clock (PCLK) • The CPU and system sections such as other bus masters, MTU3, and GPT run in synchronization with the system clock (ICLK): 8 to 100 MHz. • Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz
Reset		Pin reset, power-on reset (automatic power-on reset when the power is turned on), voltage-monitoring reset, watchdog timer reset, independent watchdog timer reset, and deep software standby reset
Voltage detection circuit (LVD)		When the voltage on VCC falls below the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes • Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode

1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

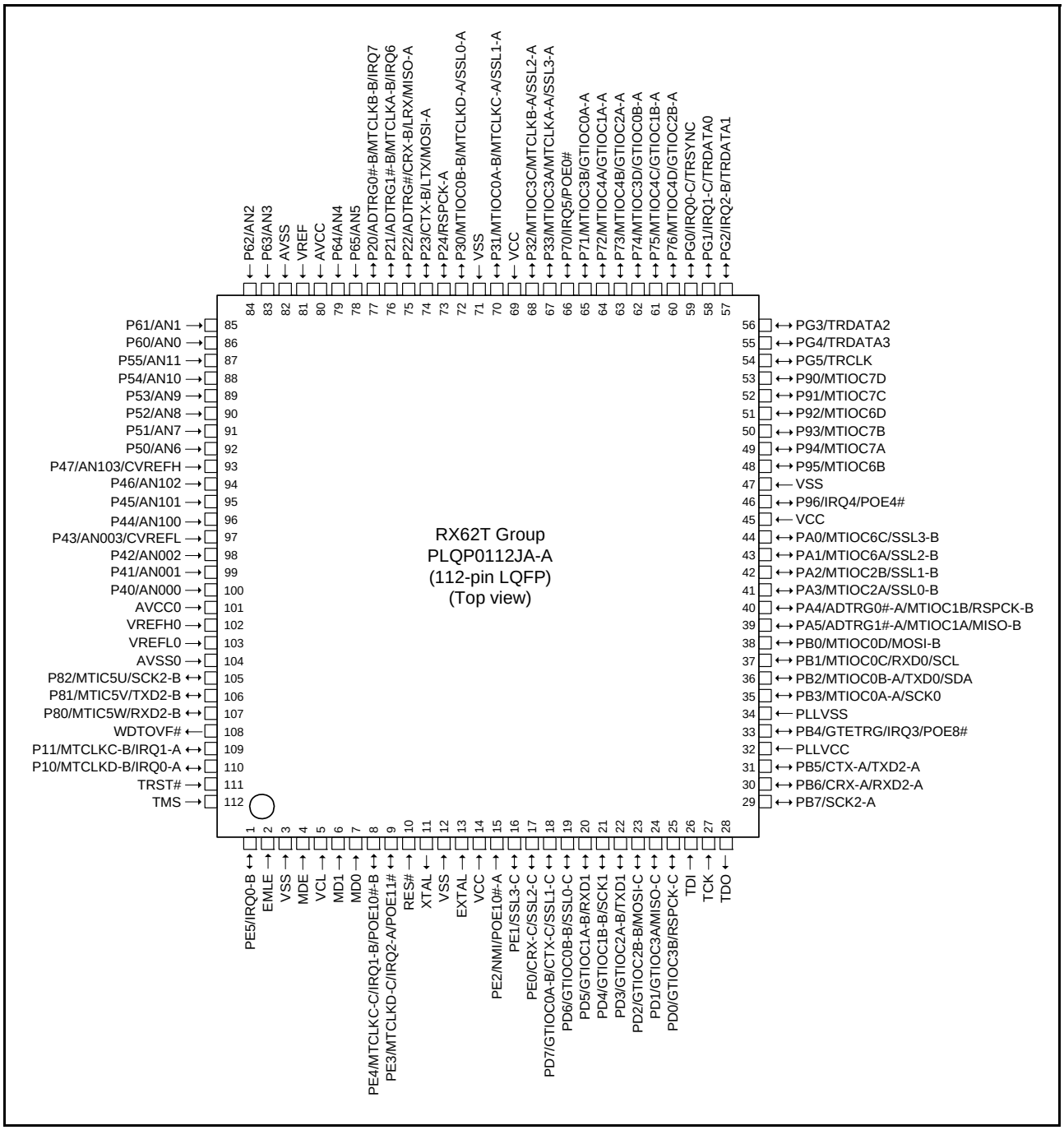

Figure 1.3 Pin Assignment of the 112-Pin LQFP

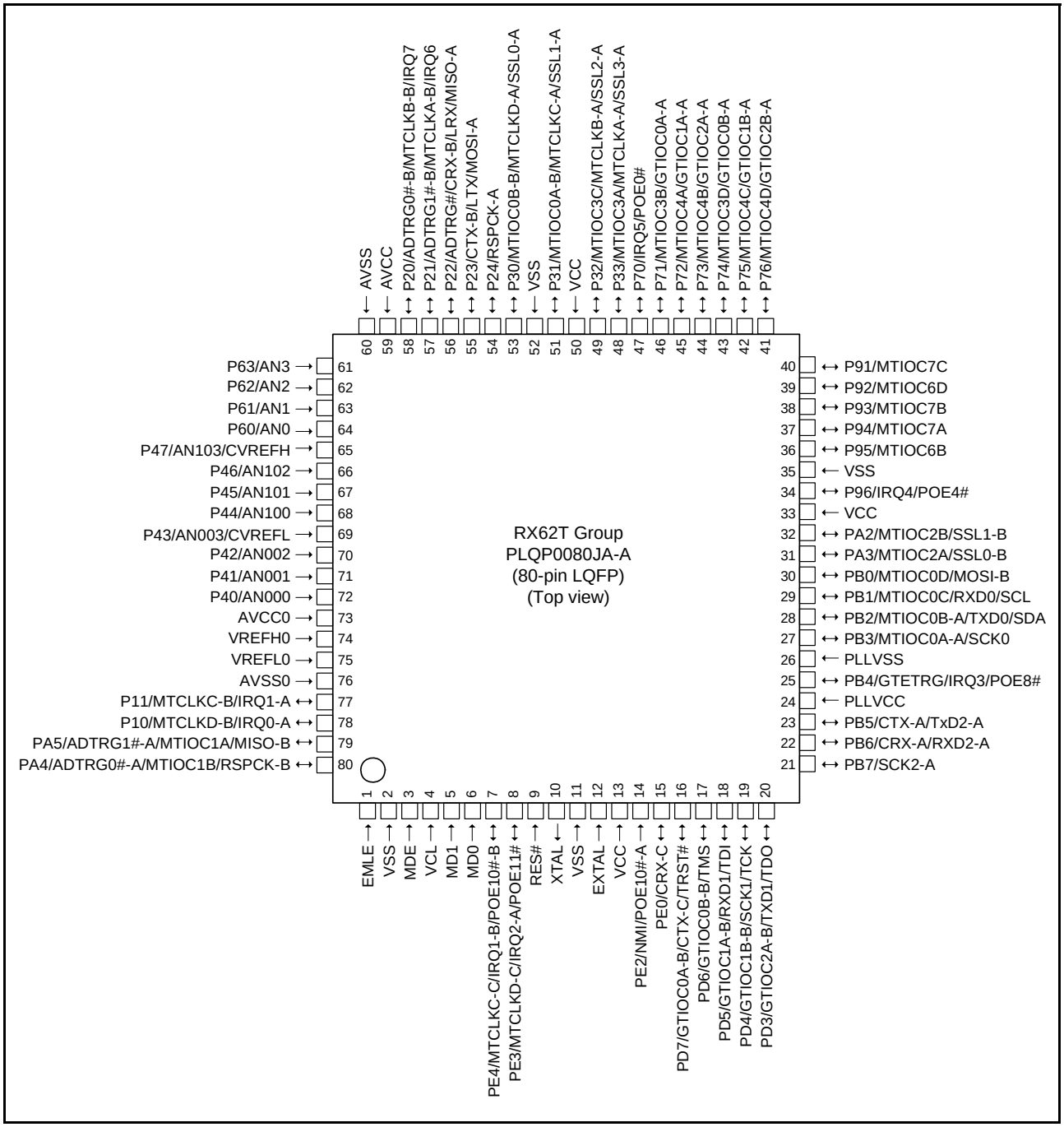

Figure 1.5 Pin Assignment of the 80-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/ SSL1-C			TRST#
19		PD6		GTIOC0B-B	SSL0-C			TMS
20		PD5		GTIOC1A-B	RXD1			TDI
21		PD4		GTIOC1B-B	SCK1			TCK
22		PD3		GTIOC2A-B	TXD1			TDO
23		PD2		GTIOC2B-B	MOSI-C			TRCLK
24		PD1		GTIOC3A	MISO-C			TRDATA3
25		PD0		GTIOC3B	RSPCK-C			TRDATA2
26		PB7			SCK2-A			TRDATA1
27		PB6			CRX-A/ RXD2-A			TRDATA0
28		PB5			CTX-A/ TXD2-A			TRSYNC
29	PLLVCC							
30		PB4		GTETRG		IRQ3	POE8#	
31	PLLVSS							
32		PB3		MTIOC0A-A	SCK0			
33		PB2		MTIOC0B-A	TXD0/SDA			
34		PB1		MTIOC0C	RXD0/SCL			
35		PB0		MTIOC0D	MOSI-B			
36		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
37		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
38		PA3		MTIOC2A	SSL0-B			
39		PA2		MTIOC2B	SSL1-B			
40		PA1		MTIOC6A	SSL2-B			

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
1	EMLE							
2	VSS							
3	MDE							
4	VCL							
5	MD1							
6	MD0							
7		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
8		PE3		MTCLKD-C		IRQ2-A	POE11#	
9	RES#							
10	XTAL							
11	VSS							
12	EXTAL							
13	VCC							
14		PE2				NMI	POE10#-A	
15		PD7		GTIOC0A-B				TRST#
16		PD6		GTIOC0B-B				TMS
17		PD5		GTIOC1A-B	RXD1			TDI
18		PD4		GTIOC1B-B	SCK1			TCK
19		PD3		GTIOC2A-B	TXD1			TDO
20		PD2		GTIOC2B-B				
21		PB7			SCK2-A			
22		PB6			CRX-A/ RXD2-A			
23		PB5			CTX-A/ TXD2-A			
24	PLLVCC							
25		PB4		GTETRG		IRQ3	POE8#	
26	PLLVSS							
27		PB3		MTIOC0A-A	SCK0			
28		PB2		MTIOC0B-A	TXD0/SDA			
29		PB1		MTIOC0C	RXD0/SCL			
30		PB0		MTIOC0D				
31		PA5	ADTRG1#-A	MTIOC1A				
32		PA3		MTIOC2A				
33	VCC							
34		P96				IRQ4	POE4#	
35	VSS							
36		P95		MTIOC6B				
37		P94		MTIOC7A				
38		P93		MTIOC7B				
39		P92		MTIOC6D				
40		P91		MTIOC7C				
41		P90		MTIOC7D				

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
42		P76		MTIOC4D/ GTIOC2B-A				
43		P75		MTIOC4C/ GTIOC1B-A				
44		P74		MTIOC3D/ GTIOC0B-A				
45		P73		MTIOC4B/ GTIOC2A-A				
46		P72		MTIOC4A/ GTIOC1A-A				
47		P71		MTIOC3B/ GTIOC0A-A				
48		P70				IRQ5	POE0#	
49		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
50		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
51	VCC							
52		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
53	VSS							
54		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
55		P24			RSPCK-A			
56		P23			CTX-B/ LTX/ MOSI-A			
57		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
58		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
59	AVCC							
60	AVSS							
61		P63	AN3					
62		P62	AN2					
63		P61	AN1					
64		P60	AN0					
65		P47	AN103/ CVREFH					
66		P46	AN102					
67		P45	AN101					
68		P44	AN100					
69		P43	AN003/ CVREFL					
70		P42	AN002					
71		P41	AN001					
72		P40	AN000					
73	AVCC0							
74	VREFH0							
75	VREFL0							

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.
Set INTB to a multiple of four.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

Table 4.1 List of I/O Registers (Address Order) (6 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 71BEh	ICU	DTC activation enable register 190	DTCER190	8	8	2 ICLK
0008 71C0h	ICU	DTC activation enable register 192	DTCER192	8	8	2 ICLK
0008 71C1h	ICU	DTC activation enable register 193	DTCER193	8	8	2 ICLK
0008 71C2h	ICU	DTC activation enable register 194	DTCER194	8	8	2 ICLK
0008 71C3h	ICU	DTC activation enable register 195	DTCER195	8	8	2 ICLK
0008 71C4h	ICU	DTC activation enable register 196	DTCER196	8	8	2 ICLK
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2 ICLK
0008 71D8h	ICU	DTC activation enable register 216	DTCER216	8	8	2 ICLK
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8	2 ICLK
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK
0008 71FEh	ICU	DTC activation enable register 254	DTCER254	8	8	2 ICLK
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK
0008 7300h	ICU	Interrupt source priority register 00	IPR00	8	8	2 ICLK
0008 7301h	ICU	Interrupt source priority register 01	IPR01	8	8	2 ICLK
0008 7302h	ICU	Interrupt source priority register 02	IPR02	8	8	2 ICLK
0008 7303h	ICU	Interrupt source priority register 03	IPR03	8	8	2 ICLK
0008 7304h	ICU	Interrupt source priority register 04	IPR04	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8048h	ADA	A/D data register E	ADDRE	16	16	2, 3 PCLK*3
0008 804Ah	ADA	A/D data register F	ADDRF	16	16	2, 3 PCLK*3
0008 804Ch	ADA	A/D data register G	ADDRG	16	16	2, 3 PCLK*3
0008 804Eh	ADA	A/D data register H	ADDRH	16	16	2, 3 PCLK*3
0008 8050h	ADA	A/D control/status register	ADCSR	8	8	2, 3 PCLK*3
0008 8051h	ADA	A/D control register	ADCR	8	8	2, 3 PCLK*3
0008 805Bh	ADA	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 805Dh	ADA	A/D self-diagnostic register	ADDIAGR	8	8	2, 3 PCLK*3
0008 8060h	ADA	A/D data register I	ADDRI	16	16	2, 3 PCLK*3
0008 8062h	ADA	A/D data register J	ADDRJ	16	16	2, 3 PCLK*3
0008 8064h	ADA	A/D data register K	ADDRK	16	16	2, 3 PCLK*3
0008 8066h	ADA	A/D data register L	ADDRL	16	16	2, 3 PCLK*3
0008 8070h	ADA	A/D start trigger select register	ADSTRGR	8	8	2, 3 PCLK*3
0008 8072h	ADA	A/D data placement register	ADDPR	8	8	2, 3 PCLK*3
0008 8240h	SCI0	Serial mode register	SMR*1	8	8	2, 3 PCLK*3
0008 8241h	SCI0	Bit rate register	BRR	8	8	2, 3 PCLK*3
0008 8242h	SCI0	Serial control register	SCR*1	8	8	2, 3 PCLK*3
0008 8243h	SCI0	Transmit data register	TDR	8	8	2, 3 PCLK*3
0008 8244h	SCI0	Serial status register	SSR*1	8	8	2, 3 PCLK*3
0008 8245h	SCI0	Receive data register	RDR	8	8	2, 3 PCLK*3
0008 8246h	SCI0	Smart card mode register	SCMR	8	8	2, 3 PCLK*3
0008 8247h	SCI0	Serial extended mode register	SEMR	8	8	2, 3 PCLK*3
0008 8240h	SMCI0	Serial mode register	SMR	8	8	2, 3 PCLK*3
0008 8241h	SMCI0	Bit rate register	BRR	8	8	2, 3 PCLK*3
0008 8242h	SMCI0	Serial control register	SCR	8	8	2, 3 PCLK*3
0008 8243h	SMCI0	Transmit data register	TDR	8	8	2, 3 PCLK*3
0008 8244h	SMCI0	Serial status register	SSR	8	8	2, 3 PCLK*3
0008 8245h	SMCI0	Receive data register	RDR	8	8	2, 3 PCLK*3
0008 8246h	SMCI0	Smart card mode register	SCMR	8	8	2, 3 PCLK*3
0008 8248h	SCI1	Serial mode register	SMR*1	8	8	2, 3 PCLK*3
0008 8249h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLK*3
0008 824Ah	SCI1	Serial control register	SCR*1	8	8	2, 3 PCLK*3
0008 824Bh	SCI1	Transmit data register	TDR	8	8	2, 3 PCLK*3
0008 824Ch	SCI1	Serial status register	SSR*1	8	8	2, 3 PCLK*3
0008 824Dh	SCI1	Receive data register	RDR	8	8	2, 3 PCLK*3
0008 824Eh	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLK*3
0008 824Fh	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLK*3
0008 8248h	SMCI1	Serial mode register	SMR	8	8	2, 3 PCLK*3
0008 8249h	SMCI1	Bit rate register	BRR	8	8	2, 3 PCLK*3
0008 824Ah	SMCI1	Serial control register	SCR	8	8	2, 3 PCLK*3
0008 824Bh	SMCI1	Transmit data register	TDR	8	8	2, 3 PCLK*3
0008 824Ch	SMCI1	Serial status register	SSR	8	8	2, 3 PCLK*3
0008 824Dh	SMCI1	Receive data register	RDR	8	8	2, 3 PCLK*3
0008 824Eh	SMCI1	Smart card mode register	SCMR	8	8	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (21 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 2116h	GPT0	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK*4
000C 2118h	GPT0	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK*4
000C 211Ah	GPT0	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK*4
000C 211Ch	GPT0	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK*4
000C 211Eh	GPT0	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK*4
000C 2120h	GPT0	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK*4
000C 2124h	GPT0	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK*4
000C 2126h	GPT0	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK*4
000C 2128h	GPT0	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK*4
000C 212Ch	GPT0	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK*4
000C 212Eh	GPT0	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK*4
000C 2130h	GPT0	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK*4
000C 2134h	GPT0	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK*4
000C 2136h	GPT0	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK*4
000C 2138h	GPT0	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK*4
000C 213Ah	GPT0	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK*4
000C 213Ch	GPT0	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK*4
000C 213Eh	GPT0	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK*4
000C 2140h	GPT0	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK*4
000C 2142h	GPT0	General PWM timer output protection function temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK*4
000C 2180h	GPT1	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK*4
000C 2182h	GPT1	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK*4
000C 2184h	GPT1	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2186h	GPT1	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK*4
000C 2188h	GPT1	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK*4
000C 218Ah	GPT1	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK*4
000C 218Ch	GPT1	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK*4
000C 218Eh	GPT1	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK*4
000C 2190h	GPT1	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK*4
000C 2192h	GPT1	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK*4
000C 2194h	GPT1	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK*4
000C 2196h	GPT1	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK*4
000C 2198h	GPT1	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK*4
000C 219Ah	GPT1	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK*4
000C 219Ch	GPT1	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK*4
000C 219Eh	GPT1	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK*4

Table 4.1 List of I/O Registers (Address Order) (24 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 22B6h	GPT3	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK*4
000C 22B8h	GPT3	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK*4
000C 22BAh	GPT3	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK*4
000C 22BCh	GPT3	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK*4
000C 22BEh	GPT3	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK*4
000C 22C0h	GPT3	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK*4
000C 22C2h	GPT3	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK*4
000C 2300h	GPT0	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2302h	GPT1	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2304h	GPT2	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2306h	GPT3	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2318h	GPT0	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 231Ah	GPT0	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 231Ch	GPT1	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 231Eh	GPT1	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2320h	GPT2	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 2322h	GPT2	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2324h	GPT3	GTIOCA falling output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 2326h	GPT3	GTIOCB falling output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2328h	GPT0	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 232Ah	GPT0	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 232Ch	GPT1	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 232Eh	GPT1	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 2330h	GPT2	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 2332h	GPT2	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 2334h	GPT3	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 2336h	GPT3	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 PCLK*3
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 PCLK*3
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 PCLK*3
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 PCLK*3
007F C440h	FLASH	Data flash read enable register 0	DFLRE0	16	16	2, 3 PCLK*3
007F C442h	FLASH	Data flash read enable register 1	DFLRE1	16	16	2, 3 PCLK*3
007F C450h	FLASH	Data flash programming/erasure enable register 0	DFLWE0	16	16	2, 3 PCLK*3
007F C452h	FLASH	Data flash programming/erasure enable register 1	DFLWE1	16	16	2, 3 PCLK*3
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 PCLK*3
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 PCLK*3
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 PCLK*3
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 PCLK*3
007F FFB4h	FLASH	Flash protect register	FPROTR	16	16	2, 3 PCLK*3
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 PCLK*3

Table 4.2 List of I/O Registers (Bit Order) (23 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT	GTBDR	BD33	BD32	BD31	BD30	BD23	BD22	BD21	BD20
		BD13	BD12	BD11	BD10	BD03	BD02	BD01	BD00
GPT	GTSWP	—	—	—	—	—	—	—	—
		—	—	—	—	SWP3	SWP2	SWP1	SWP0
GPT	LCCR	LPSC[1:0]		TPSC[1:0]		LCNTAT		LCTO[2:0]	
		—	LCINTO	LCINTD	LCINTC	—	LCNTS	LCNTCR	LCNTE
GPT	LCST	—	—	—	—	—	—	—	—
		—	—	—	—	—	LISO	LISD	LISC
GPT	LCNTA								
GPT	LCNT00								
GPT	LCNT01								
GPT	LCNT02								
GPT	LCNT03								
GPT	LCNT04								
GPT	LCNT05								
GPT	LCNT06								
GPT	LCNT07								
GPT	LCNT08								
GPT	LCNT09								
GPT	LCNT10								
GPT	LCNT11								
GPT	LCNT12								
GPT	LCNT13								
GPT	LCNT14								
GPT	LCNT15								
GPT	LCNTDU								
GPT	LCNTDL								
GPT0	GTIOR	OBHLD	OBDFLT			GTIOB[5:0]			
		OAHLD	OADFLT			GTIOA[5:0]			
GPT0	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA

Table 4.2 List of I/O Registers (Bit Order) (26 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT1	GTADTBRB								
GPT1	GTADTDBRB								
GPT1	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
		NFS[3:0]				NVB	NVA	NEB	NEA
GPT1	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT1	GTDVU								
GPT1	GTDVD								
GPT1	GTDBU								
GPT1	GTDBD								
GPT1	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	
GPT1	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT2	GTIOR	OBHLD	OBDFLT	GTIOB[5:0]					
		OAHLD	OADFLT	GTIOA[5:0]					
GPT2	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA
GPT2	GTCR	—	—	CCLR[1:0]		—	—	TPCS[1:0]	
		—	—	—	—	—	MD[2:0]		
GPT2	GTBER	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]	
		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
GPT2	GTUDC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	UDF	UD
GPT2	GTITC	—	ADTBL	—	ADTAL	—	IVTT[2:0]		
		IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
GPT2	GTST	TUCF	—	—	—	DTEF	ITCNT[2:0]		
		TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
GPT2	GTCNT								
GPT2	GTCCRA								
GPT2	GTCCRB								
GPT2	GTCCRC								
GPT2	GTCCRD								
GPT2	GTCCRE								
GPT2	GTCCRF								
GPT2	GTPR								

Table 4.2 List of I/O Registers (Bit Order) (30 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
FLASH	FSTATR0	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	—	ERSSPD	PRGSPD
FLASH	FSTATR1	FCUERR	—	—	FLOCKST	—	—	—	—
FLASH	FENTRYR	FEKEY[7:0]							
		FENTRYD	—	—	—	—	—	—	FENTRY0
FLASH	FPROTR	FPKEY[7:0]							
		—	—	—	—	—	—	—	FPROTCN
FLASH	FRESETR	FRKEY[7:0]							
		—	—	—	—	—	—	—	FRESET
FLASH	FCMDR	CMDR[7:0]							
		PCMDR[7:0]							
FLASH	FCPSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	ESUSPMD
FLASH	DFLBCCNT	—	—	—	—	—		BCADR[7:0]	
		BCADR[7:0]						—	BCSIZE
FLASH	FPESTAT	—	—	—	—	—	—	—	—
		PEERRST[7:0]							
FLASH	DFLBCSTAT	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	BCST
FLASH	PCKAR	—	—	—	—	—	—	—	—
		PCKA[7:0]							

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.

Table 5.3 DC Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	In operation	Max.*2	I_{CC}*3	-	-	70	mA	ICLK = 100 MHz PCLK = 50 MHz
		Normal*4		-	35	-		
		Increased by BGO operation*5		-	15	-		
	Sleep				22	60		
	All-module-clock-stop mode*6				14	28		
	Standby mode	Software standby mode		-	0.10	3	mA	
		Deep software standby mode		-	20	60	µA	
Analog power supply current	During 12-bit A/D conversion (when a sample-and-hold circuit is in use; per unit)		AI_{CC0}	-	3	5	mA	
	During 12-bit A/D conversion (when a sample-and-hold circuit is not in use; per unit)			-	3	5	mA	
	Programmable gain amp (per channel)			-	1	2	mA	
	Window comparator (1 channel)				0.5	1	mA	
	Window comparator (6 channels)			-	1	2	mA	
	During 12-bit A/D conversion (per unit)			-	60	90	µA	
	During 10-bit A/D conversion (per unit)		AI_{CC}	-	0.9	2	mA	
	Waiting for 10-bit A/D conversion (all units)			-	0.3	3	µA	
Reference power supply current	During 12-bit A/D conversion (per unit)		AI_{REFH0}	-	1.6	3	mA	
	Waiting for 12-bit A/D conversion (all units)			-	1.6	3	mA	
	During 10-bit A/D conversion (per unit)		AI_{REF}	-	0.1	1	mA	
	Waiting for 10-bit A/D conversion (all units)			-	0.1	3	µA	
VCC rising gradient			SV_{CC}	-	-	20	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max. = 0.54 x f + 16 (max.)
ICC max. = 0.3 x f + 5 (normal operation)
ICC max. = 0.44 x f + 16 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
Note 6. The values are for reference.

5.3 AC Characteristics

Table 5.6 Operation Frequency Value

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f	8	-	100	MHz
	Peripheral module clock (PCLK)		8	-	50	

5.3.1 Clock Timing

Table 5.7 Clock Timing

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Oscillation settling time after reset (crystal)	t_{OSC1}	10	-	ms	Figure 5.1
Oscillation settling time after leaving software standby mode (crystal)	t_{OSC2}	10	-	ms	Figure 5.2
Oscillation settling time after leaving deep software standby mode (crystal)	t_{OSC3}	10	-	ms	Figure 5.3
EXTAL external clock output delay settling time	t_{DEXT}	1	-	ms	Figure 5.1
EXTAL external clock input low pulse width	t_{EXL}	35	-	ns	Figure 5.4
EXTAL external clock input high pulse width	t_{EXH}	35	-	ns	
EXTAL external clock rising time	t_{EXr}	-	5	ns	
EXTAL external clock falling time	t_{EXf}	-	5	ns	
On-chip oscillator (IWDTCLK) oscillation frequency	$f_{IWDTCLK}$	62.5	187.5	kHz	

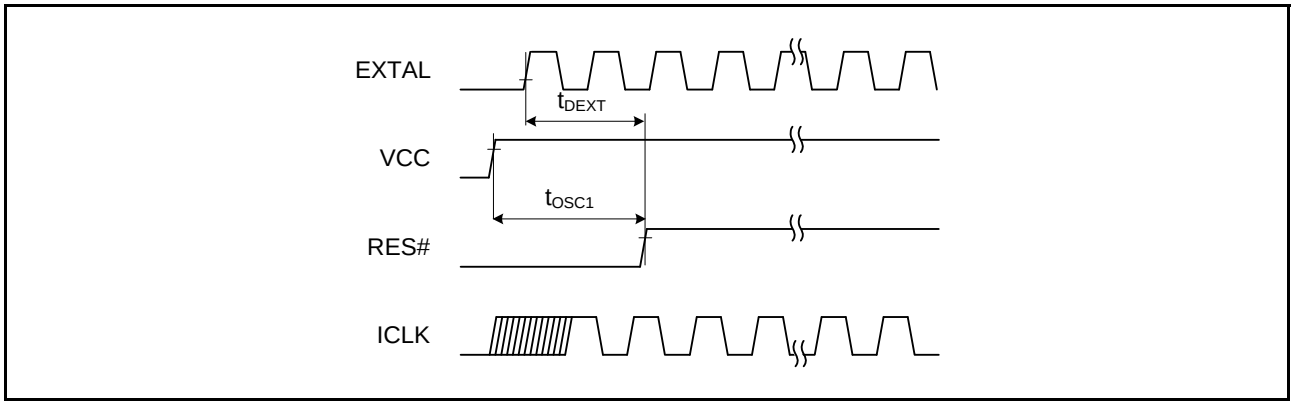

Figure 5.1 Oscillation Settling Timing

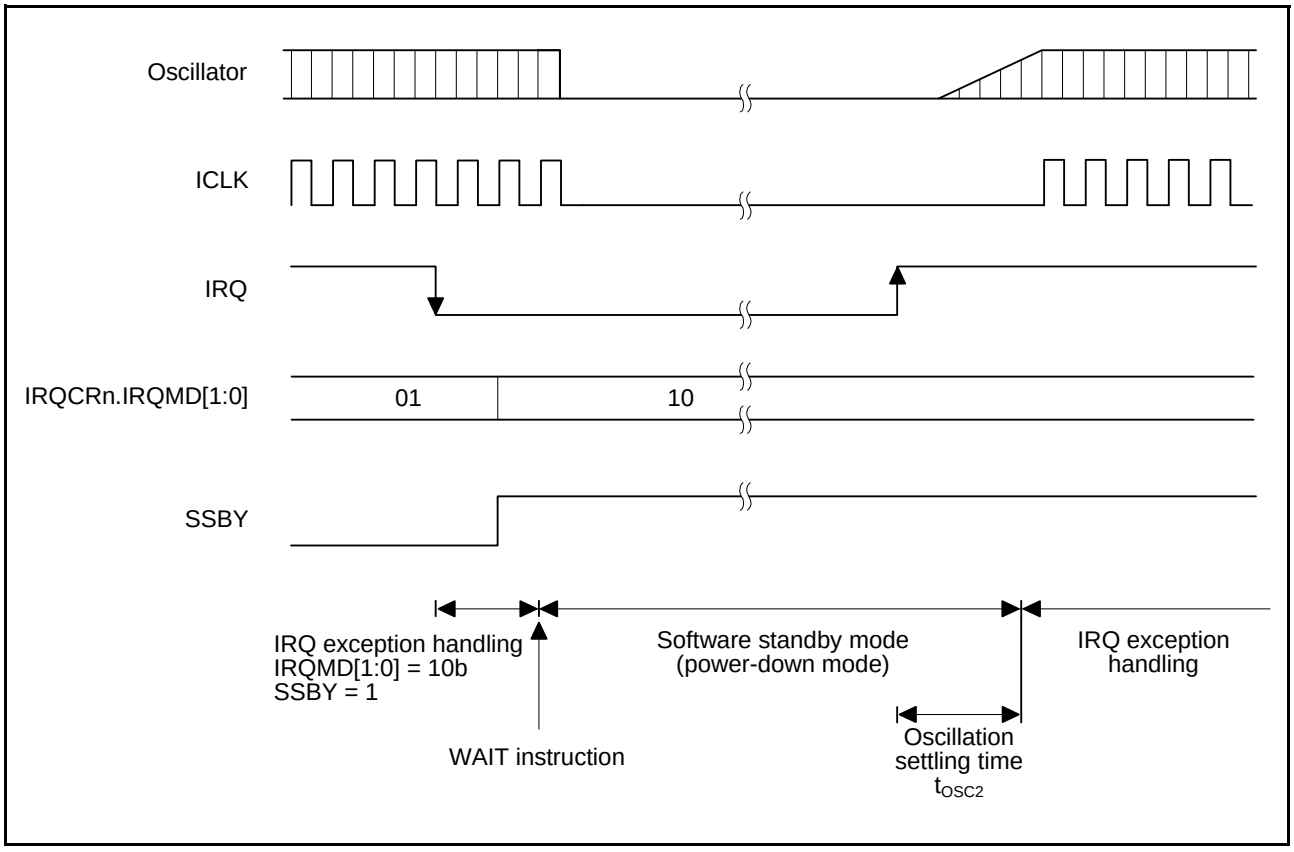

Figure 5.2 Oscillation Settling Timing after Software Standby Mode

Table 5.17 Characteristics of the Programmable Gain Amplifier

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		Cin	-	-	6	pF	
Input offset voltage		Voff	-	-	8	mV	
Input voltage range (Vin)	Gain × 2.000	Vin	0.050 x AVcc	-	0.450 x AVcc	V	
	Gain × 2.500		0.047 x AVcc	-	0.360 x AVcc		
	Gain × 3.077		0.045 x AVcc	-	0.292 x AVcc		
	Gain × 3.636		0.042 x AVcc	-	0.247 x AVcc		
	Gain × 4.000		0.040 x AVcc	-	0.212 x AVcc		
	Gain × 4.444		0.036 x AVcc	-	0.191 x AVcc		
	Gain × 5.000		0.033 x AVcc	-	0.170 x AVcc		
	Gain × 5.714		0.031 x AVcc	-	0.148 x AVcc		
	Gain × 6.667		0.029 x AVcc	-	0.127 x AVcc		
	Gain × 10.000		0.025 x AVcc	-	0.08 x AVcc		
	Gain × 13.333		0.023 x AVcc	-	0.06 x AVcc		
Slew rate		SR	10	-	-	V/µs	
Gain error	Gain × 2.000	-	-	-	1	%	
	Gain × 2.500		-	-	1		
	Gain × 3.077		-	-	1		
	Gain × 3.636		-	-	1.5		
	Gain × 4.000		-	-	1.5		
	Gain × 4.444		-	-	2		
	Gain × 5.000		-	-	2		
	Gain × 5.714		-	-	2		
	Gain × 6.667		-	-	3		
	Gain × 10.000		-	-	4		
	Gain × 13.333		-	-	4		

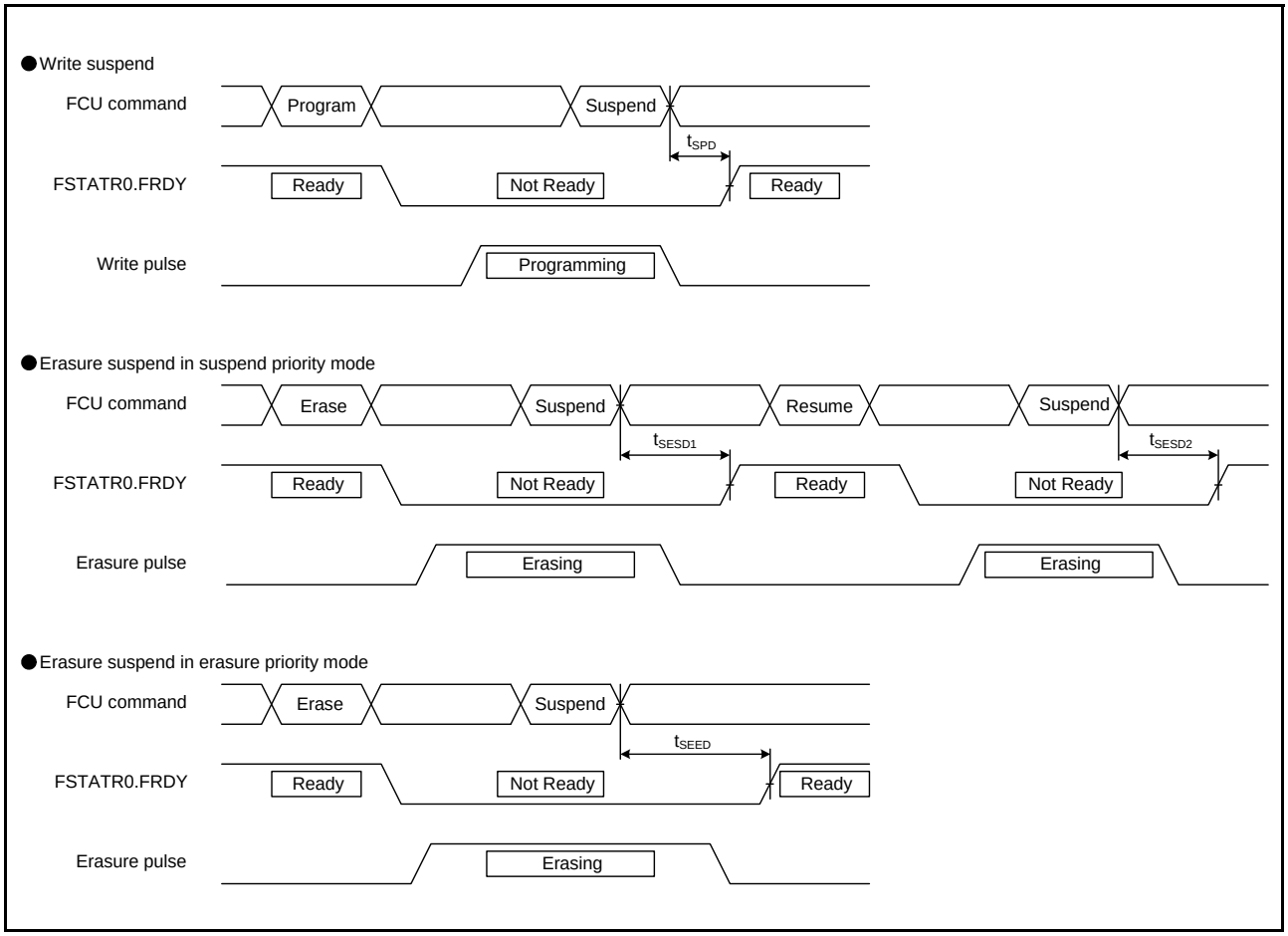

Figure 5.24 Flash Memory Write/Erase Suspend Timing

Rev.	Date	Description	
		Page	Summary
2.00	Jan 10, 2014	98	Table 5.1 Absolute Maximum Ratings, changed
		102	Table 5.3 DC Characteristics (2): Note 3, changed
		103	Table 5.5 Permissible Power Consumption, added
		117	5.3.4 Timing of PWM Delay Generation Circuit, added
		117	Table 5.14 Timing of the PWM Delay Generation Circuit, added
		120	Table 5.17 Characteristics of the Programmable Gain Amplifier, changed
		125	Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1), changed
		125	Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2), added
		126	Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1), changed
		126	Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2), added