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Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I ² C, SPI |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 22 |
| Program Memory Size | 3.5KB (2K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 64 x 8 |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 5x10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 28-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f872-e-so |

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PIC16F872

TABLE 1-2: PIC16F872 PINOUT DESCRIPTION (CONTINUED)

| Pin Name | Pin# | I/O/P Type | Buffer Type | Description |
|--|-------|------------|-----------------------|--|
| RB0/INT RB0 INT | 21 | I/O | TTL/ST ⁽¹⁾ | PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. Digital I/O. External interrupt pin. |
| RB1 | 22 | I/O | TTL | Digital I/O. |
| RB2 | 23 | I/O | TTL | Digital I/O. |
| RB3/PGM RB3 PGM | 24 | I/O | TTL | Digital I/O. Low voltage ICSP programming enable pin. |
| RB4 | 25 | I/O | TTL | Digital I/O. |
| RB5 | 26 | I/O | TTL | Digital I/O. |
| RB6/PGC RB6 PGC | 27 | I/O | TTL/ST ⁽²⁾ | Digital I/O. In-Circuit Debugger and ICSP programming clock. |
| RB7/PGD RB7 PGD | 28 | I/O | TTL/ST ⁽²⁾ | Digital I/O. In-Circuit Debugger and ICSP programming data. |
| RC0/T1OSO/T1CKI RC0 T1OSO T1CKI | 11 | I/O | ST | PORTC is a bi-directional I/O port. Digital I/O. Timer1 oscillator output. Timer1 clock input. |
| RC1/T1OSI RC1 T1OSI | 12 | I/O | ST | Digital I/O. Timer1 oscillator input. |
| RC2/CCP1 RC2 CCP1 | 13 | I/O | ST | Digital I/O. Capture1 input/Compare1 output/PWM1 output. |
| RC3/SCK/SCL RC3 SCK SCL | 14 | I/O | ST | Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C mode. |
| RC4/SDI/SDA RC4 SDI SDA | 15 | I/O | ST | Digital I/O. SPI Data In pin (SPI mode). SPI Data I/O pin (I ² C mode). |
| RC5/SDO RC5 SDO | 16 | I/O | ST | Digital I/O. SPI Data Out pin (SPI mode). |
| RC6 | 17 | I/O | ST | Digital I/O. |
| RC7 | 18 | I/O | ST | Digital I/O. |
| VSS | 8, 19 | P | — | Ground reference for logic and I/O pins. |
| VDD | 20 | P | — | Positive supply for logic and I/O pins. |

Legend: I = input O = output I/O = input/output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

PIC16F872

2.2.2.3 INTCON Register

The INTCON Register is a readable and writable register, which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON REGISTER (ADDRESS: 0Bh, 8Bh, 10Bh, 18Bh)

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-x |
|-------|-------|--------|-------|-------|--------|-------|-------|
| GIE | PEIE | TMR0IE | INTE | RBIE | TMR0IF | INTF | RBIF |
| bit 7 | | | | | | | bit 0 |

- bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts
- bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
- bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt
- bit 4 **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt
- bit 3 **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt
- bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow
- bit 1 **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur
- bit 0 **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared (must be cleared in software).
0 = None of the RB7:RB4 pins have changed state

Legend:

| | | |
|--------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

3.0 DATA EEPROM AND FLASH PROGRAM MEMORY

The Data EEPROM and FLASH Program Memory are readable and writable during normal operation over the entire VDD range. These operations take place on a single byte for Data EEPROM memory and a single word for Program memory. A write operation causes an erase-then-write operation to take place on the specified byte or word. A bulk erase operation may not be issued from user code (which includes removing code protection).

Access to program memory allows for checksum calculation. The values written to Program memory do not need to be valid instructions. Therefore, numbers of up to 14 bits can be stored in memory for use as calibration parameters, serial numbers, packed 7-bit ASCII, etc. Executing a program memory location, containing data that forms an invalid instruction, results in the execution of a NOP instruction.

The EEPROM Data memory is rated for high erase/write cycles (specification #D120). The FLASH Program memory is rated much lower (specification #D130) because EEPROM Data memory can be used to store frequently updated values. An on-chip timer controls the write time and it will vary with voltage and temperature, as well as from chip to chip. Please refer to the specifications for exact limits (specifications #D122 and #D133).

A byte or word write automatically erases the location and writes the new value (erase before write). Writing to EEPROM Data memory does not impact the operation of the device. Writing to Program memory will cease the execution of instructions until the write is complete. The program memory cannot be accessed during the write. During the write operation, the oscillator continues to run, the peripherals continue to function and interrupt events will be detected and essentially "queued" until the write is complete. When the write completes, the next instruction in the pipeline is executed and the branch to the interrupt vector will take place if the interrupt is enabled and occurred during the write.

Read and write access to both memories take place indirectly through a set of Special Function Registers (SFR). The six SFRs used are:

- EEDATA
- EEDATH
- EEADR
- EEADRH
- EECON1
- EECON2

The EEPROM Data memory allows byte read and write operations without interfering with the normal operation of the microcontroller. When interfacing to EEPROM Data memory, the EEADR register holds the address to be accessed. Depending on the operation, the EEDATA register holds the data to be written or the data read at the address in EEADR. The PIC16F872 has 64 bytes of EEPROM Data memory and therefore, requires that the two Most Significant bits of EEADR remain clear. EEPROM Data memory on these devices wraps around to 0 (i.e., 40h in the EEADR maps to 00h).

The FLASH Program memory allows non-intrusive read access, but write operations cause the device to stop executing instructions until the write completes. When interfacing to the Program memory, the EEADRH:EEADR registers pair forms a two-byte word which holds the 13-bit address of the memory location being accessed. The EEDATH:EEDATA register pair holds the 14-bit data for writes or reflects the value of program memory after a read operation. Just as in EEPROM Data memory accesses, the value of the EEADRH:EEADR registers must be within the valid range of program memory, depending on the device (0000h to 07FFh). Addresses outside of this range wrap around to 0000h (i.e., 0800h maps to 0000h).

3.1 EECON1 and EECON2 Registers

The EECON1 register is the control register for configuring and initiating the access. The EECON2 register is not a physically implemented register, but is used exclusively in the memory write sequence to prevent inadvertent writes.

There are many bits used to control the read and write operations to EEPROM Data and FLASH Program memory. The EEPGD bit determines if the access will be a program or data memory access. When clear, any subsequent operations will work on the EEPROM Data memory. When set, all subsequent operations will operate in the Program memory.

Read operations only use one additional bit, RD, which initiates the read operation from the desired memory location. Once this bit is set, the value of the desired memory location will be available in the data registers. This bit cannot be cleared by firmware. It is automatically cleared at the end of the read operation. For EEPROM Data memory reads, the data will be available in the EEDATA register in the very next instruction cycle after the RD bit is set. For program memory reads, the data will be loaded into the EEDATH:EEDATA registers, following the second instruction after the RD bit is set.

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|-----------------------|------------|------------------------|--------|--------|-------|-------|--------|-------|-------|--------------------------|---------------------------------|
| 01h,101h | TMR0 | Timer0 Module Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 0Bh,8Bh, 10Bh,18Bh | INTCON | GIE | PEIE | TMR0IE | INTE | RBIE | TMR0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 81h,181h | OPTION_REG | RBPU | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'.
Shaded cells are not used by Timer0.

7.0 TIMER2 MODULE

Timer2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time-base for the PWM mode of the CCP module(s). The TMR2 register is readable and writable, and is cleared on any device RESET.

The input clock ($F_{osc}/4$) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon RESET.

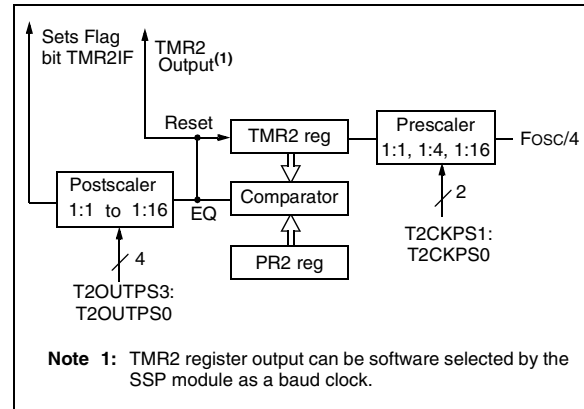
The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit, TMR2IF (PIR1<1>)).

Timer2 can be shut-off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Register 7-1 shows the Timer2 Control register.

Additional information on timer modules is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).

FIGURE 7-1: TIMER2 BLOCK DIAGRAM



REGISTER 7-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|---------|---------|---------|---------|--------|---------|---------|
| — | TOUTPS3 | TOUTPS2 | TOUTPS1 | TOUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 |
| bit 7 | | | | | | | bit 0 |

- bit 7 **Unimplemented:** Read as '0'
- bit 6-3 **TOUTPS3:TOUTPS0:** Timer2 Output Postscale Select bits
 0000 = 1:1 Postscale
 0001 = 1:2 Postscale
 0010 = 1:3 Postscale
 •
 •
 •
 1111 = 1:16 Postscale
- bit 2 **TMR2ON:** Timer2 On bit
 1 = Timer2 is on
 0 = Timer2 is off
- bit 1-0 **T2CKPS1:T2CKPS0:** Timer2 Clock Prescale Select bits
 00 = Prescaler is 1
 01 = Prescaler is 4
 1x = Prescaler is 16

Legend:

| | | |
|--------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

PIC16F872

NOTES:

REGISTER 9-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS: 14h)

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 |

bit 7

bit 0

bit 7 **WCOL**: Write Collision Detect bit

Master mode:

1 = A write to SSPBUF was attempted while the I²C conditions were not valid

0 = No collision

Slave mode:

1 = SSPBUF register is written while still transmitting the previous word (must be cleared in software)

0 = No collision

bit 6 **SSPOV**: Receive Overflow Indicator bit

In SPI mode:

1 = A new byte is received while SSPBUF holds previous data. Data in SSPSR is lost on overflow. In Slave mode, the user must read the SSPBUF, even if only transmitting data, to avoid overflows. In Master mode, the overflow bit is not set since each operation is initiated by writing to the SSPBUF register. (Must be cleared in software.)

0 = No overflow

In I²C mode:

1 = A byte is received while the SSPBUF is holding the previous byte. SSPOV is a "don't care" in Transmit mode. (Must be cleared in software.)

0 = No overflow

bit 5 **SSPEN**: Synchronous Serial Port Enable bit

In SPI mode:

When enabled, these pins must be properly configured as input or output.

1 = Enables serial port and configures SCK, SDO, SDI, and \overline{SS} as the source of the serial port pins

0 = Disables serial port and configures these pins as I/O port pins

In I²C mode:

When enabled, these pins must be properly configured as input or output.

1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins

0 = Disables serial port and configures these pins as I/O port pins

bit 4 **CKP**: Clock Polarity Select bit

In SPI mode:

1 = IDLE state for clock is a high level

0 = IDLE state for clock is a low level

In I²C slave mode:

SCK release control

1 = Enable clock

0 = Holds clock low (clock stretch). (Used to ensure data setup time.)

In I²C master mode:

Unused in this mode

bit 3-0 **SSPM3:SSPM0**: Synchronous Serial Port Mode Select bits

0000 = SPI Master mode, clock = Fosc/4

0001 = SPI Master mode, clock = Fosc/16

0010 = SPI Master mode, clock = Fosc/64

0011 = SPI Master mode, clock = TMR2 output/2

0100 = SPI Slave mode, clock = SCK pin. \overline{SS} pin control enabled.

0101 = SPI Slave mode, clock = SCK pin. \overline{SS} pin control disabled. \overline{SS} can be used as I/O pin.

0110 = I²C Slave mode, 7-bit address

0111 = I²C Slave mode, 10-bit address

1000 = I²C Master mode, clock = Fosc / (4 * (SSPADD+1))

1011 = I²C Firmware Controlled Master mode (slave idle)

1110 = I²C Firmware Controlled Master mode, 7-bit address with START and STOP bit interrupts enabled

1111 = I²C Firmware Controlled Master mode, 10-bit address with START and STOP bit interrupts enabled

1001, 1010, 1100, 1101 = reserved

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

There are certain conditions that will cause the MSSP module not to give this $\overline{\text{ACK}}$ pulse. These are if either (or both):

- a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- b) The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

If the BF bit is set, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF and SSPOV are set. Table 9-2 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low time for proper operation. The high and low times of the I²C specification, as well as the requirement of the MSSP module, is shown in timing parameter #100 and parameter #101 of the electrical specifications.

9.2.1.1 Addressing

Once the MSSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- a) The SSPSR register value is loaded into the SSPBUF register on the falling edge of the 8th SCL pulse.
- b) The buffer full bit, BF, is set on the falling edge of the 8th SCL pulse.
- c) An $\overline{\text{ACK}}$ pulse is generated.
- d) SSP interrupt flag bit, SSPIF (PIR1<3>), is set (interrupt is generated if enabled) on the falling edge of the 9th SCL pulse.

In 10-bit Address mode, two address bytes need to be received by the slave. The five Most Significant bits (MSBs) of the first address byte specify if this is a 10-bit address. Bit R/W (SSPSTAT<2>) must specify a write, so the slave device will receive the second address byte. For a 10-bit address the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSBs of the address. The sequence of events for a 10-bit address is as follows, with steps 7-9 for slave transmitter:

1. Receive first (high) byte of Address (bits SSPIF, BF and UA (SSPSTAT<1>) are set).
2. Update the SSPADD register with the second (low) byte of Address (clears bit UA and releases the SCL line).
3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
4. Receive second (low) byte of Address (bits SSPIF, BF and UA are set).
5. Update the SSPADD register with the first (high) byte of Address. This will clear bit UA and release the SCL line.
6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
7. Receive Repeated START condition.
8. Receive first (high) byte of Address (bits SSPIF and BF are set).
9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

Note: Following the Repeated START condition (step 7) in 10-bit mode, the user only needs to match the first 7-bit address. The user does not update the SSPADD for the second half of the address.

9.2.1.2 Slave Reception

When the R/W bit of the address byte is clear and an address match occurs, the R/W bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no Acknowledge ($\overline{\text{ACK}}$) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set, or bit SSPOV (SSPCON<6>) is set. This is an error condition due to user firmware.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the received byte.

Note: The SSPBUF will be loaded if the SSPOV bit is set and the BF flag is cleared. If a read of the SSPBUF was performed, but the user did not clear the state of the SSPOV bit before the next receive occurred, the $\overline{\text{ACK}}$ is not sent and the SSPBUF is updated.

PIC16F872

9.2.7 I²C MASTER MODE SUPPORT

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON and by setting the SSPEN bit. Once Master mode is enabled, the user has six options.

- Assert a START condition on SDA and SCL.
- Assert a Repeated START condition on SDA and SCL.
- Write to the SSPBUF register, initiating transmission of data/address.
- Generate a STOP condition on SDA and SCL.
- Configure the I²C port to receive data.
- Generate an Acknowledge condition at the end of a received byte of data.

Note: The MSSP module, when configured in I²C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a START condition and immediately write the SSPBUF register to initiate transmission, before the START condition is complete. In this case, the SSPBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

9.2.7.1 I²C Master Mode Operation

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since the Repeated START condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic '0'. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/W bit. In this case, the R/W bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. START and STOP conditions indicate the beginning and end of transmission.

The baud rate generator used for SPI mode operation is now used to set the SCL clock frequency for either 100 kHz, 400 kHz or 1 MHz I²C operation. The baud rate generator reload value is contained in the lower 7 bits of the SSPADD register. The baud rate generator

will automatically begin counting on a write to the SSPBUF. Once the given operation is complete (i.e., transmission of the last data bit is followed by ACK) the internal clock will automatically stop counting and the SCL pin will remain in its last state

A typical transmit sequence would go as follows:

- a) The user generates a Start Condition by setting the START enable bit (SEN) in SSPCON2.
- b) SSPIF is set. The module will wait the required start time before any other operation takes place.
- c) The user loads the SSPBUF with address to transmit.
- d) Address is shifted out the SDA pin until all 8 bits are transmitted.
- e) The MSSP module shifts in the ACK bit from the slave device and writes its value into the SSPCON2 register (SSPCON2<6>).
- f) The module generates an interrupt at the end of the ninth clock cycle by setting SSPIF.
- g) The user loads the SSPBUF with eight bits of data.
- h) DATA is shifted out the SDA pin until all 8 bits are transmitted.
- i) The MSSP module shifts in the ACK bit from the slave device, and writes its value into the SSPCON2 register (SSPCON2<6>).
- j) The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
- k) The user generates a STOP condition by setting the STOP enable bit PEN in SSPCON2.
- l) Interrupt is generated once the STOP condition is complete.

9.2.8 BAUD RATE GENERATOR

In I²C Master mode, the reload value for the BRG is located in the lower 7 bits of the SSPADD register (Figure 9-10). When the BRG is loaded with this value, the BRG counts down to 0 and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (Tcy), on the Q2 and Q4 clock.

In I²C Master mode, the BRG is reloaded automatically. If Clock Arbitration is taking place, for instance, the BRG will be reloaded when the SCL pin is sampled high (Figure 9-11).

FIGURE 9-10: BAUD RATE GENERATOR BLOCK DIAGRAM

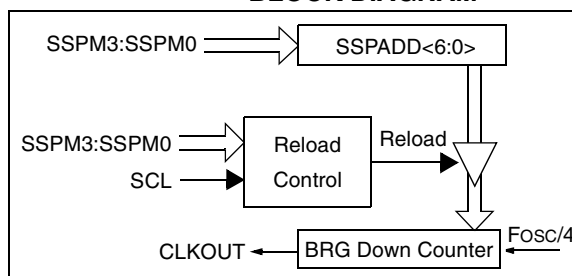


FIGURE 9-14: I²C MASTER MODE TIMING (TRANSMISSION, 7 OR 10-BIT ADDRESS)

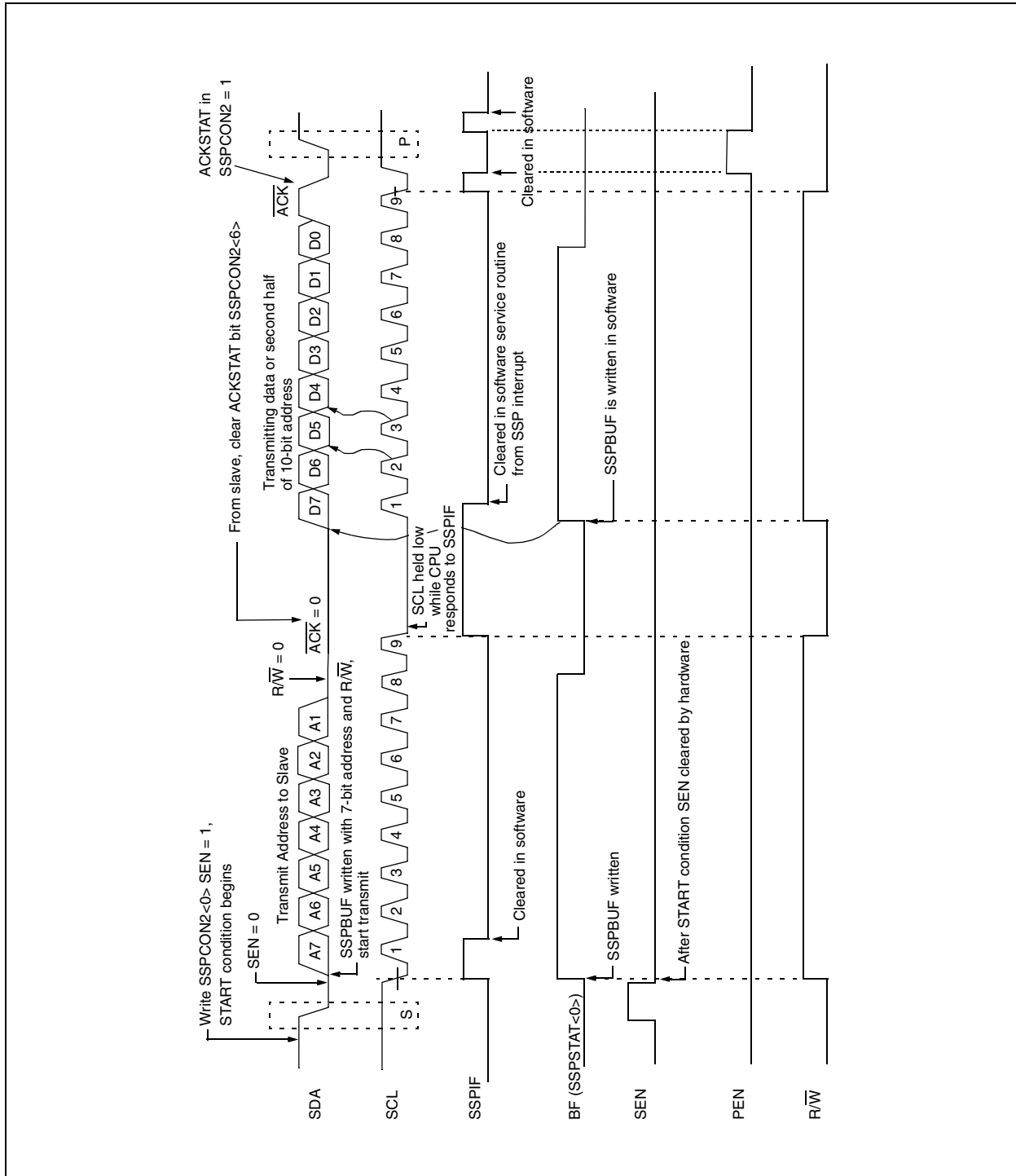


FIGURE 11-5: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD} VIA RC NETWORK)

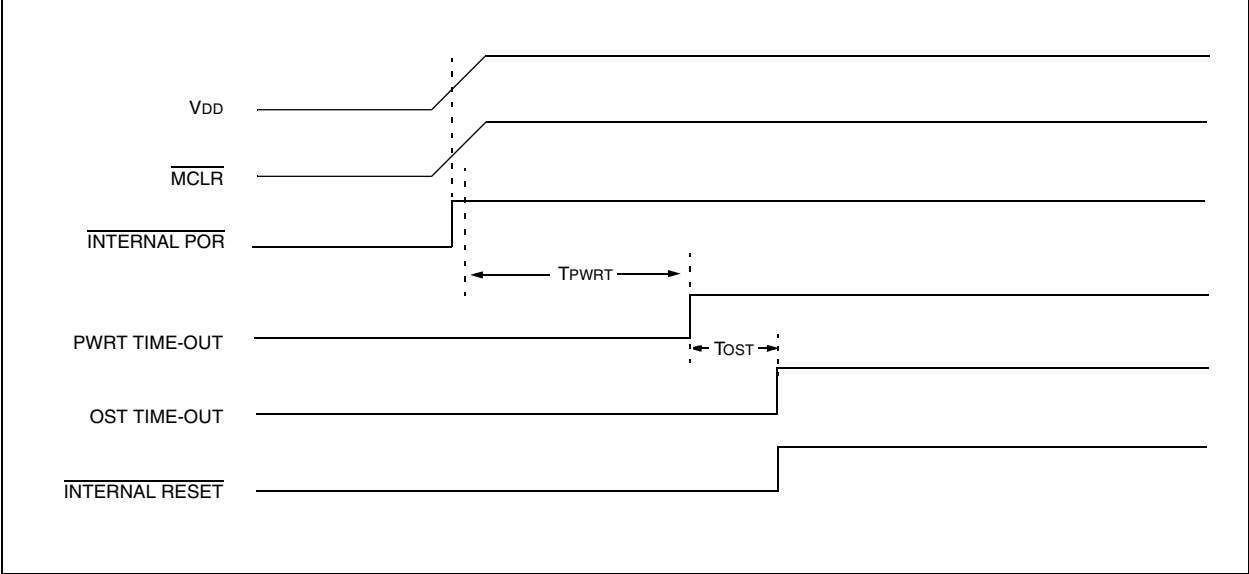
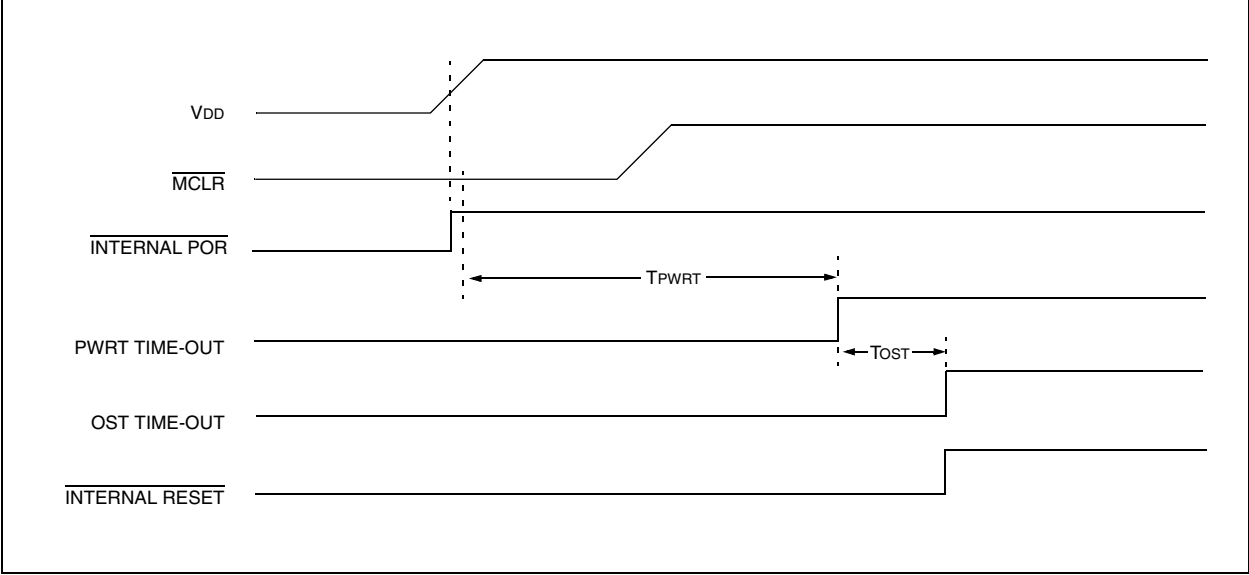


FIGURE 11-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1



11.13 Power-down Mode (SLEEP)

Power-down mode is entered by executing a `SLEEP` instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{PD} bit (`STATUS<3>`) is cleared, the \overline{TO} (`STATUS<4>`) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the `SLEEP` instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either V_{DD} or V_{SS} , ensure no external circuitry is drawing current from the I/O pin, power-down the A/D and disable external clocks. Pull all I/O pins that are hi-impedance inputs, high or low externally, to avoid switching currents caused by floating inputs. The `T0CKI` input should also be at V_{DD} or V_{SS} for lowest current consumption. The contribution from on-chip pull-ups on `PORTB` should also be considered.

The \overline{MCLR} pin must be at a logic high level (V_{IHMC}).

11.13.1 WAKE-UP FROM SLEEP

The device can wake-up from `SLEEP` through one of the following events:

1. External `RESET` input on \overline{MCLR} pin.
2. Watchdog Timer wake-up (if `WDT` was enabled).
3. Interrupt from `INT` pin, `RB` port change or Peripheral Interrupt.

External \overline{MCLR} Reset will cause a device `RESET`. All other events are considered a continuation of program execution and cause a "wake-up". The \overline{TO} and \overline{PD} bits in the `STATUS` register can be used to determine the cause of device `RESET`. The \overline{PD} bit, which is set on power-up, is cleared when `SLEEP` is invoked. The \overline{TO} bit is cleared if a `WDT` time-out occurred and caused wake-up.

The following peripheral interrupts can wake the device from `SLEEP`:

1. `PSP` read or write.
2. `TMR1` interrupt. Timer1 must be operating as an asynchronous counter.
3. `CCP` Capture mode interrupt.
4. Special event trigger (Timer1 in Asynchronous mode using an external clock).
5. `SSP` (`START/STOP`) bit detect interrupt.
6. `SSP` transmit or receive in Slave mode (`SPI/I2C`).
7. `USART` `RX` or `TX` (Synchronous Slave mode).
8. A/D conversion (when A/D clock source is `RC`).
9. `EEPROM` write operation completion.

Other peripherals cannot generate interrupts, since during `SLEEP`, no on-chip clocks are present.

When the `SLEEP` instruction is being executed, the next instruction (`PC + 1`) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the `GIE` bit. If the `GIE` bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the `GIE` bit is set (enabled), the device executes the instruction after the `SLEEP` instruction and then branches to the interrupt address (`0004h`). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

11.13.2 WAKE-UP USING INTERRUPTS

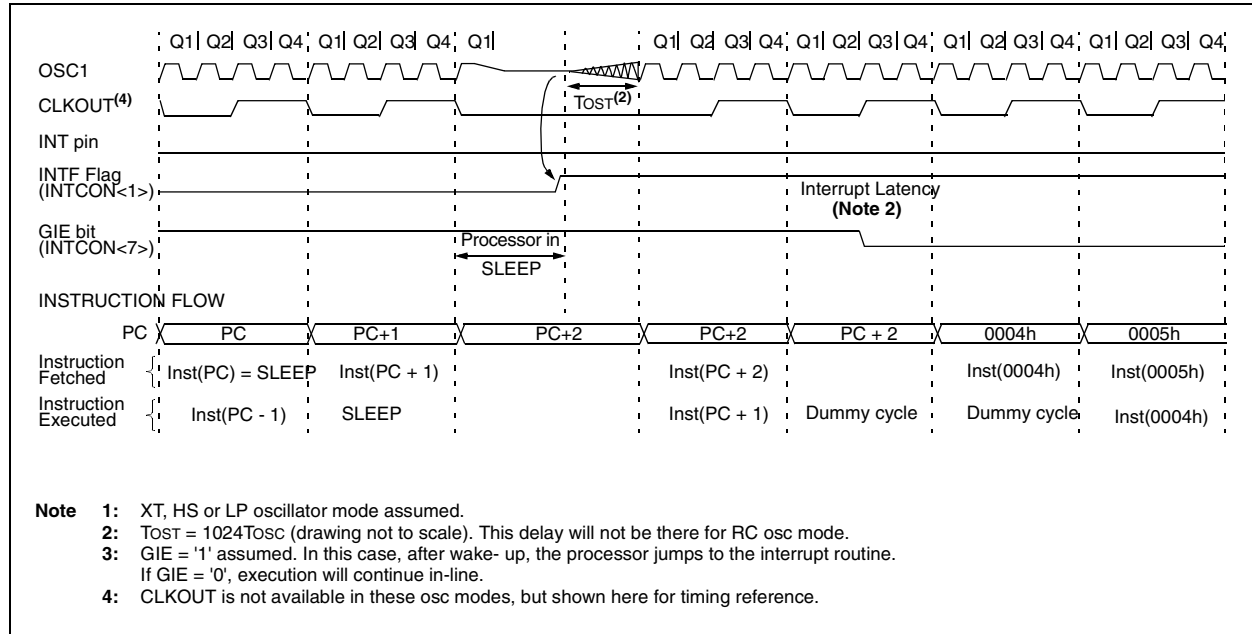
When global interrupts are disabled (`GIE` cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a `SLEEP` instruction, the `SLEEP` instruction will complete as a `NOP`. Therefore, the `WDT` and `WDT` postscaler will not be cleared, the \overline{TO} bit will not be set and \overline{PD} bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a `SLEEP` instruction, the device will immediately wake-up from `SLEEP`. The `SLEEP` instruction will be completely executed before the wake-up. Therefore, the `WDT` and `WDT` postscaler will be cleared, the \overline{TO} bit will be set and the \overline{PD} bit will be cleared.

Even if the flag bits were checked before executing a `SLEEP` instruction, it may be possible for flag bits to become set before the `SLEEP` instruction completes. To determine whether a `SLEEP` instruction executed, test the \overline{PD} bit. If the \overline{PD} bit is set, the `SLEEP` instruction was executed as a `NOP`.

To ensure that the `WDT` is cleared, a `CLRWDT` instruction should be executed before a `SLEEP` instruction.

FIGURE 11-11: WAKE-UP FROM SLEEP THROUGH INTERRUPT



11.14 In-Circuit Debugger

When the DEBUG bit in the configuration word is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB® IDE. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 11-8 shows which features are consumed by the background debugger.

TABLE 11-8: DEBUGGER RESOURCES

| | |
|----------------|--|
| I/O pins | RB6, RB7 |
| Stack | 1 level |
| Program Memory | Address 0000h must be NOP Last 100h words |
| Data Memory | 0x070 (0x0F0, 0x170, 0x1F0) 0x1EB - 0x1EF |

To use the In-Circuit Debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to MCLR/VPP, VDD, GND, RB7 and RB6. This will interface to the In-Circuit Debugger module available from Microchip or one of the third party development tool companies.

11.15 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

11.16 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during program/verify. It is recommended that only the 4 Least Significant bits of the ID location are used.

PIC16F872

SWAPF **Swap Nibbles in f**

Syntax: `[label] SWAPF f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (\text{destination}<7:4>)$,
 $(f<7:4>) \rightarrow (\text{destination}<3:0>)$

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed in register 'f'.

XORWF **Exclusive OR W with f**

Syntax: `[label] XORWF f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(W) .XOR. (f) \rightarrow (\text{destination})$

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

XORLW **Exclusive OR Literal with W**

Syntax: `[label] XORLW k`

Operands: $0 \leq k \leq 255$

Operation: $(W) .XOR. k \rightarrow (W)$

Status Affected: Z

Description: The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

TABLE 13-1: DEVELOPMENT TOOLS FROM MICROCHIP

| | PIC12CXXXX | PIC14000 | PIC16C5X | PIC16C6X | PIC16CXXXX | PIC16F62X | PIC16C7X | PIC16C7XX | PIC16C8X | PIC16F8XX | PIC16C9XX | PIC17C4X | PIC17C7XX | PIC18CXX2 | PIC18FXXXX | 24CXX/ 25CXX/ 93CXX | HC5XX | MCRFXX | MCP2510 |
|---------------------------|---|----------|----------|----------|------------|-----------|----------|-----------|----------|-----------|-----------|----------|-----------|-----------|------------|---------------------------|-------|--------|---------|
| Software Tools | MPLAB® Integrated Development Environment | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | MPLAB® C17 C Compiler | | | | | | | | | | | ✓ | | | | | | | |
| | MPLAB® C18 C Compiler | | | | | | | | | | | | | ✓ | ✓ | | | | |
| Emulators | MPASM™ Assembler/ MPLINK™ Object Linker | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | MPLAB® ICE In-Circuit Emulator | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | ICEPIC™ In-Circuit Emulator | ✓ | | ✓ | ✓ | | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| Debugger | MPLAB® ICD In-Circuit Debugger | | | | ✓ | | ✓ | | | ✓ | | | | | ✓ | | | | |
| Programmers | PICSTART® Plus Entry Level Development Programmer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | PRO MATE® II Universal Device Programmer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| Demo Boards and Eval Kits | PICDEM™ 1 Demonstration Board | | ✓ | | | | † | | ✓ | | | ✓ | | | | | | | |
| | PICDEM™ 2 Demonstration Board | | | | † | | † | | | | | | | ✓ | ✓ | | | | |
| | PICDEM™ 3 Demonstration Board | | | | | | | | | | ✓ | | | | | | | | |
| | PICDEM™ 14A Demonstration Board | ✓ | | | | | | | | | | | | | | | | | |
| | PICDEM™ 17 Demonstration Board | | | | | | | | | | | | ✓ | | | | | | |
| | KEELOQ® Evaluation Kit | | | | | | | | | | | | | | | | ✓ | | |
| | KEELOQ® Transponder Kit | | | | | | | | | | | | | | | | ✓ | | |
| | microID™ Programmer's Kit | | | | | | | | | | | | | | | | | ✓ | |
| | 125 kHz microID™ Developer's Kit | | | | | | | | | | | | | | | | | ✓ | |
| | 125 kHz Anticollision microID™ Developer's Kit | | | | | | | | | | | | | | | | | ✓ | |
| | 13.56 MHz Anticollision microID™ Developer's Kit | | | | | | | | | | | | | | | | | ✓ | |
| | MCP2510 CAN Developer's Kit | | | | | | | | | | | | | | | | | ✓ | ✓ |

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

PIC16F872

14.5 Timing Parameter Symbolology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I²C specifications only)
4. Ts (I²C specifications only)

| T | | T | |
|---|-----------|---|------|
| F | Frequency | T | Time |

Lowercase letters (pp) and their meanings:

| | | | |
|-----------|-------------------|-----|------------------------------------|
| pp | | | |
| cc | CCP1 | osc | OSC1 |
| ck | CLKOUT | rd | \overline{RD} |
| cs | \overline{CS} | rw | \overline{RD} or \overline{WR} |
| di | SDI | sc | SCK |
| do | SDO | ss | \overline{SS} |
| dt | Data in | t0 | T0CKI |
| io | I/O port | t1 | T1CKI |
| mc | \overline{MCLR} | wr | \overline{WR} |

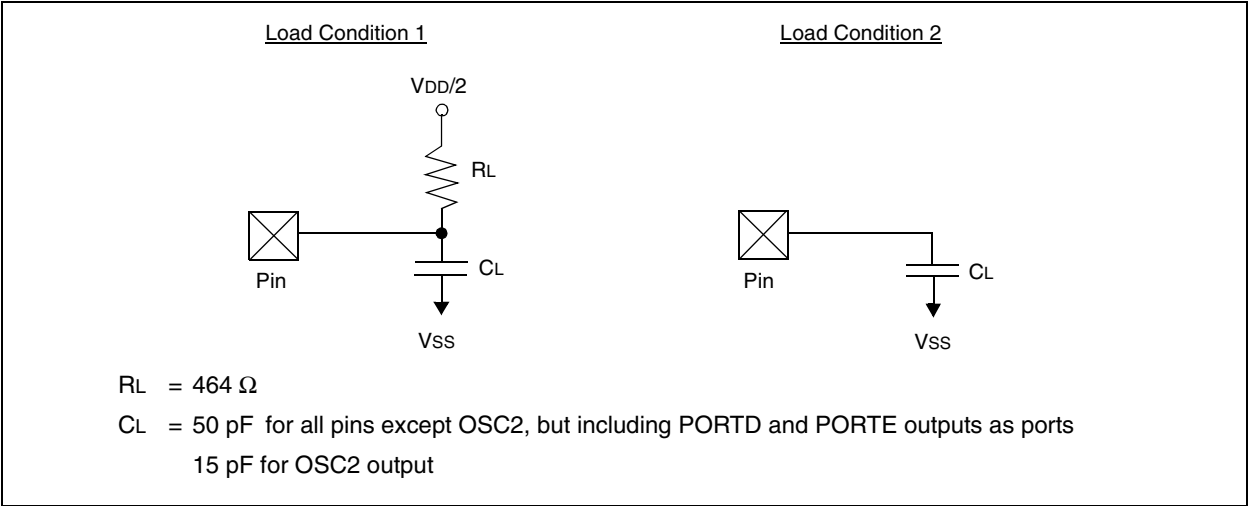
Uppercase letters and their meanings:

| | | | |
|----------------------------|------------------------|------|--------------|
| S | | P | Period |
| F | Fall | R | Rise |
| H | High | V | Valid |
| I | Invalid (Hi-impedance) | Z | Hi-impedance |
| L | Low | | |
| I²C only | | High | High |
| AA | output access | Low | Low |
| BUF | Bus free | | |

TCC:ST (I²C specifications only)

| | | | |
|-----------|-----------------|-----|----------------|
| CC | | SU | Setup |
| HD | Hold | | |
| ST | | STO | STOP condition |
| DAT | DATA input hold | | |
| STA | START condition | | |

FIGURE 14-3: LOAD CONDITIONS



PIC16F872

TABLE 14-6: SPI MODE REQUIREMENTS

| Param No. | Symbol | Characteristic | | Min | Typ† | Max | Units | Conditions |
|-----------|-----------------------|---|-----------------------------|-------------------------|----------|-----------|----------|------------|
| 70* | TssL2scH, TssL2scL | $\overline{SS}\downarrow$ to SCK \downarrow or SCK \uparrow Input | | T _{CY} | — | — | ns | |
| 71* | TscH | SCK Input High Time (Slave mode) | | T _{CY} + 20 | — | — | ns | |
| 72* | TscL | SCK Input Low Time (Slave mode) | | T _{CY} + 20 | — | — | ns | |
| 73* | TdiV2scH, TdiV2scL | Setup Time of SDI Data Input to SCK Edge | | 100 | — | — | ns | |
| 74* | Tsch2diL, TscL2diL | Hold Time of SDI Data Input to SCK Edge | | 100 | — | — | ns | |
| 75* | TdoR | SDO Data Output Rise Time | Standard(F) Extended(LF) | — — | 10 25 | 25 50 | ns ns | |
| 76* | TdoF | SDO Data Output Fall Time | | — | 10 | 25 | ns | |
| 77* | TssH2doZ | $\overline{SS}\uparrow$ to SDO Output Hi-Impedance | | 10 | — | 50 | ns | |
| 78* | TscR | SCK Output Rise Time (Master mode) | Standard(F) Extended(LF) | — — | 10 25 | 25 50 | ns ns | |
| 79* | TscF | SCK Output Fall Time (Master mode) | | — | 10 | 25 | ns | |
| 80* | Tsch2doV, TscL2doV | SDO Data Output Valid after SCK Edge | Standard(F) Extended(LF) | — — | — — | 50 145 | ns | |
| 81* | TdoV2scH, TdoV2scL | SDO Data Output Setup to SCK Edge | | T _{CY} | — | — | ns | |
| 82* | TssL2doV | SDO Data Output Valid after $\overline{SS}\downarrow$ Edge | | — | — | 50 | ns | |
| 83* | Tsch2ssH, TscL2ssH | $\overline{SS}\uparrow$ after SCK Edge | | 1.5T _{CY} + 40 | — | — | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-14: I²C BUS START/STOP BITS TIMING

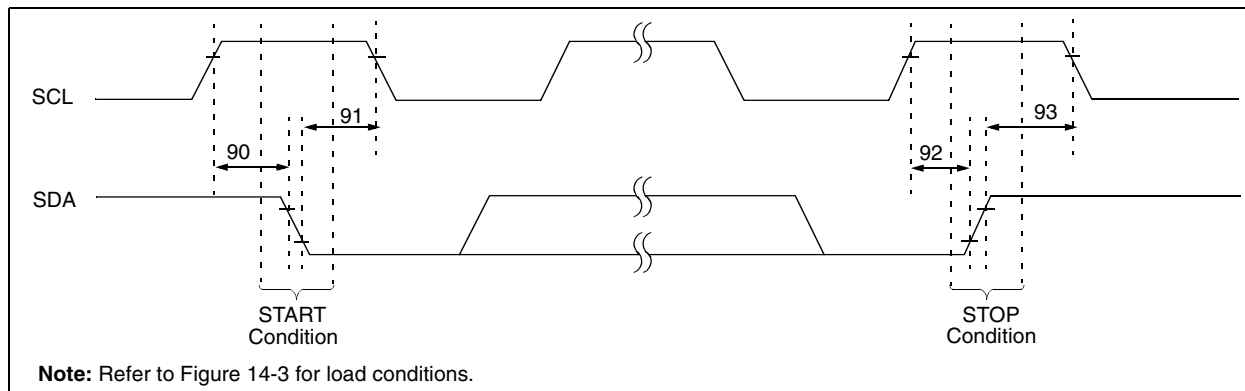


TABLE 14-7: I²C BUS START/STOP BITS REQUIREMENTS

| Parameter No. | Symbol | Characteristic | | Min | Typ | Max | Units | Conditions |
|---------------|---------|-----------------|--------------|------|-----|-----|-------|---|
| 90 | TSU:STA | START condition | 100 kHz mode | 4700 | — | — | ns | Only relevant for Repeated START condition |
| | | Setup time | 400 kHz mode | 600 | — | — | | |
| 91 | THD:STA | START condition | 100 kHz mode | 4000 | — | — | ns | After this period, the first clock pulse is generated |
| | | Hold time | 400 kHz mode | 600 | — | — | | |
| 92 | TSU:STO | STOP condition | 100 kHz mode | 4700 | — | — | ns | |
| | | Setup time | 400 kHz mode | 600 | — | — | | |
| 93 | THD:STO | STOP condition | 100 kHz mode | 4000 | — | — | ns | |
| | | Hold time | 400 kHz mode | 600 | — | — | | |

15.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3 σ) or (mean - 3 σ) respectively, where σ is a standard deviation, over the whole temperature range.

FIGURE 15-1: TYPICAL I_{DD} vs. F_{osc} OVER V_{DD} (HS MODE)

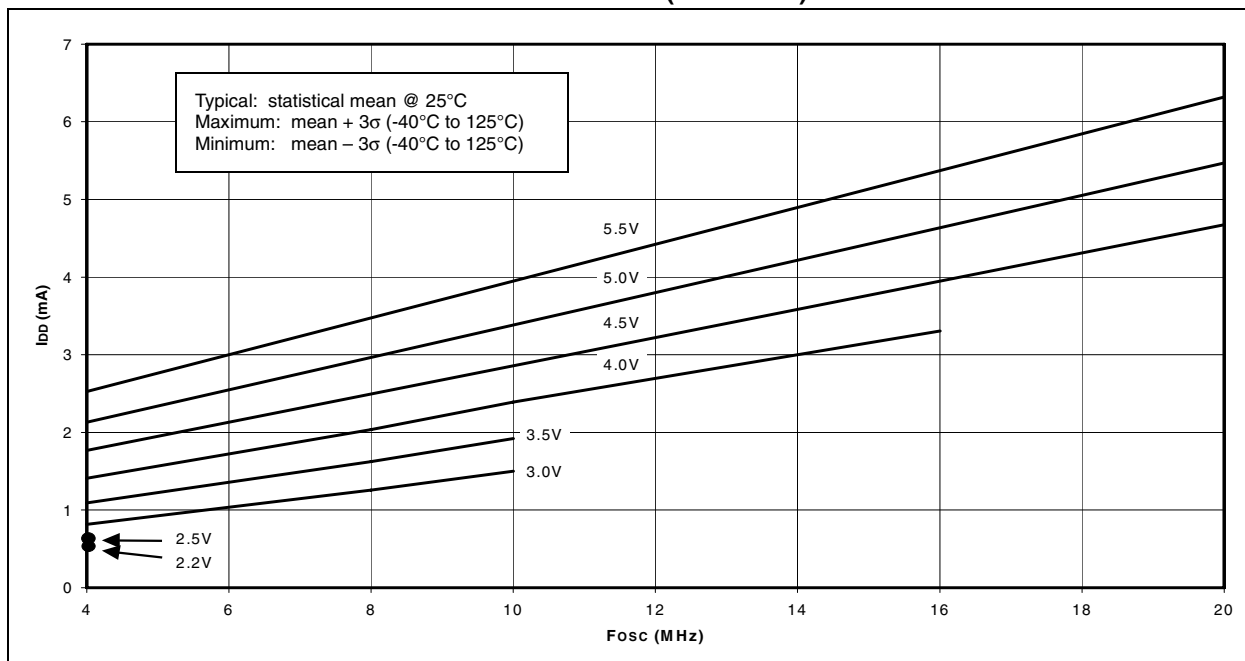
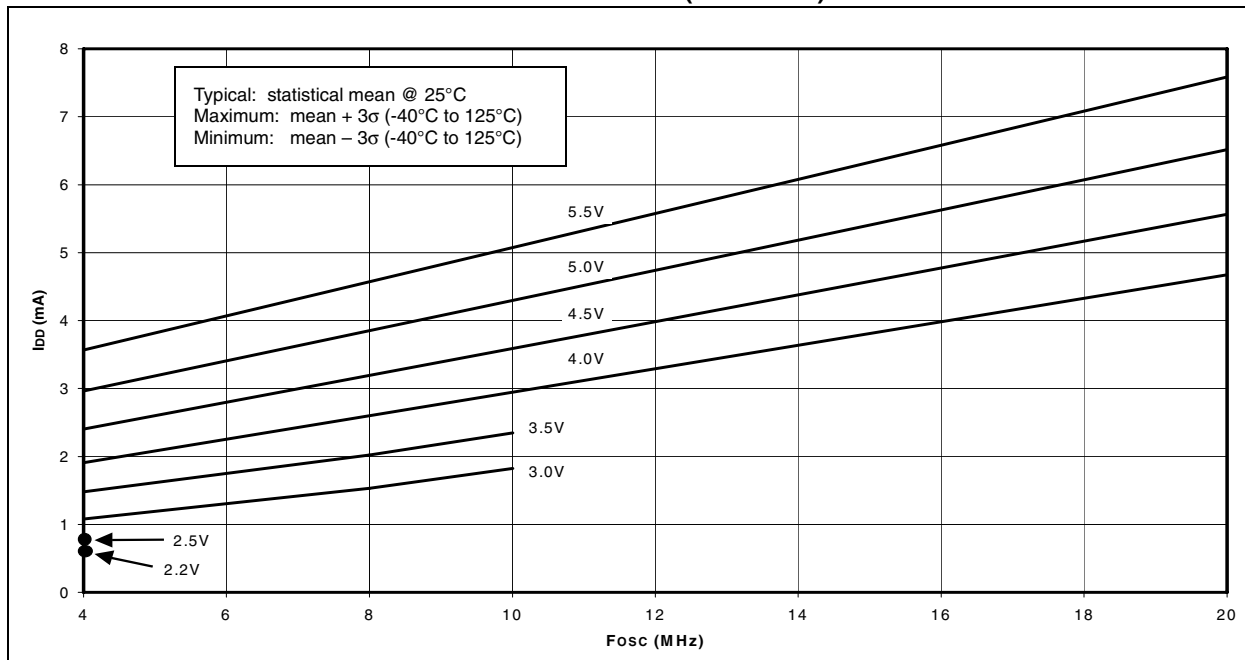


FIGURE 15-2: MAXIMUM I_{DD} vs. F_{osc} OVER V_{DD} (HS MODE)



PIC16F872

| | |
|--|---------|
| Bus Collision During START Condition (SCL = 0) | 75 |
| Bus Collision During START Condition (SDA Only) | 74 |
| Capture/Compare/PWM | 131 |
| CLKOUT and I/O | 128 |
| External Clock | 127 |
| First START Bit Timing | 65 |
| I ² C Bus Data | 135 |
| I ² C Bus START/STOP Bits | 134 |
| I ² C Master Mode Transmission | 68 |
| I ² C Mode (7-bit Reception) | 60, 70 |
| I ² C Mode (7-bit Transmission) | 61 |
| Master Mode Transmit Clock Arbitration | 72 |
| Power-up Timer | 129 |
| Repeat START Condition | 66 |
| RESET | 129 |
| Slave Mode General Call Address Sequence (7 or 10-bit Mode) | 61 |
| Slow Rise Time (MCLR Tied to VDD Via RC Network) | 96 |
| SPI Master Mode | 56 |
| SPI Master Mode (CKE = 0, SMP = 0) | 132 |
| SPI Master Mode (CKE = 1, SMP = 1) | 132 |
| SPI Slave Mode (CKE = 0) | 57, 133 |
| SPI Slave Mode (CKE = 1) | 57, 133 |
| Start-up Timer | 129 |
| STOP Condition Receive or Transmit Mode | 72 |
| Time-out Sequence on Power-up | 96 |
| Time-out Sequence on Power-up (MCLR Not Tied to VDD) Case 1 | 95 |
| Case 2 | 96 |
| Time-out Sequence on Power-up (MCLR Tied to VDD Via RC Network) | 95 |
| Timer0 | 130 |
| Timer1 | 130 |
| Wake-up from SLEEP via Interrupt | 101 |
| Watchdog Timer | 129 |
| Timing Parameter Symbolology | 126 |
| TMR0 Register | 9, 11 |
| TMR1CS bit | 39 |
| TMR1H Register | 9 |
| TMR1L Register | 9 |
| TMR1ON bit | 39 |
| TMR2 Register | 9 |
| TOUTPS3:TOUTPS0 bits | 43 |
| TRISA Register | 10 |
| TRISB Register | 10 |
| TRISC Register | 10 |

U

| | |
|---|----|
| UA Bit Update Address Bit (UA) | 52 |
|---|----|

W

| | |
|--|----------------|
| Wake-up from SLEEP | 87, 100 |
| Interrupts | 93 |
| MCLR Reset | 93 |
| WDT Reset | 93 |
| Wake-Up Using Interrupts | 100 |
| Watchdog Timer (WDT) | 87, 99 |
| Enable (WDTE Bit) | 99 |
| Postscaler. <i>See</i> Postscaler, WDT | |
| Programming Considerations | 99 |
| RC Oscillator | 99 |
| Time-out Period | 99 |
| WDT Reset, Normal Operation | 91, 93 |
| WDT Reset, SLEEP | 91, 93 |
| WDT Reset, Wake-up | 93 |
| WCOL | 65 |
| WCOL Bit | 53 |
| WCOL Status Flag | 65, 67, 69, 71 |
| Write Collision Detect Bit (WCOL) | 53 |
| Write Verify Data EEPROM and FLASH Program Memory | 27 |
| WWW, On-Line Support | 2 |