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Revision History:	**2001-05**	V2.0
Previous Version:	1999-08	
	1998-02	(Preliminary)
	04.97	(Advance Information)

Page	**Subjects (major changes since last revision)[1)]**
All	Converted to Infineon layout
1	Operating frequency up to 25 MHz
1 et al.	References to Flash removed
1	Timer Unit with three timers
1, 12, 73	On-chip XRAM described
2	Derivative table updated
10	Supply voltage is 5 V
21	Functionality of reduced CAPCOM6 corrected
22f	Timer description improved
29, 30	Sections “Oscillator Watchdog” and “Power Management” added
37	POCON reset values adjusted
41 to 73	Parameter section reworked

1) These changes refer to the last two versions. Version 1998-02 covers OTP and ROM derivatives, while version 1999-08 ist the most recent one.

Controller Area Network (CAN): License of Robert Bosch GmbH

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Pin Configuration
(top view)

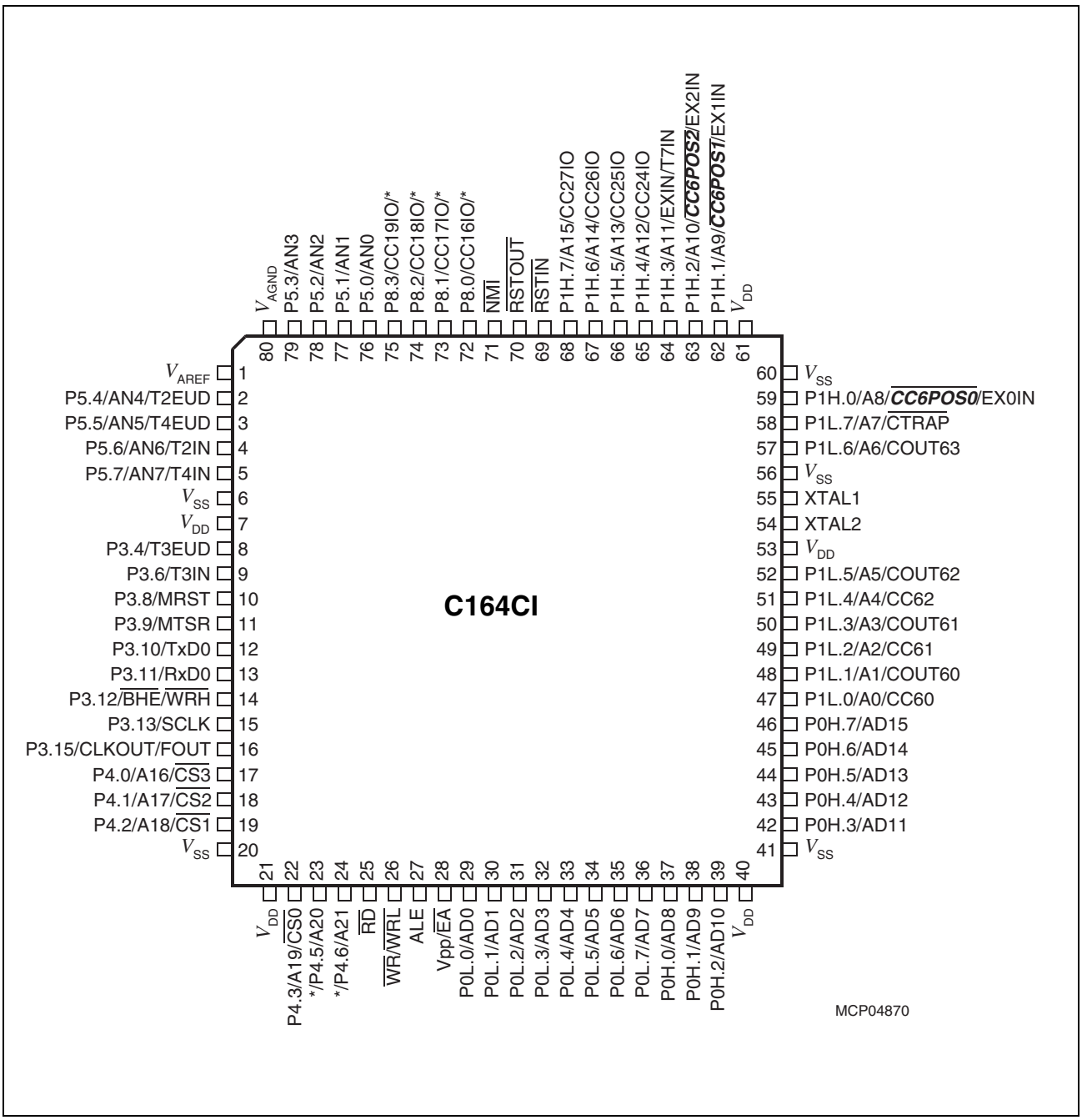


Figure 2

***)** The marked pins of Port 4 and Port 8 can have CAN interface lines assigned to them. **Table 2** on the pages below lists the possible assignments.

The ***marked input signals*** are available only in devices with a full-function CAPCOM6. They are not available in devices with a reduced-function CAPCOM6.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
$\overline{EA}/V_{PP}$	28	I	External Access Enable pin. **A low level** at this pin during and after Reset forces the C164CI to latch the configuration from PORT0 and pin $\overline{RD}$, and to begin instruction execution out of external memory. **A high level** forces the C164CI to latch the configuration from pins $\overline{RD}$ and ALE, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'. *Note: This pin also accepts the programming voltage for the OTP derivatives.*
PORT0 P0L.0-7 P0H.0-7	 29-36 37-39, 42-46	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 – D7 P0H.0 – P0H.7: I/O D8 – D15 **Multiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 – AD7 P0H.0 – P0H.7: A8 – A15 AD8 – AD15

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.
P1L.0-7	47-52, 57-59		
P1H.0-7	59, 62-68		
			The following PORT1 pins also serve for alt. functions:
P1L.0	47	I/O	CC60 CAPCOM6: Input / Output of Channel 0
P1L.1	48	O	COUT60 CAPCOM6: Output of Channel 0
P1L.2	49	I/O	CC61 CAPCOM6: Input / Output of Channel 1
P1L.3	50	O	COUT61 CAPCOM6: Output of Channel 1
P1L.4	51	I/O	CC62 CAPCOM6: Input / Output of Channel 2
P1L.5	52	O	COUT62 CAPCOM6: Output of Channel 2
P1L.6	57	O	COUT63 Output of 10-bit Compare Channel
P1L.7	58	I	$\overline{\text{CTRAP}}$ CAPCOM6: Trap Input $\overline{\text{CTRAP}}$ is an input pin with an internal pullup resistor. A low level on this pin switches the compare outputs of the CAPCOM6 unit to the logic level defined by software.
P1H.0	59	I	$\overline{\text{CC6POS0}}$ CAPCOM6: Position 0 Input, **)
		I	EX0IN Fast External Interrupt 0 Input
P1H.1	62	I	$\overline{\text{CC6POS1}}$ CAPCOM6: Position 1 Input, **)
		I	EX1IN Fast External Interrupt 1 Input
P1H.2	63	I	$\overline{\text{CC6POS2}}$ CAPCOM6: Position 2 Input, **)
		I	EX2IN Fast External Interrupt 2 Input
P1H.3	64	I	EX3IN Fast External Interrupt 3 Input, T7IN CAPCOM2: Timer T7 Count Input
P1H.4	65	I/O	CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	66	I/O	CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	67	I/O	CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	68	I/O	CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.
			Note: The marked (**) input signals are available only in devices with a full function CAPCOM6.

Functional Description

The architecture of the C164CI combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.
The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C164CI.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).

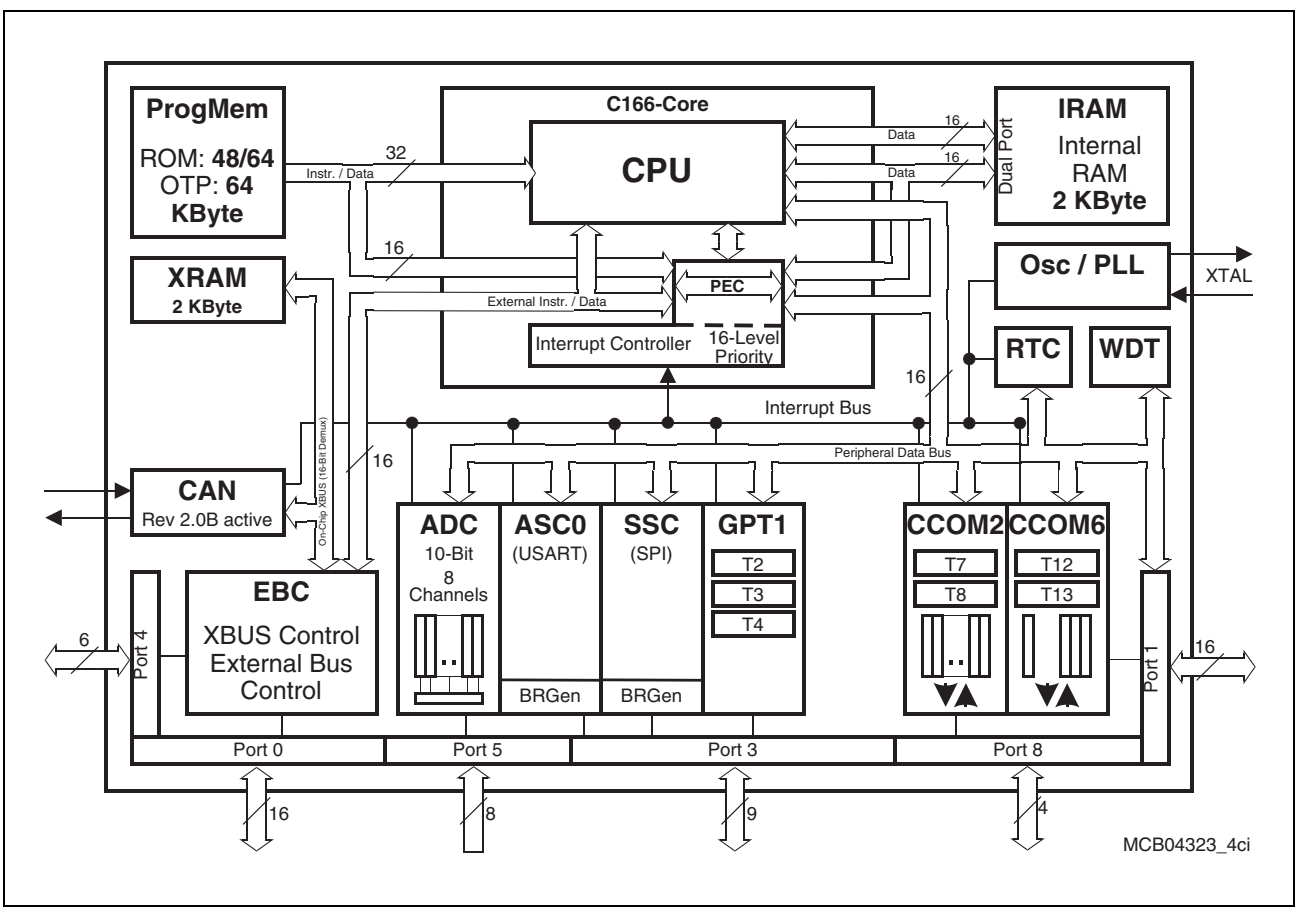


Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resoures, the X-Peripherals (see **Figure 3**).

The XBUS resources (XRAM, CAN) of the C164CI can be enabled or disabled during initialization by setting the general X-Peripheral enable bit XPEN (SYSCON.2). Modules that are disabled consume neither address space nor port pins.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

– 16-/18-/20-/22-bit Addresses, 16-bit Data, Demultiplexed
– 16-/18-/20-/22-bit Addresses, 16-bit Data, Multiplexed
– 16-/18-/20-/22-bit Addresses, 8-bit Data, Multiplexed
– 16-/18-/20-/22-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/ output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 4 external $\overline{CS}$ signals (3 windows plus default) can be generated in order to save external glue logic. The C164CI offers the possibility to switch the $\overline{CS}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{CS}$ signals are directly generated from the address. The unlatched $\overline{CS}$ mode is enabled by setting CSCFG (SYSCON.6).

For applications which require less than 4 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 6 address lines, if an address space of 4 MBytes is used.

Note: When the on-chip CAN Module is used with the interface lines assigned to Port 4, the CAN lines override the segment address lines and the segment address output on Port 4 is therefore limited to 4 bits i.e. address lines A19 … A16.

Table 3 C164CI Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
Fast External Interrupt 0	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
Fast External Interrupt 1	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
Fast External Interrupt 2	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
Fast External Interrupt 3	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
GPT1 Timer 2	T2IR	T2IE	T2INT	$00'0088_H$	22_H
GPT1 Timer 3	T3IR	T3IE	T3INT	$00'008C_H$	23_H
GPT1 Timer 4	T4IR	T4IE	T4INT	$00'0090_H$	24_H
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	$00'00A0_H$	28_H
A/D Overrun Error	ADEIR	ADEIE	ADEINT	$00'00A4_H$	29_H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	$00'00A8_H$	$2A_H$
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	$00'011C_H$	47_H
ASC0 Receive	S0RIR	S0RIE	S0RINT	$00'00AC_H$	$2B_H$
ASC0 Error	S0EIR	S0EIE	S0EINT	$00'00B0_H$	$2C_H$
SSC Transmit	SCTIR	SCTIE	SCTINT	$00'00B4_H$	$2D_H$
SSC Receive	SCRIR	SCRIE	SCRINT	$00'00B8_H$	$2E_H$
SSC Error	SCEIR	SCEIE	SCEINT	$00'00BC_H$	$2F_H$
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	$00'00C0_H$	30_H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	$00'00C4_H$	31_H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	$00'00C8_H$	32_H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	$00'00CC_H$	33_H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	$00'00E0_H$	38_H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	$00'00E4_H$	39_H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	$00'00E8_H$	$3A_H$
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	$00'00EC_H$	$3B_H$
CAPCOM Timer 7	T7IR	T7IE	T7INT	$00'00F4_H$	$3D_H$
CAPCOM Timer 8	T8IR	T8IE	T8INT	$00'00F8_H$	$3E_H$
CAPCOM6 Interrupt	CC6IR	CC6IE	CC6INT	$00'00FC_H$	$3F_H$
CAN Interface 1	XP0IR	XP0IE	XP0INT	$00'0100_H$	40_H
PLL/OWD and RTC	XP3IR	XP3IE	XP3INT	$00'010C_H$	43_H

Table 7 C164CI Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
CC26IC b	$F174_H$ **E**	BA_H	CAPCOM Reg. 26 Interrupt Ctrl. Reg.	0000_H
CC27	$FE76_H$	$3B_H$	CAPCOM Register 27	0000_H
CC27IC b	$F176_H$ **E**	BB_H	CAPCOM Reg. 27 Interrupt Ctrl. Reg.	0000_H
CC28	$FE78_H$	$3C_H$	CAPCOM Register 28	0000_H
CC28IC b	$F178_H$ **E**	BC_H	CAPCOM Reg. 28 Interrupt Ctrl. Reg.	0000_H
CC29	$FE7A_H$	$3D_H$	CAPCOM Register 29	0000_H
CC29IC b	$F184_H$ **E**	$C2_H$	CAPCOM Reg. 29 Interrupt Ctrl. Reg.	0000_H
CC30	$FE7C_H$	$3E_H$	CAPCOM Register 30	0000_H
CC30IC b	$F18C_H$ **E**	$C6_H$	CAPCOM Reg. 30 Interrupt Ctrl. Reg.	0000_H
CC31	$FE7E_H$	$3F_H$	CAPCOM Register 31	0000_H
CC31IC b	$F194_H$ **E**	CA_H	CAPCOM Reg. 31 Interrupt Ctrl. Reg.	0000_H
CC60	$FE30_H$	18_H	CAPCOM 6 Register 0	0000_H
CC61	$FE32_H$	19_H	CAPCOM 6 Register 1	0000_H
CC62	$FE34_H$	$1A_H$	CAPCOM 6 Register 2	0000_H
CC6EIC b	$F188_H$ **E**	$C4_H$	CAPCOM 6 Emergency Interrrupt Control Register	0000_H
CC6CIC b	$F17E_H$ **E**	BF_H	CAPCOM 6 Interrupt Control Register	0000_H
CC6MCON b	$FF32_H$	99_H	CAPCOM 6 Mode Control Register	$00FF_H$
CC6MIC b	$FF36_H$	$9B_H$	CAPCOM 6 Mode Interrupt Ctrl. Reg.	0000_H
CC6MSEL	$F036_H$ **E**	$1B_H$	CAPCOM 6 Mode Select Register	0000_H
CC8IC b	$FF88_H$	$C4_H$	External Interrupt 0 Control Register	0000_H
CC9IC b	$FF8A_H$	$C5_H$	External Interrupt 1 Control Register	0000_H
CCM4 b	$FF22_H$	91_H	CAPCOM Mode Control Register 4	0000_H
CCM5 b	$FF24_H$	92_H	CAPCOM Mode Control Register 5	0000_H
CCM6 b	$FF26_H$	93_H	CAPCOM Mode Control Register 6	0000_H
CCM7 b	$FF28_H$	94_H	CAPCOM Mode Control Register 7	0000_H
CMP13	$FE36_H$	$1B_H$	CAPCOM 6 Timer 13 Compare Reg.	0000_H
CP	$FE10_H$	08_H	CPU Context Pointer Register	$FC00_H$
CSP	$FE08_H$	04_H	CPU Code Segment Pointer Register (8 bits, not directly writeable)	0000_H

Table 7 C164CI Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
CTCON	**b**	$FF30_H$		98_H	CAPCOM 6 Compare Timer Ctrl. Reg.	1010_H
DP0H	**b**	$F102_H$	**E**	81_H	P0H Direction Control Register	00_H
DP0L	**b**	$F100_H$	**E**	80_H	P0L Direction Control Register	00_H
DP1H	**b**	$F106_H$	**E**	83_H	P1H Direction Control Register	00_H
DP1L	**b**	$F104_H$	**E**	82_H	P1L Direction Control Register	00_H
DP3	**b**	$FFC6_H$		$E3_H$	Port 3 Direction Control Register	0000_H
DP4	**b**	$FFCA_H$		$E5_H$	Port 4 Direction Control Register	00_H
DP8	**b**	$FFD6_H$		EB_H	Port 8 Direction Control Register	00_H
DPP0		$FE00_H$		00_H	CPU Data Page Pointer 0 Reg. (10 bits)	0000_H
DPP1		$FE02_H$		01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2		$FE04_H$		02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3		$FE06_H$		03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON	**b**	$F1C0_H$	**E**	$E0_H$	External Interrupt Control Register	0000_H
EXISEL	**b**	$F1DA_H$	**E**	ED_H	External Interrupt Source Select Reg.	0000_H
FOCON	**b**	$FFAA_H$		$D5_H$	Frequency Output Control Register	0000_H
IDCHIP		$F07C_H$	**E**	$3E_H$	Identifier	$XXXX_H$
IDMANUF		$F07E_H$	**E**	$3F_H$	Identifier	1820_H
IDMEM		$F07A_H$	**E**	$3D_H$	Identifier	$XXXX_H$
IDPROG		$F078_H$	**E**	$3C_H$	Identifier	$XXXX_H$
IDMEM2		$F076_H$	**E**	$3B_H$	Identifier	$XXXX_H$
ISNC	**b**	$F1DE_H$	**E**	EF_H	Interrupt Subnode Control Register	0000_H
MDC	**b**	$FF0E_H$		87_H	CPU Multiply Divide Control Register	0000_H
MDH		$FE0C_H$		06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL		$FE0E_H$		07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP3	**b**	$F1C6_H$	**E**	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP4	**b**	$F1CA_H$	**E**	$E5_H$	Port 4 Open Drain Control Register	00_H
ODP8	**b**	$F1D6_H$	**E**	EB_H	Port 8 Open Drain Control Register	00_H
ONES	**b**	$FF1E_H$		$8F_H$	Constant Value 1's Register (read only)	$FFFF_H$
OPAD		$EDC2_H$	**X**	---	OTP Progr. Interface Address Register	0000_H
OPCTRL		$EDC0_H$	**X**	---	OTP Progr. Interface Control Register	0007_H

Absolute Maximum Ratings

Table 8 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100|	mA	–
Power dissipation	P_{DISS}	–	1.5	W	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 10 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)[2]
Strong driver	10 mA	2.5 mA
Medium driver	4.0 mA	1.0 mA
Weak driver	0.5 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

2) The current ROM-version of the C164CI (step Ax) is equipped with port drivers, which provide reduced driving capability and reduced control. Please refer to the actual errata sheet for details.

Power Consumption C164CI (ROM)

(Operating Conditions apply)

Parameter	Sym-bol	Limit Values		Unit	Test Conditions
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD}	–	1 + 2.5 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX}	–	1 + 1.1 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO}[2]	–	500 + 50 × f_{OSC}	µA	$\overline{RSTIN}$ = V_{IH1} f_{OSC} in [MHz][1]
Sleep and Power-down mode supply current with RTC running	I_{PDR}[2]	–	200 + 25 × f_{OSC}	µA	V_{DD} = V_{DDmax} f_{OSC} in [MHz][3]
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	50	µA	V_{DD} = V_{DDmax}[3]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 9**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is determined mainly by the current consumed by the oscillator (see **Figure 8**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

3) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

Power Consumption C164CI (OTP)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD}	–	10 + 3.5 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL} f_{CPU} in [MHz] [1]
Idle mode supply current with all peripherals active	I_{IDX}	–	5 + 1.25 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [1]
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO} [2]	–	500 + 50 × f_{OSC}	µA	$\overline{RSTIN}$ = V_{IH1} f_{OSC} in [MHz] [1]
Sleep and Power-down mode supply current with RTC running	I_{PDR} [2]	–	200 + 25 × f_{OSC}	µA	V_{DD} = V_{DDmax} f_{OSC} in [MHz] [3]
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	50	µA	V_{DD} = V_{DDmax} [3]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is determined mainly by the current consumed by the oscillator (see **Figure 8**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

3) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

P0.15-13 (P0H.7-5). Register RP0H can be loaded from the upper half of register RSTCON under software control.

Table 11 associates the combinations of these three bits with the respective clock generation mode.

Table 11 C164CI Clock Generation Modes

CLKCFG[1] (RP0H.7-5)	CPU Frequency $f_{CPU} = f_{OSC} \times F$	External Clock Input Range[2]	Notes
1 1 1	$f_{OSC} \times 4$	2.5 to 6.25 MHz	Default configuration
1 1 0	$f_{OSC} \times 3$	3.33 to 8.33 MHz	–
1 0 1	$f_{OSC} \times 2$	5 to 12.5 MHz	–
1 0 0	$f_{OSC} \times 5$	2 to 5 MHz	–
0 1 1	$f_{OSC} \times 1$	1 to 25 MHz	Direct drive[3]
0 1 0	$f_{OSC} \times 1.5$	6.66 to 16.66 MHz	–
0 0 1	$f_{OSC} / 2$	2 to 50 MHz	CPU clock via prescaler
0 0 0	$f_{OSC} \times 2.5$	4 to 10 MHz	–

1) Please note that pin P0.15 (corresponding to RP0H.7) is inverted in emulation mode, and thus also in EHM.

2) The external clock input range refers to a CPU clock range of 10 … 25 MHz.

3) The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When prescaler operation is configured (CLKCFG = 001_B) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

When PLL operation is configured (via CLKCFG) the on-chip phase locked loop is enabled and provides the CPU clock (see **Table 11**). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{OSC} \times$ **F**). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

AC Characteristics
External Clock Drive XTAL1
(Operating Conditions apply)

Table 12 External Clock Drive Characteristics

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	40	–	20	–	60[1]	500[1]	ns
High time[2]	t_1	SR	20[3]	–	6	–	10	–	ns
Low time[2]	t_2	SR	20[3]	–	6	–	10	–	ns
Rise time[2]	t_3	SR	–	8	–	5	–	10	ns
Fall time[2]	t_4	SR	–	8	–	5	–	10	ns

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

2) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating freqency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

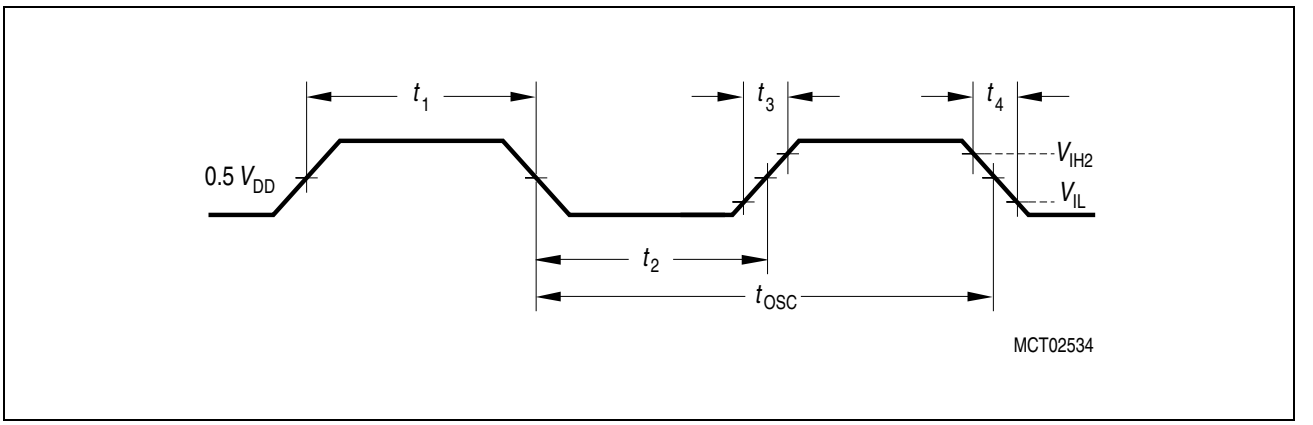


Figure 13 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.
It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

8) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample time t_S depend on programming and can be taken from **Table 14**.

Sample time and conversion time of the C164CI's A/D Converter are programmable. **Table 14** should be used to calculate the above timings.
The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 14 A/D Converter Computation Table

ADCON.15|14 (ADCTC)	A/D Converter Basic Clock f_{BC}	ADCON.13|12 (ADSTC)	Sample time t_S
00	f_{CPU} / 4	00	$t_{BC} \times 8$
01	f_{CPU} / 2	01	$t_{BC} \times 16$
10	f_{CPU} / 16	10	$t_{BC} \times 32$
11	f_{CPU} / 8	11	$t_{BC} \times 64$

Converter Timing Example:

Assumptions: f_{CPU} = 25 MHz (i.e. t_{CPU} = 40 ns), ADCTC = '00', ADSTC = '00'.
Basic clock f_{BC} = f_{CPU}/4 = 6.25 MHz, i.e. t_{BC} = 160 ns.
Sample time t_S = $t_{BC} \times 8$ = 1280 ns.
Conversion time t_C = t_S + 40 t_{BC} + 2 t_{CPU} = (1280 + 6400 + 80) ns = 7.8 µs.

Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 15 Memory Cycle Variables

Description	Symbol	Values
ALE Extension	t_A	TCL × <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL × (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL × (1 - <MTTC>)

Note: Please respect the maximum operating frequency of the respective derivative.

AC Characteristics

Multiplexed Bus

(Operating Conditions apply)
ALE cycle time = 6 TCL + 2t_A + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
Address hold after ALE	t_7	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	26	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns

Multiplexed Bus (cont'd)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A + t_C + t_F$ (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	26 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$[1)]	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In[1)]	t_{39}	SR	–	40 + t_C + $2t_A$	–	3TCL - 20 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$[1)]	t_{40}	CC	46 + t_F	–	3TCL - 14 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns

External XRAM Access

If XPER-Share mode is enabled the on-chip XRAM of the C164CI can be accessed (during hold states) by an external master like an asynchronous SRAM.

Table 16 XRAM Access Timing (Operating Conditions apply)

Parameter		Symbol		Limit Values		Unit
				min.	max.	
Address setup time before $\overline{RD}/\overline{WR}$ falling edge		t_{40}	SR	4	–	ns
Address hold time after $\overline{RD}/\overline{WR}$ rising edge		t_{41}	SR	0	–	ns
Data turn on delay after $\overline{RD}$ falling edge	Read	t_{42}	CC	2	–	ns
Data output valid delay after address latched	Read	t_{43}	CC	–	37	ns
Data turn off delay after $\overline{RD}$ rising edge	Read	t_{44}	CC	0	10	ns
Write data setup time before $\overline{WR}$ rising edge	Write	t_{45}	SR	10	–	ns
Write data hold time after $\overline{WR}$ rising edge	Write	t_{46}	SR	1	–	ns
$\overline{WR}$ pulse width	Write	t_{47}	SR	18	–	ns
$\overline{WR}$ signal recovery time	Write	t_{48}	SR	t_{40}	–	ns

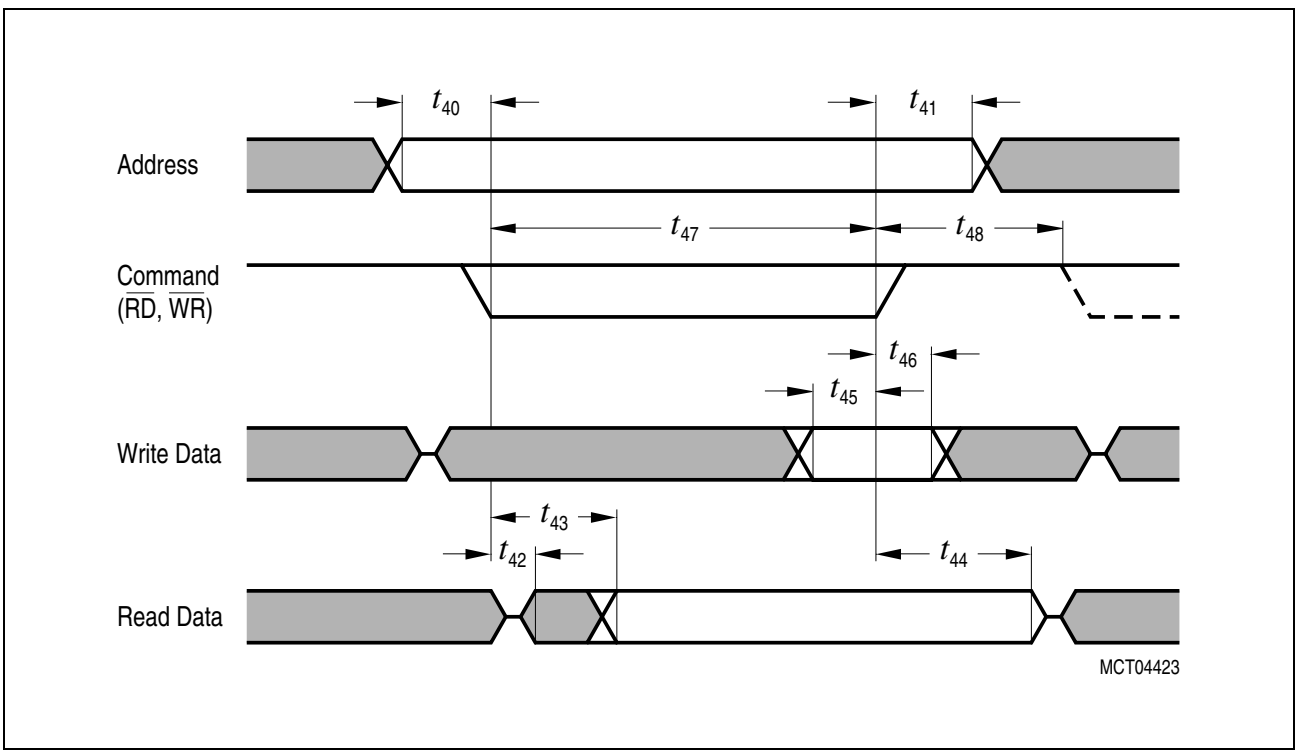
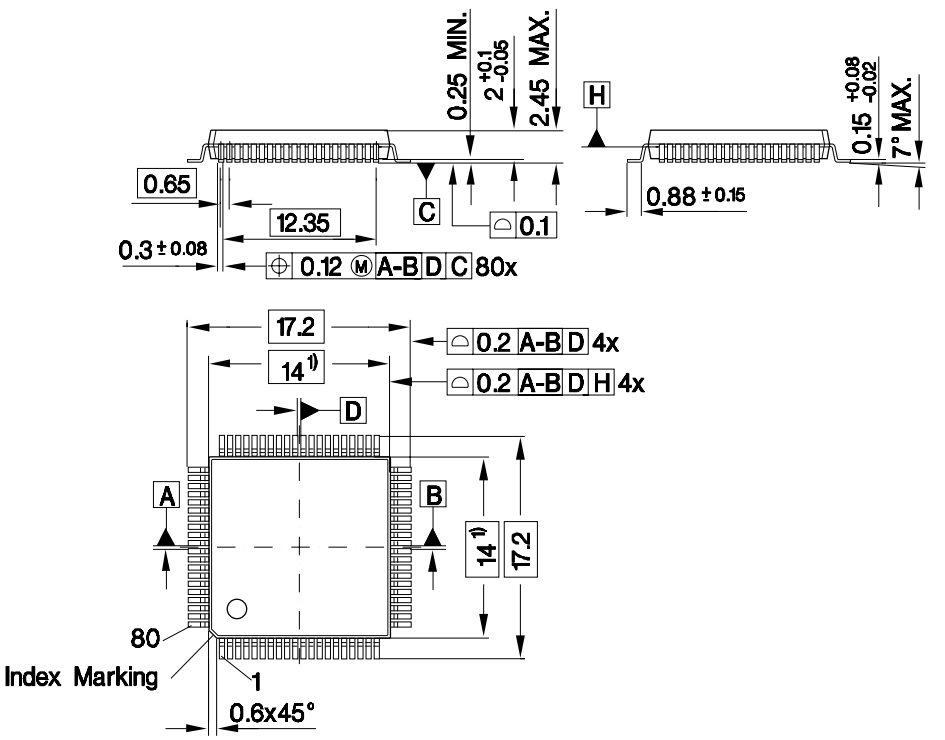


Figure 25 External Access to the XRAM

Package Outlines

P-MQFP-80-7
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05249

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm