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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, SPI, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	59
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	PG-MQFP-80-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c164cilmcafxuma1

Data Sheet, V2.0, May 2001

C164CI/SI
C164CL/SL

16-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.
P1L.0-7	47-52, 57-59		
P1H.0-7	59, 62-68		
			The following PORT1 pins also serve for alt. functions:
P1L.0	47	I/O	CC60 CAPCOM6: Input / Output of Channel 0
P1L.1	48	O	COUT60 CAPCOM6: Output of Channel 0
P1L.2	49	I/O	CC61 CAPCOM6: Input / Output of Channel 1
P1L.3	50	O	COUT61 CAPCOM6: Output of Channel 1
P1L.4	51	I/O	CC62 CAPCOM6: Input / Output of Channel 2
P1L.5	52	O	COUT62 CAPCOM6: Output of Channel 2
P1L.6	57	O	COUT63 Output of 10-bit Compare Channel
P1L.7	58	I	$\overline{\text{CTRAP}}$ CAPCOM6: Trap Input $\overline{\text{CTRAP}}$ is an input pin with an internal pullup resistor. A low level on this pin switches the compare outputs of the CAPCOM6 unit to the logic level defined by software.
P1H.0	59	I	$\overline{\text{CC6POS0}}$ CAPCOM6: Position 0 Input, **)
		I	EX0IN Fast External Interrupt 0 Input
P1H.1	62	I	$\overline{\text{CC6POS1}}$ CAPCOM6: Position 1 Input, **)
		I	EX1IN Fast External Interrupt 1 Input
P1H.2	63	I	$\overline{\text{CC6POS2}}$ CAPCOM6: Position 2 Input, **)
		I	EX2IN Fast External Interrupt 2 Input
P1H.3	64	I	EX3IN Fast External Interrupt 3 Input, T7IN CAPCOM2: Timer T7 Count Input
P1H.4	65	I/O	CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	66	I/O	CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	67	I/O	CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	68	I/O	CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.
			Note: The marked (**) input signals are available only in devices with a full function CAPCOM6.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
P8		IO	Port 8 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). Port 8 pins provide inputs/outputs for CAPCOM2 and serial interface lines.[1)]
P8.0	72	I/O I	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp., CAN1_RxD CAN 1 Receive Data Input
P8.1	73	I/O O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp., CAN1_TxD CAN 1 Transmit Data Output
P8.2	74	I/O I	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp., CAN1_RxD CAN 1 Receive Data Input
P8.3	75	I/O O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp., CAN1_TxD CAN 1 Transmit Data Output
V_{AREF}	1	–	Reference voltage for the A/D converter.
V_{AGND}	80	–	Reference ground for the A/D converter.
V_{DD}	7, 21, 40, 53, 61	–	Digital Supply Voltage: +5 V during normal operation and idle mode. ≥2.5 V during power down mode.
V_{SS}	6, 20, 41, 56, 60	–	Digital Ground.

1) The CAN interface lines are assigned to ports P4 and P8 under software control. Within the CAN module several assignments can be selected.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated as if it were a hardware reset. In particular, the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Memory Organization

The memory space of the C164CI is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C164CI incorporates 64 KBytes of on-chip OTP memory or 64/48 KBytes of on-chip mask-programmable ROM (not in the ROM-less derivative, of course) for code or constant data. The lower 32 KBytes of the on-chip ROM/OTP can be mapped either to segment 0 or segment 1.
The OTP memory can be programmed by the CPU itself (in system, e.g. during booting) or directly via an external interface (e.g. before assembly). The programming time is approx. 100 µs per word. An external programming voltage V_{PP} = 11.5 V must be supplied for this purpose (via pin $\overline{EA}/V_{PP}$).

2 KBytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

2 KBytes of on-chip Extension RAM (XRAM) are provided to store user data, user stacks, or code. The XRAM is accessed like external memory and therefore cannot be used for the system stack or for register banks and is not bitaddressable. The XRAM permits 16-bit accesses with maximum speed.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 4 MBytes of external RAM and/or ROM can be connected to the microcontroller.

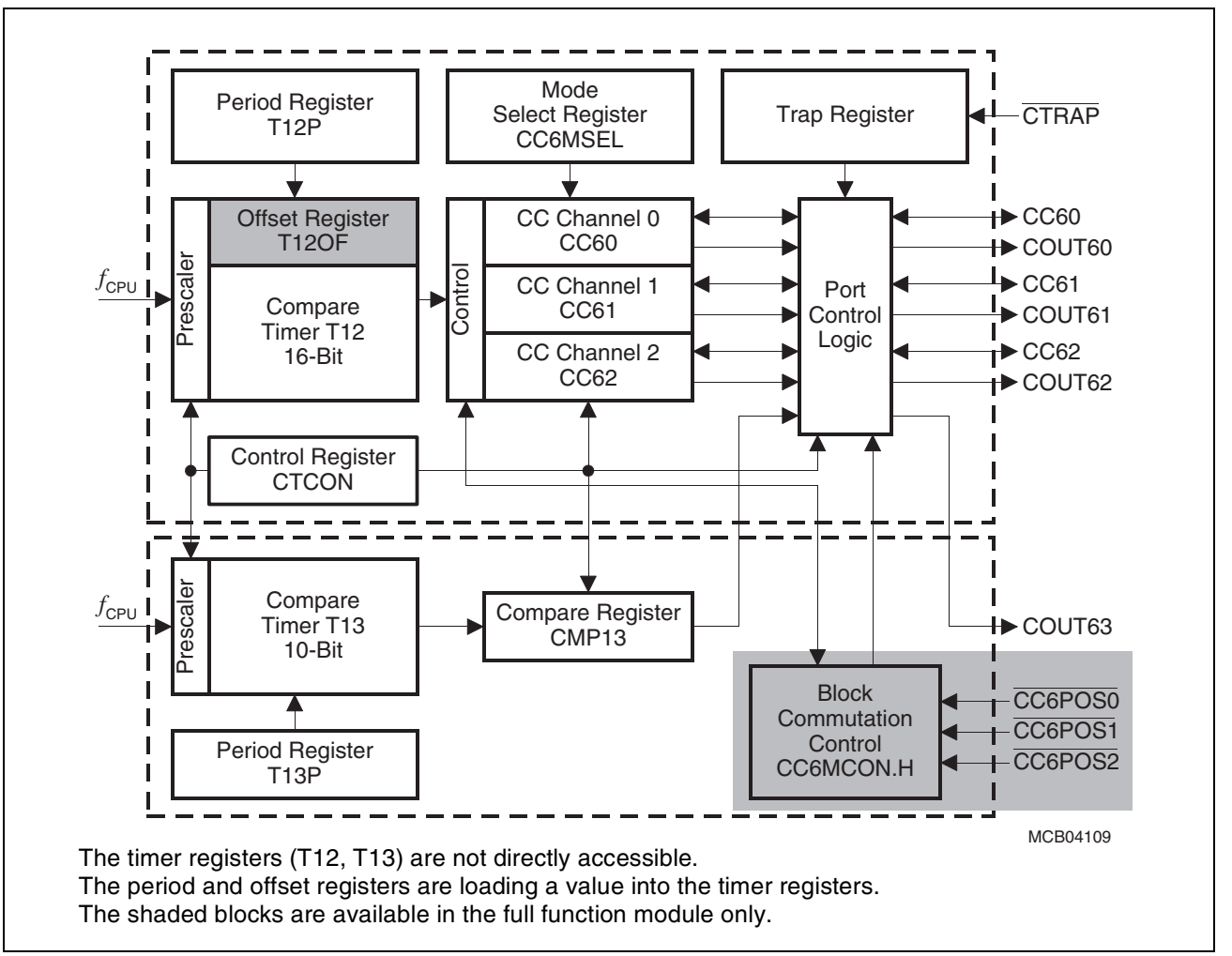
Table 3 C164CI Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM 6 Timer 12	T12IR	T12IE	T12INT	$00'0134_H$	$4D_H$
CAPCOM 6 Timer 13	T13IR	T13IE	T13INT	$00'0138_H$	$4E_H$
CAPCOM 6 Emergency	CC6EIR	CC6EIE	CC6EINT	$00'013C_H$	$4F_H$

The Capture/Compare Unit CAPCOM6

The CAPCOM6 unit supports generation and control of timing sequences on up to three 16-bit capture/compare channels plus one 10-bit compare channel.
In compare mode the CAPCOM6 unit provides two output signals per channel which have inverted polarity and non-overlapping pulse transitions. The compare channel can generate a single PWM output signal and is further used to modulate the capture/compare output signals.
In capture mode the contents of compare timer 12 is stored in the capture registers upon a signal transition at pins CCx.

Compare timers T12 (16-bit) and T13 (10-bit) are free running timers which are clocked by the prescaled CPU clock.



The timer registers (T12, T13) are not directly accessible.
The period and offset registers are loading a value into the timer registers.
The shaded blocks are available in the full function module only.

Figure 5 CAPCOM6 Block Diagram

For motor control applications both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer 12 or by a typical hall sensor pattern at the interrupt inputs (block commutation).

Note: Multichannel signal generation is provided only in devices with a full CAPCOM6.

General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates three 16-bit timers. Each timer may operate independently in a number of different modes, or may be concatenated with another timer.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer over-flow/underflow. The state of this latch may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL.

A/D Converter

For analog signal measurement, a 10-bit A/D converter with 8 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 8 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C164CI supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels (standard or extension) are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

CAN-Module

The integrated CAN-Module handles the completely autonomous transmission and reception of CAN frames in accordance with the CAN specification V2.0 part B (active), i.e. the on-chip CAN-Modules can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

The module provides Full CAN functionality on up to 15 message objects. Message object 15 may be configured for Basic CAN functionality. Both modes provide separate masks for acceptance filtering which allows to accept a number of identifiers in Full CAN mode and also allows to disregard a number of identifiers in Basic CAN mode. All message objects can be updated independent from the other objects and are equipped for the maximum message length of 8 bytes.

The bit timing is derived from the XCLK and is programmable up to a data rate of 1 Mbit/s. Each CAN-Module uses two pins of Port 4 or Port 8 to interface to an external bus transceiver. The interface pins are assigned via software.

Note: When the CAN interface is assigned to Port 4, the respective segment address lines on Port 4 cannot be used. This will limit the external address space.

Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/4/128/256. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 20 µs and 336 ms can be monitored (@ 25 MHz).
The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

Oscillator Watchdog

The Oscillator Watchdog (OWD) monitors the clock signal generated by the on-chip oscillator (either with a crystal or via external clock drive). For this operation the PLL provides a clock signal which is used to supervise transitions on the oscillator clock. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the OWD activates the PLL Unlock/OWD interrupt node and supplies the CPU with the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

In direct drive mode the PLL base frequency is used directly (f_{CPU} = 2 … 5 MHz).
In prescaler mode the PLL base frequency is divided by 2 (f_{CPU} = 1 … 2.5 MHz).

Note: The CPU clock source is only switched back to the oscillator clock after a hardware reset.

The oscillator watchdog can be disabled by setting bit OWDDIS in register SYSCON. In this case (OWDDIS = ‘1’) the PLL remains idle and provides no clock signal, while the CPU clock signal is derived directly from the oscillator clock or via prescaler or SDD. Also no interrupt request will be generated in case of a missing oscillator clock.

Note: At the end of a reset bit OWDDIS reflects the inverted level of pin $\overline{RD}$ at that time. Thus the oscillator watchdog may also be disabled via hardware by (externally) pulling the $\overline{RD}$ line low upon a reset, similar to the standard reset configuration via PORT0.

Table 10 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)[2]
Strong driver	10 mA	2.5 mA
Medium driver	4.0 mA	1.0 mA
Weak driver	0.5 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

2) The current ROM-version of the C164CI (step Ax) is equipped with port drivers, which provide reduced driving capability and reduced control. Please refer to the actual errata sheet for details.

Power Consumption C164CI (ROM)

(Operating Conditions apply)

Parameter	Sym-bol	Limit Values		Unit	Test Conditions
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD}	–	1 + 2.5 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX}	–	1 + 1.1 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO}[2]	–	500 + 50 × f_{OSC}	µA	$\overline{RSTIN}$ = V_{IH1} f_{OSC} in [MHz][1]
Sleep and Power-down mode supply current with RTC running	I_{PDR}[2]	–	200 + 25 × f_{OSC}	µA	V_{DD} = V_{DDmax} f_{OSC} in [MHz][3]
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	50	µA	V_{DD} = V_{DDmax}[3]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 9**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is determined mainly by the current consumed by the oscillator (see **Figure 8**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

3) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

Power Consumption C164CI (OTP)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD}	–	10 + 3.5 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL} f_{CPU} in [MHz] [1]
Idle mode supply current with all peripherals active	I_{IDX}	–	5 + 1.25 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [1]
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO} [2]	–	500 + 50 × f_{OSC}	µA	$\overline{RSTIN}$ = V_{IH1} f_{OSC} in [MHz] [1]
Sleep and Power-down mode supply current with RTC running	I_{PDR} [2]	–	200 + 25 × f_{OSC}	µA	V_{DD} = V_{DDmax} f_{OSC} in [MHz] [3]
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	50	µA	V_{DD} = V_{DDmax} [3]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is determined mainly by the current consumed by the oscillator (see **Figure 8**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

3) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

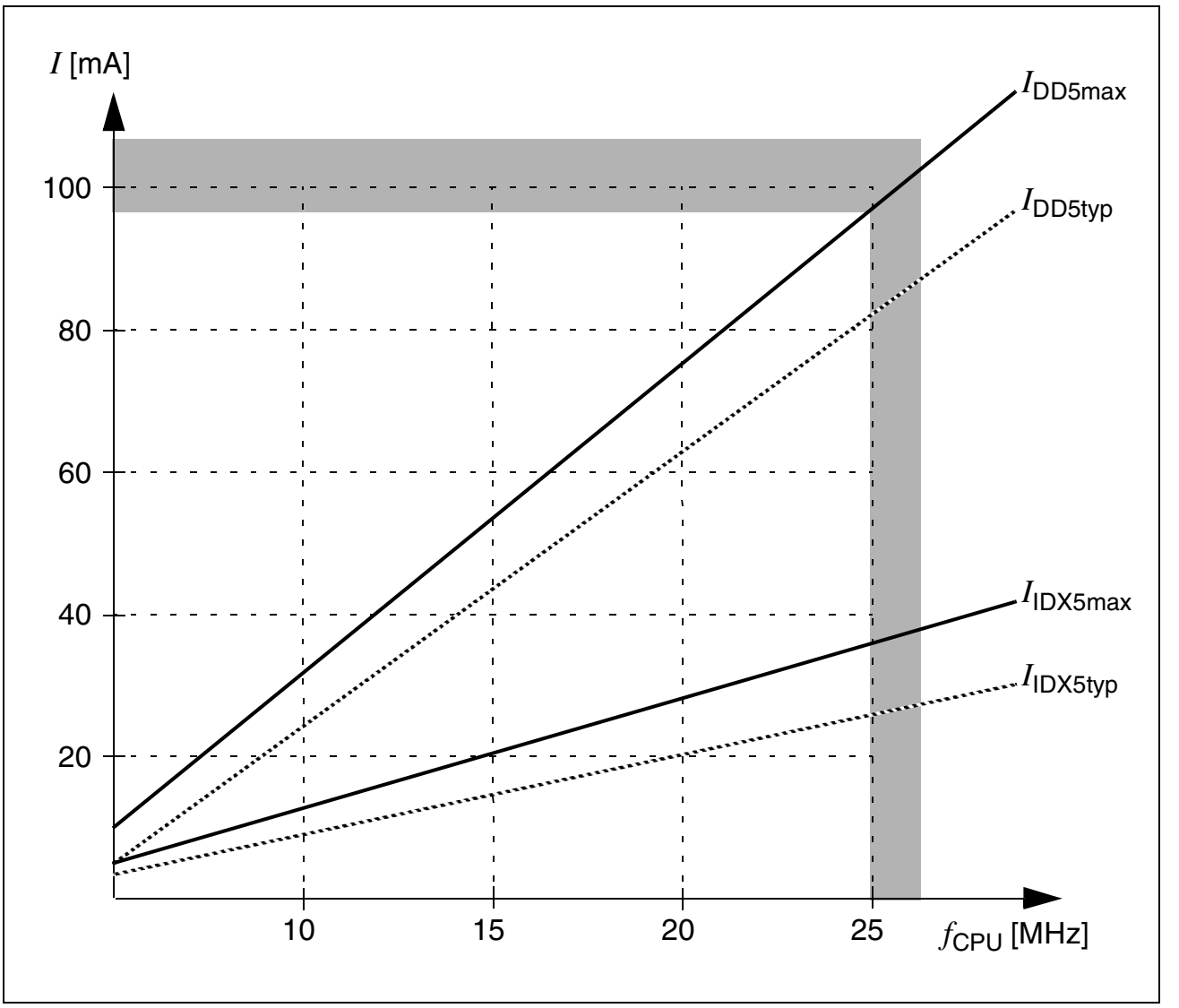


Figure 10 Supply/Idle Current as a Function of Operating Frequency for OTP Derivatives

AC Characteristics
Definition of Internal Timing

The internal operation of the C164CI is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see **Figure 11**).

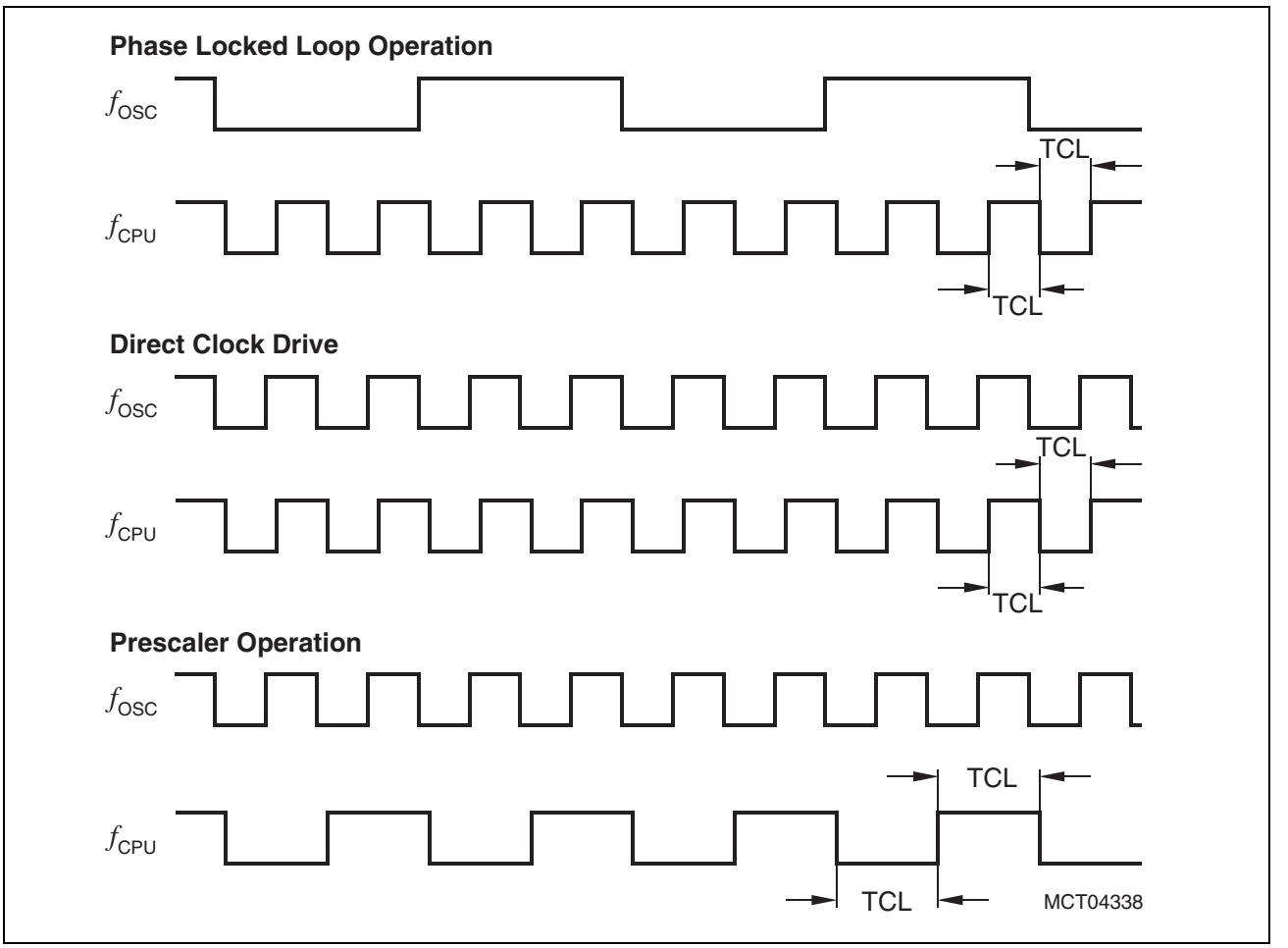


Figure 11 Generation Mechanisms for the CPU Clock

The CPU clock signal f_{CPU} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU}. This influence must be regarded when calculating the timings for the C164CI.

*Note: The example for PLL operation shown in **Figure 11** refers to a PLL factor of 4.*

The used mechanism to generate the basic CPU clock is selected by bitfield CLKCFG in register RP0H.7-5.
Upon a long hardware reset register RP0H is loaded with the logic levels present on the upper half of PORT0 (P0H), i.e. bitfield CLKCFG represents the logic levels on pins

Direct Drive

When direct drive is configured (CLKCFG = 011_B) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC}.
The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{OSC} \times DC_{min} \qquad \text{(DC = duty cycle)}$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{OSC}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, …). Timings that require an even number of TCLs (2, 4, …) may use the formula $2TCL = 1/f_{OSC}$.

Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 15 Memory Cycle Variables

Description	Symbol	Values
ALE Extension	t_A	TCL × <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL × (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL × (1 - <MTTC>)

Note: Please respect the maximum operating frequency of the respective derivative.

AC Characteristics

Multiplexed Bus

(Operating Conditions apply)
ALE cycle time = 6 TCL + 2t_A + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
Address hold after ALE	t_7	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	26	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns

Multiplexed Bus (cont'd)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A + t_C + t_F$ (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	26 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$[1)]	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In[1)]	t_{39}	SR	–	40 + t_C + $2t_A$	–	3TCL - 20 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$[1)]	t_{40}	CC	46 + t_F	–	3TCL - 14 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns

Multiplexed Bus (cont'd)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A + t_C + t_F$ (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE fall. edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW delay)	t_{43}	CC	-4 + t_A	–	-4 + t_A	–	ns
Address float after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW delay)	t_{45}	CC	–	20	–	TCL	ns
$\overline{\text{RdCS}}$ to Valid Data In (with RW delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{\text{RdCS}}$ to Valid Data In (no RW delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (with RW delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (no RW delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{\text{WrCS}}$	t_{50}	CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$	t_{52}	SR	–	20 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{54}	CC	20 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{56}	CC	20 + t_F	–	2TCL - 20 + t_F	–	ns

[1] These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

Demultiplexed Bus (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{\text{RdCS}}$ (no RW-delay)[1]	t_{68}	SR	–	0 + t_F	–	TCL - 20 + $2t_A$ + t_F[1]	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55}	CC	-6 + t_F	–	-6 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{57}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.

3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

AC Characteristics

CLKOUT

(Operating Conditions apply)

Parameter	Symbol	Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
		min.	max.	min.	max.	
CLKOUT cycle time	t_{29} CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30} CC	14	–	TCL - 6	–	ns
CLKOUT low time	t_{31} CC	10	–	TCL - 10	–	ns
CLKOUT rise time	t_{32} CC	–	4	–	4	ns
CLKOUT fall time	t_{33} CC	–	4	–	4	ns
CLKOUT rising edge to ALE falling edge	t_{34} CC	$0 + t_A$	$10 + t_A$	$0 + t_A$	$10 + t_A$	ns

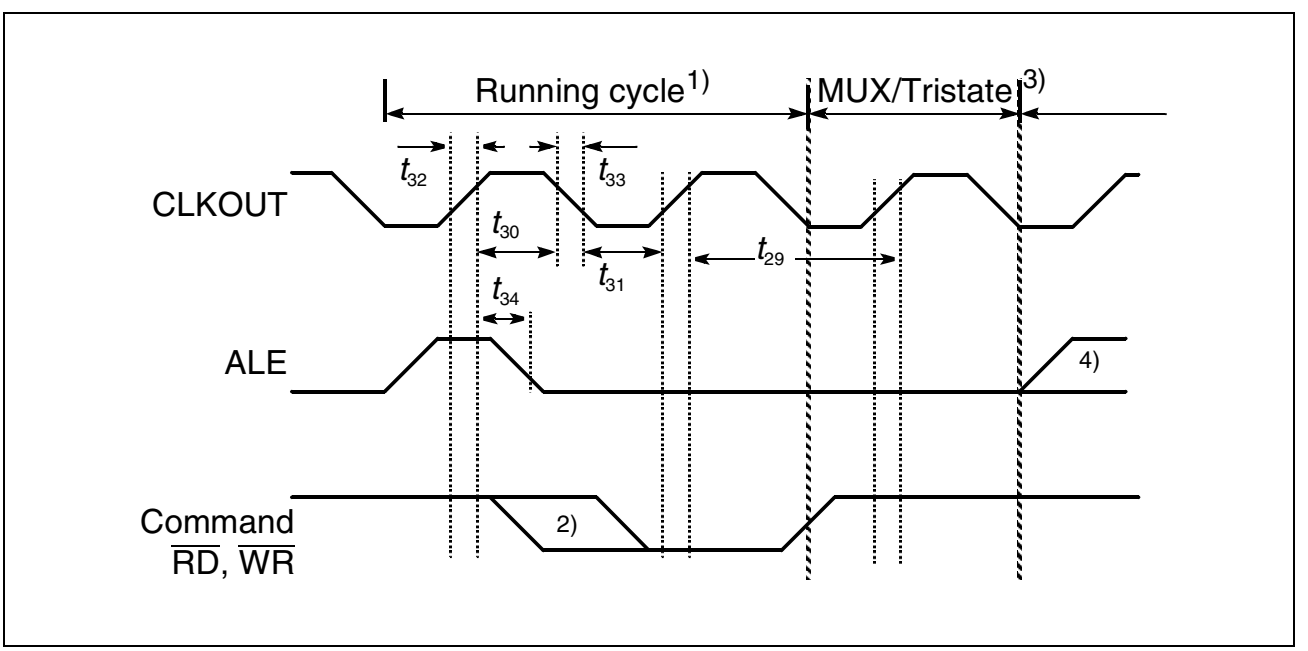


Figure 24 CLKOUT Timing

Notes

1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
2) The leading edge of the respective command depends on RW-delay.
3) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.
4) The next external bus cycle may start here.