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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, SPI, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	59
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	PG-MQFP-80-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c164cilmcakxuma1

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Pin Configuration

(top view)



Figure 2

*) The marked pins of Port 4 and Port 8 can have CAN interface lines assigned to them. Table 2 on the pages below lists the possible assignments.

The *marked input signals* are available only in devices with a full-function CAPCOM6. They are not available in devices with a reduced-function CAPCOM6.



Table 2	Fable 2Pin Definitions and Functions (cont'd)									
Symbol	Pin No.	Input Outp.	Function	Function						
EA/V _{PP}	28	1	 External Access Enable pin. A low level at this pin during and after Reset forces the C164CI to latch the configuration from PORT0 and pin RD, and to begin instruction execution out of external memory. A high level forces the C164CI to latch the configuration from pins RD and ALE, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'. 							
			Note: This pin also accepts the programming voltage for the OTP derivatives.							
PORT0 POL.0-7 POH.0-7	29- 36 37-39, 42-46	IO	PORT0 consists of the two 8-bit bidirectional I/O ports POL and POH. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed							
			bus modes and as the modes.	he data (D) bus	s in demultiplexed bus					
			Data Path Width: P0L.0 – P0L.7: P0H.0 – P0H.7: Multiplexed bus mo Data Path Width: P0L.0 – P0L.7: P0H.0 – P0H.7:	8-bit D0 – D7 I/O odes: 8-bit AD0 – AD7 A8 – A15	16-bit D0 – D7 D8 – D15 16-bit AD0 – AD7 AD8 – AD15					



Functional Description

The architecture of the C164CI combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C164CI.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).



Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resoures, the X-Peripherals (see Figure 3).

The XBUS resources (XRAM, CAN) of the C164CI can be enabled or disabled during initialization by setting the general X-Peripheral enable bit XPEN (SYSCON.2). Modules that are disabled consume neither address space nor port pins.



External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-/20-/22-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/22-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/22-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/22-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/ output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 4 external \overline{CS} signals (3 windows plus default) can be generated in order to save external glue logic. The C164Cl offers the possibility to switch the \overline{CS} outputs to an unlatched mode. In this mode the internal filter logic is switched off and the \overline{CS} signals are directly generated from the address. The unlatched \overline{CS} mode is enabled by setting CSCFG (SYSCON.6).

For applications which require less than 4 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 6 address lines, if an address space of 4 MBytes is used.

Note: When the on-chip CAN Module is used with the interface lines assigned to Port 4, the CAN lines override the segment address lines and the segment address output on Port 4 is therefore limited to 4 bits i.e. address lines A19 ... A16.



Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C164CI's instructions can be executed in just one machine cycle which requires 2 CPU clocks (4 TCL). For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16×16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', reduces the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.



Figure 4

CPU Block Diagram



The Capture/Compare Unit CAPCOM6

The CAPCOM6 unit supports generation and control of timing sequences on up to three 16-bit capture/compare channels plus one 10-bit compare channel.

In compare mode the CAPCOM6 unit provides two output signals per channel which have inverted polarity and non-overlapping pulse transitions. The compare channel can generate a single PWM output signal and is further used to modulate the capture/ compare output signals.

In capture mode the contents of compare timer 12 is stored in the capture registers upon a signal transition at pins CCx.

Compare timers T12 (16-bit) and T13 (10-bit) are free running timers which are clocked by the prescaled CPU clock.



Figure 5 CAPCOM6 Block Diagram

For motor control applications both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer 12 or by a typical hall sensor pattern at the interrupt inputs (block commutation).

Note: Multichannel signal generation is provided only in devices with a full CAPCOM6.



Oscillator Watchdog

The Oscillator Watchdog (OWD) monitors the clock signal generated by the on-chip oscillator (either with a crystal or via external clock drive). For this operation the PLL provides a clock signal which is used to supervise transitions on the oscillator clock. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the OWD activates the PLL Unlock/OWD interrupt node and supplies the CPU with the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

In direct drive mode the PLL base frequency is used directly ($f_{CPU} = 2 \dots 5 \text{ MHz}$). In prescaler mode the PLL base frequency is divided by 2 ($f_{CPU} = 1 \dots 2.5 \text{ MHz}$).

Note: The CPU clock source is only switched back to the oscillator clock after a hardware reset.

The oscillator watchdog can be disabled by setting bit OWDDIS in register SYSCON. In this case (OWDDIS = '1') the PLL remains idle and provides no clock signal, while the CPU clock signal is derived directly from the oscillator clock or via prescaler or SDD. Also no interrupt request will be generated in case of a missing oscillator clock.

Note: At the end of a reset bit OWDDIS reflects the inverted level of pin RD at that time. Thus the oscillator watchdog may also be disabled via hardware by (externally) pulling the RD line low upon a reset, similar to the standard reset configuration via PORT0.



Instruction Set Summary

 Table 6 lists the instructions of the C164CI in a condensed way.

The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the "C166 Family Instruction Set Manual".

This document also provides a detailled description of each instruction.

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2/4
ADDC(B)	Add word (byte) operands with Carry	2/4
SUB(B)	Subtract word (byte) operands	2/4
SUBC(B)	Subtract word (byte) operands with Carry	2/4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2/4
OR(B)	Bitwise OR, (word/byte operands)	2/4
XOR(B)	Bitwise XOR, (word/byte operands)	2/4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2/4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2/4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2/4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

Table 6 Instruction Set Summary



Special Function Registers Overview

Table 7 lists all SFRs which are implemented in the C164CI in alphabetical order. **Bit-addressable** SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers within on-chip X-peripherals are marked with the letter "**X**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Name		Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC b	b	FF98 _H	CCH	A/D Converter End of Conversion Interrupt Control Register	0000 _H
ADCON k	b	FFA0 _H	D0 _H	A/D Converter Control Register	0000 _H
ADDAT		FEA0 _H	50 _H	A/D Converter Result Register	0000 _H
ADDAT2		F0A0 _H E	50 _H	A/D Converter 2 Result Register	0000 _H
ADDRSEL1		FE18 _H	0C _H	Address Select Register 1	0000 _H
ADDRSEL2		FE1A _H	0D _H	Address Select Register 2	0000 _H
ADDRSEL3		FE1C _H	0E _H	Address Select Register 3	0000 _H
ADDRSEL4		FE1E _H	0F _H	Address Select Register 4	0000 _H
ADEIC b	b	FF9A _H	CD _H	A/D Converter Overrun Error Interrupt Control Register	0000 _H
BUSCON0	o	FF0C _H	86 _H	Bus Configuration Register 0	0000 _H
BUSCON1	b	FF14 _H	8A _H	Bus Configuration Register 1	0000 _H
BUSCON2	b	FF16 _H	8B _H	Bus Configuration Register 2	0000 _H
BUSCON3	b	FF18 _H	8C _H	Bus Configuration Register 3	0000 _H
BUSCON4	b	FF1A _H	8D _H	Bus Configuration Register 4	0000 _H
C1BTR		EF04 _H X		CAN1 Bit Timing Register	UUUU _H
C1CSR		EF00 _H X		CAN1 Control / Status Register	XX01 _H
C1GMS		EF06 _H X		CAN1 Global Mask Short	UFUU _H
C1LARn		EFn4 _H X		CAN Lower Arbitration Register (msg. n)	UUUU _H
C1LGML		EF0A _H X		CAN Lower Global Mask Long	UUUU _H
C1LMLM		EF0E _H X		CAN Lower Mask of Last Message	UUUU _H

Table 7 C164Cl Registers, Ordered by Name



Absolute Maximum Ratings

	5									
Parameter	Parameter Symbol Limit Values		Values	Unit	Notes					
		min.	max.							
Storage temperature	T _{ST}	-65	150	°C	-					
Junction temperature	TJ	-40	150	°C	under bias					
Voltage on V_{DD} pins with respect to ground (V_{SS})	V _{DD}	-0.5	6.5	V	-					
Voltage on any pin with respect to ground (V_{SS})	V _{IN}	-0.5	V _{DD} + 0.5	V	-					
Input current on any pin during overload condition	-	-10	10	mA	-					
Absolute sum of all input currents during overload condition	-	-	100	mA	_					
Power dissipation	P _{DISS}	_	1.5	W	-					

Table 8 Absolute Maximum Rating Parameters

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.



Port Output Driver Mode	Maximum Output Current (I _{OLmax} , -I _{OHmax}) ¹⁾	Nominal Output Current $(I_{OLnom}, -I_{OHnom})^2)$
Strong driver	10 mA	2.5 mA
Medium driver	4.0 mA	1.0 mA
Weak driver	0.5 mA	0.1 mA

Table 10 Current Limits for Port Output Drivers

¹⁾ An output current above II_{OXnom}I may be drawn from up to three pins at the same time. For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.

²⁾ The current ROM-version of the C164CI (step Ax) is equipped with port drivers, which provide reduced driving capability and reduced control. Please refer to the actual errata sheet for details.

Power Consumption C164CI (ROM)

(Operating Conditions apply)

Parameter	Sym-	Limit	Values	Unit	Test
	bol	min.	max.		Conditions
Power supply current (active) with all peripherals active	I _{DD}	_	1 + 2.5 × f _{CPU}	mA	$\overline{\text{RSTIN}} = V_{\text{IL}}$ $f_{\text{CPU}} \text{ in } [\text{MHz}]^{1)}$
Idle mode supply current with all peripherals active	I _{IDX}	_	1 + 1.1 × f _{CPU}	mA	$\overline{\text{RSTIN}} = V_{\text{IH1}}$ $f_{\text{CPU}} \text{ in [MHz]}^{1)}$
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I _{IDO} ²⁾	_	500 + 50 × f _{OSC}	μA	$\overline{\text{RSTIN}} = V_{\text{IH1}}$ f_{OSC} in [MHz] ¹⁾
Sleep and Power-down mode supply current with RTC running	I _{PDR} ²⁾	_	200 + 25 × f _{OSC}	μA	$V_{\text{DD}} = V_{\text{DDmax}}$ f_{OSC} in [MHz] ³⁾
Sleep and Power-down mode supply current with RTC disabled	I _{PDO}	_	50	μA	$V_{\rm DD} = V_{\rm DDmax}^{3)}$

¹⁾ The supply current is a function of the operating frequency. This dependency is illustrated in Figure 9. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

²⁾ This parameter is determined mainly by the current consumed by the oscillator (see Figure 8). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

³⁾ This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD} , V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.



P0.15-13 (P0H.7-5). Register RP0H can be loaded from the upper half of register RSTCON under software control.

Table 11 associates the combinations of these three bits with the respective clock generation mode.

CLKCFG ¹⁾ (RP0H.7-5)	CPU Frequency $f_{CPU} = f_{OSC} \times F$	External Clock Input Range ²⁾	Notes		
1 1 1	$f_{OSC} \times 4$	2.5 to 6.25 MHz	Default configuration		
1 1 0	$f_{OSC} \times 3$	3.33 to 8.33 MHz	-		
101	$f_{OSC} \times 2$	5 to 12.5 MHz	-		
1 0 0	$f_{OSC} \times 5$	2 to 5 MHz	-		
0 1 1	$f_{OSC} \times 1$	1 to 25 MHz	Direct drive ³⁾		
0 1 0	$f_{\rm OSC} imes$ 1.5	6.66 to 16.66 MHz	-		
0 0 1	f _{OSC} / 2	2 to 50 MHz	CPU clock via prescaler		
0 0 0	$f_{\rm OSC} \times 2.5$	4 to 10 MHz	-		

 Table 11
 C164Cl Clock Generation Modes

¹⁾ Please note that pin P0.15 (corresponding to RP0H.7) is inverted in emulation mode, and thus also in EHM.

²⁾ The external clock input range refers to a CPU clock range of 10 ... 25 MHz.

³⁾ The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When prescaler operation is configured (CLKCFG = 001_B) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.

The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC} .

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

When PLL operation is configured (via CLKCFG) the on-chip phase locked loop is enabled and provides the CPU clock (see **Table 11**). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{OSC} \times F$). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.



Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC} . The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and Figure 12).

For a period of $N \times \text{TCL}$ the minimum value is computed using the corresponding deviation D_N :

$$(N \times \text{TCL})_{\text{min}} = N \times \text{TCL}_{\text{NOM}} - D_N; D_N [\text{ns}] = \pm (13.3 + N \times 6.3) / f_{\text{CPU}} [\text{MHz}],$$

where N = number of consecutive TCLs and 1 $\leq N \leq$ 40.

So for a period of 3 TCLs @ 25 MHz (i.e. N = 3): D₃ = (13.3 + 3 × 6.3)/25 = 1.288 ns, and (3TCL)_{min} = 3TCL_{NOM} - 1.288 ns = 58.7 ns (@ f_{CPU} = 25 MHz).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is neglectible.

Note: For all periods longer than 40 TCL the N = 40 value can be used (see Figure 12).



Figure 12 Approximated Maximum Accumulated PLL Jitter



AC Characteristics External Clock Drive XTAL1

(Operating Conditions apply)

Parameter	Symbol		bol Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t _{OSC}	SR	40	_	20	_	60 ¹⁾	500 ¹⁾	ns
High time ²⁾	<i>t</i> ₁	SR	20 ³⁾	_	6	_	10	_	ns
Low time ²⁾	<i>t</i> ₂	SR	20 ³⁾	-	6	_	10	_	ns
Rise time ²⁾	t ₃	SR	_	8	-	5	_	10	ns
Fall time ²⁾	<i>t</i> ₄	SR	_	8	_	5	_	10	ns

Table 12 External Clock Drive Characteristics

 The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

²⁾ The clock input signal must reach the defined levels V_{IL2} and V_{IH2} .

³⁾ The minimum high and low time refers to a duty cycle of 50%. The maximum operating freqency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.



Figure 13 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.

It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).



Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 15Memory Cycle Variables

Description	Symbol	Values
ALE Extension	t _A	TCL × <alectl></alectl>
Memory Cycle Time Waitstates	t _C	2TCL × (15 - <mctc>)</mctc>
Memory Tristate Time	t _F	2TCL × (1 - <mttc>)</mttc>

Note: Please respect the maximum operating frequency of the respective derivative.

AC Characteristics

Multiplexed Bus

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A + t_C + t_F$ (120 ns at 25 MHz CPU clock without waitstates)

Parameter		nbol	Max. CPU Clock = 25 MHz		Variable (1 / 2TCL =	Unit	
			min.	max.	min.	max.	
ALE high time	<i>t</i> 5	CC	$10 + t_{A}$	_	TCL - 10 + <i>t</i> _A	-	ns
Address setup to ALE	<i>t</i> ₆	CC	$4 + t_A$	-	TCL - 16 + <i>t</i> _A	-	ns
Address hold after ALE	<i>t</i> ₇	CC	$10 + t_{A}$	_	TCL - 10 + <i>t</i> _A	-	ns
ALE falling edge to RD, WR (with RW-delay)	<i>t</i> 8	CC	$10 + t_{A}$	-	TCL - 10 + <i>t</i> _A	-	ns
ALE falling edge to RD, WR (no RW-delay)	t ₉	СС	$-10 + t_{A}$	_	$-10 + t_{A}$	-	ns
Address float after RD, WR (with RW-delay)	<i>t</i> ₁₀	CC	_	6	_	6	ns
Address float after RD, WR (no RW-delay)	<i>t</i> ₁₁	CC	_	26	_	TCL + 6	ns
RD, WR low time (with RW-delay)	t ₁₂	CC	$30 + t_{\rm C}$	-	2TCL - 10 + <i>t</i> _C	-	ns





Figure 16 External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE





Figure 17 External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Extended ALE



Demultiplexed Bus (cont'd)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter		nbol	Max. CPU Clock = 25 MHz		Variable (1 / 2TCL =	Unit	
			min.	max.	min.	max.	
Data valid to \overline{WR}	t ₂₂	CC	$20 + t_{\rm C}$	_	2TCL - 20 + <i>t</i> _C	_	ns
Data hold after WR	t ₂₄	CC	10 + <i>t</i> _F	-	TCL - 10 + <i>t</i> _F	_	ns
ALE rising edge after \overline{RD} , WR	t ₂₆	CC	-10 + <i>t</i> _F	_	-10 + <i>t</i> _F	_	ns
Address hold after $\overline{WR}^{2)}$	t ₂₈	CC	$0 + t_{F}$	-	$0 + t_{F}$	_	ns
ALE falling edge to $\overline{CS}^{3)}$	t ₃₈	CC	-4 - t _A	10 - <i>t</i> _A	-4 - t _A	10 - <i>t</i> _A	ns
CS low to Valid Data In ³⁾	t ₃₉	SR	_	$40 + t_{C} + 2t_{A}$	_	3TCL - 20 + <i>t</i> _C + 2 <i>t</i> _A	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}^{3)}$	<i>t</i> ₄₁	CC	6 + <i>t</i> _F	_	TCL - 14 + <i>t</i> _F	_	ns
ALE falling edge to \overline{RdCS} , WrCS (with RW-delay)	t ₄₂	CC	16 + <i>t</i> _A	_	TCL - 4 + <i>t</i> _A	_	ns
ALE falling edge to RdCS, WrCS (no RW-delay)	t ₄₃	CC	$-4 + t_{A}$	_	-4 + t _A	_	ns
RdCS to Valid Data In (with RW-delay)	t ₄₆	SR	_	16 + <i>t</i> _C	_	2TCL - 24 + <i>t</i> _C	ns
RdCS to Valid Data In (no RW-delay)	t ₄₇	SR	_	$36 + t_{\rm C}$	_	3TCL - 24 + <i>t</i> _C	ns
RdCS, WrCS Low Time (with RW-delay)	t ₄₈	CC	$30 + t_{\rm C}$	_	2TCL - 10 + <i>t</i> _C	-	ns
RdCS, WrCS Low Time (no RW-delay)	t ₄₉	CC	$50 + t_{\rm C}$	_	3TCL - 10 + <i>t</i> _C	-	ns
Data valid to \overline{WrCS}	t ₅₀	CC	$26 + t_{\rm C}$	_	2TCL - 14 + <i>t</i> _C	-	ns
Data hold after RdCS	<i>t</i> ₅₁	SR	0	-	0	_	ns
Data float after RdCS (with RW-delay) ¹⁾	t ₅₃	SR	_	$20 + t_{\rm F}$	_	$2\text{TCL} - 20 + 2t_A + t_F^{(1)}$	ns





Figure 23 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE

Infineon goes for Business Excellence

"Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.

Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction."

Dr. Ulrich Schumacher

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