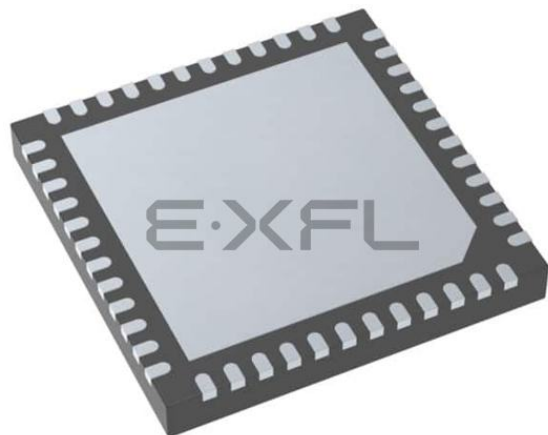




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	38
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l452ceu6

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2 Description

The STM32L452xx devices are the ultra-low-power microcontrollers based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L452xx devices embed high-speed memories (Flash memory up to 512 Kbyte, 160 Kbyte of SRAM), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L452xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer a fast 12-bit ADC (5 Msps), two comparators, one operational amplifier, one DAC channel, an internal voltage reference buffer, a low-power RTC, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, four general-purpose 16-bit timers, and two 16-bit low-power timers.

In addition, up to 21 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces.

- Four I2Cs
- Three SPIs
- Three USARTs, one UART and one Low-Power UART.
- One SAI (Serial Audio Interfaces)
- One SDMMC
- One CAN
- One USB full-speed device crystal less

The STM32L452xx operates in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V V_{DD} power supply when using internal LDO regulator and a 1.05 to 1.32V V_{DD12} power supply when using external SMPS supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMP and comparators. A VBAT input allows to backup the RTC and backup registers. Dedicated V_{DD12} power supplies can be used to bypass the internal LDO regulator when connected to an external SMPS.

The STM32L452xx family offers six packages from 48 to 100-pin packages.

hardware. DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various $\Sigma\Delta$ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 4 multiplexed input digital serial channels:
 - configurable SPI interface to connect various SD modulator(s)
 - configurable Manchester coded 1 wire interface support
 - PDM (Pulse Density Modulation) microphone input support
 - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
 - clock output for SD modulator(s): 0..20 MHz
- alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
 - internal sources: device memory data streams (DMA)
- 2 digital filter modules with adjustable digital signal processing:
 - Sinc^x filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
 - integrator: oversampling ratio (1..256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by:
 - software trigger
 - internal timers
 - external events
 - start-of-conversion synchronously with first digital filter module (DFSDM1_FLT0)
- analog watchdog feature:
 - low value and high value data threshold registers
 - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
 - input from final output data or from selected input digital serial channels
 - continuous monitoring independently from standard conversion
- short circuit detector to detect saturated analog input values (bottom and top range):
 - up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
 - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
 - storage of minimum and maximum values of final conversion data
 - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- “regular” or “injected” conversions:
 - “regular” conversions can be requested at any time or even in continuous mode

3.23.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.24 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.26 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L452xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and one universal asynchronous receiver transmitters (UART4).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2 and USART3 also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4) to wake up the MCU from Stop mode using baudrates up to 204 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 13. STM32L452xx USART/UART/LPUART features

USART modes/features ⁽¹⁾	USART1	USART2	USART3	UART4	LPUART1
Hardware flow control for modem	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X
Synchronous mode	X	X	X	-	-
Smartcard mode	X	X	X	-	-
Single-wire half-duplex communication	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	-
LIN mode	X	X	X	X	-
Dual clock domain	X	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	-	X
Receiver timeout interrupt	X	X	X	X	-
Modbus communication	X	X	X	X	-
Auto baud rate detection	X (4 modes)				-
Driver Enable	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits				

1. X = supported.

Table 16. STM32L452xx pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	LQFP64 SMPS	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	B2	-	-	-	75	G11	VDD	S	-	-	-	-
37	C3	49	49	A7	76	A10	PA14 (JTCK/ SWCLK)	I/O	FT	(3)	JTCK/SWCLK, LPTIM1_OUT, I2C1_SMBA, I2C4_SMBA, SAI1_FS_B, EVENTOUT	-
38	A2	50	50	A6	77	A9	PA15 (JTDI)	I/O	FT	(3)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, UART4_RTS_DE, TSC_G3_IO1, EVENTOUT	-
-	D4	51	51	B7	78	B11	PC10	I/O	FT	-	TRACED1, SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, SDMMC1_D2, EVENTOUT	-
-	B3	52	52	B6	79	C10	PC11	I/O	FT	-	SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, SDMMC1_D3, EVENTOUT	-
-	A3	53	53	C5	80	B10	PC12	I/O	FT	-	TRACED3, SPI3_MOSI, USART3_CK, TSC_G3_IO4, SDMMC1_CK, EVENTOUT	-
-	-	-	-	-	81	C9	PD0	I/O	FT	-	SPI2_NSS, CAN1_RX, EVENTOUT	-
-	-	-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK, CAN1_TX, EVENTOUT	-
-	C4	54	-	B5	83	C8	PD2	I/O	FT	-	TRACED2, TIM3_ETR, USART3_RTS_DE, TSC_SYNC, SDMMC1_CMD, EVENTOUT	-

Table 17. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2 LPTIM1	I2C4/TIM1/ TIM2/TIM3	I2C4/USART2/ CAN1/TIM1	I2C1/I2C2/ I2C3/I2C4	SPI1/SPI2/I2C4	SPI3/DFSDM/ COMP1	USART1/ USART2/ USART3
Port E	PE0	-	-	-	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	-	-	-	DFSDM1_ DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	-	-	-	DFSDM1_ CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_ DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_ CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_ CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	-	-
	PE11	-	TIM1_CH2	-	-	-	-	-	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	-	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	-	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^{\circ}\text{C}$ and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = V_{DDA} = 3\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 14](#).

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 15](#).

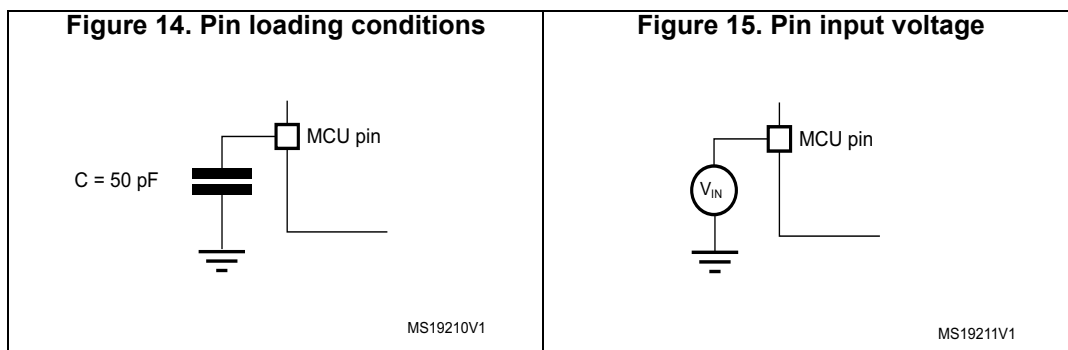


Table 42. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX ⁽¹⁾					Unit
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I _{DD_ALL} (Sleep)	Supply current in sleep mode,	f _{HCLK} = f _{HSE} up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.700	0.730	0.830	1.00	1.35	0.80	0.90	1.05	1.30	1.90	mA
				16 MHz	0.475	0.505	0.605	0.775	1.10	0.55	0.65	0.80	1.05	1.65	
				8 MHz	0.300	0.325	0.425	0.590	0.920	0.35	0.45	0.60	0.85	1.45	
				4 MHz	0.210	0.235	0.335	0.500	0.830	0.25	0.30	0.45	0.75	1.35	
				2 MHz	0.165	0.190	0.290	0.455	0.785	0.20	0.25	0.40	0.70	1.25	
				1 MHz	0.145	0.170	0.265	0.430	0.760	0.15	0.25	0.40	0.65	1.25	
				100 kHz	0.125	0.150	0.245	0.410	0.740	0.15	0.20	0.35	0.65	1.20	
			Range 1	80 MHz	2.30	2.35	2.45	2.65	3.05	2.55	2.65	2.85	3.15	3.80	
				72 MHz	2.10	2.15	2.25	2.45	2.80	2.35	2.40	2.60	2.90	3.55	
				64 MHz	1.90	1.90	2.05	2.25	2.60	2.10	2.20	2.35	2.70	3.35	
				48 MHz	1.40	1.40	1.55	1.75	2.15	1.60	1.65	1.85	2.15	2.80	
				32 MHz	0.970	1.00	1.15	1.30	1.70	1.10	1.20	1.40	1.70	2.35	
				24 MHz	0.765	0.800	0.920	1.10	1.50	0.90	0.95	1.15	1.45	2.10	
				16 MHz	0.555	0.590	0.705	0.895	1.25	0.65	0.75	0.90	1.20	1.85	
I _{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	f _{HCLK} = f _{MSI} all peripherals disable		2 MHz	76.0	110	215	395	745	120	185	355	610	1250	μA
				1 MHz	54.0	86.5	195	370	725	88.5	160	335	585	1250	
				400 kHz	39.0	70.5	175	355	710	68.5	140	320	570	1200	
				100 kHz	35.5	75.0	195	345	715	66.0	130	305	560	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 60. MSI oscillator characteristics⁽¹⁾ (continued)

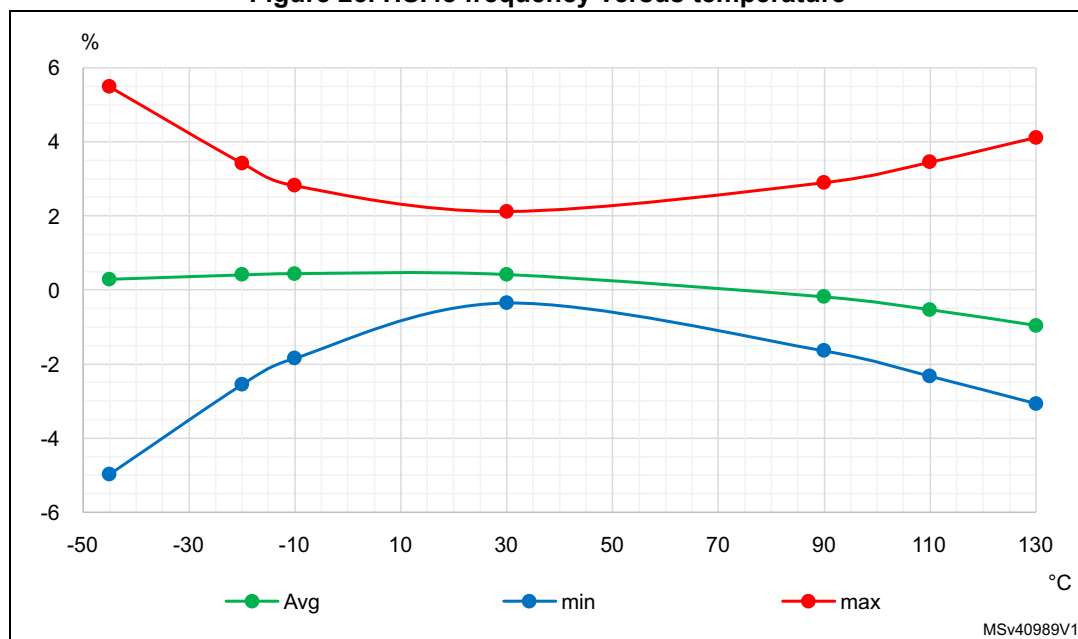
Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta V_{DD}(MSI)^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	$V_{DD}=1.62$ V to 3.6 V	-1.2	-	0.5	%
				$V_{DD}=2.4$ V to 3.6 V	-0.5	-		
			Range 4 to 7	$V_{DD}=1.62$ V to 3.6 V	-2.5	-	0.7	
				$V_{DD}=2.4$ V to 3.6 V	-0.8	-		
			Range 8 to 11	$V_{DD}=1.62$ V to 3.6 V	-5	-	1	
				$V_{DD}=2.4$ V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}(MSI)^{(2)(6)}$	Frequency variation in sampling mode ⁽³⁾	MSI mode	$T_A= -40$ to 85 °C		-	1	2	%
			$T_A= -40$ to 125 °C		-	2	4	
P_USB Jitter(MSI) ⁽⁶⁾	Period jitter for USB clock ⁽⁴⁾	PLL mode Range 11	for next transition	-	-	-	3.458	ns
			for paired transition	-	-	-	3.916	
MT_USB Jitter(MSI) ⁽⁶⁾	Medium term jitter for USB clock ⁽⁵⁾	PLL mode Range 11	for next transition	-	-	-	2	ns
			for paired transition	-	-	-	1	
CC jitter(MSI) ⁽⁶⁾	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI) ⁽⁶⁾	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
$t_{SU}(MSI)^{(6)}$	MSI oscillator start-up time	Range 0		-	-	10	20	us
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)^{(6)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

Table 61. HSI48 oscillator characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N _T jitter	Next transition jitter Accumulated jitter on 28 cycles ⁽⁴⁾	-	-	+/-0.15 ⁽²⁾	-	ns
P _T jitter	Paired transition jitter Accumulated jitter on 56 cycles ⁽⁴⁾	-	-	+/-0.25 ⁽²⁾	-	ns

1. V_{DD} = 3 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

Figure 25. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 62. LSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{LSI}	LSI Frequency	V _{DD} = 3.0 V, T _A = 30 °C	31.04	-	32.96	kHz
		V _{DD} = 1.62 to 3.6 V, T _A = -40 to 125 °C	29.5	-	34	
t _{SU} (LSI) ⁽²⁾	LSI oscillator start-up time	-	-	80	130	μs
t _{STAB} (LSI) ⁽²⁾	LSI oscillator stabilization time	5% of final frequency	-	125	180	μs
I _{DD} (LSI) ⁽²⁾	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.9 PLL characteristics

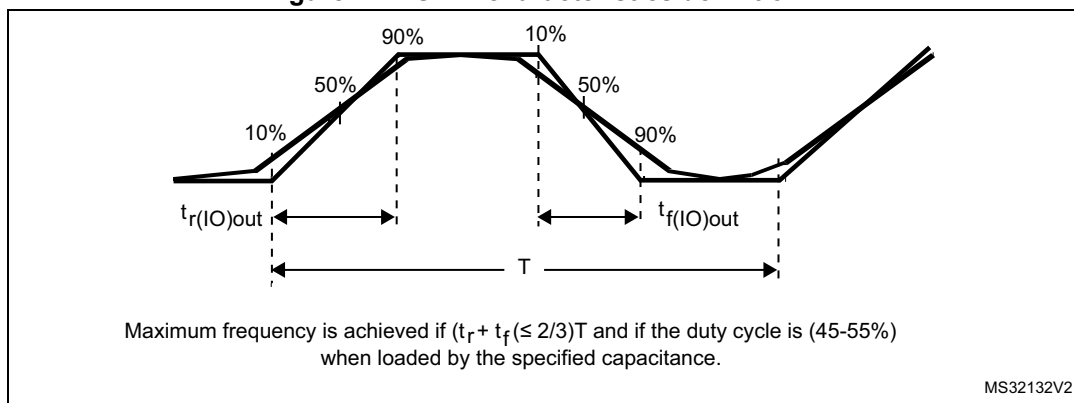
The parameters given in [Table 63](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 23: General operating conditions](#).

Table 63. PLL, PLLSAI1 characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock ⁽²⁾	-	4	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	3.0968	-	80	MHz
		Voltage scaling Range 2	3.0968	-	26	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	12	-	80	MHz
		Voltage scaling Range 2	12	-	26	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	12	-	80	MHz
		Voltage scaling Range 2	12	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	MHz
		Voltage scaling Range 2	96	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	μs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	-	40	-	$\pm ps$
	RMS period jitter		-	30	-	
$I_{DD}(PLL)$	PLL power consumption on V_{DD} ⁽¹⁾	VCO freq = 96 MHz	-	200	260	μA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.

2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 2 PLLs.

Figure 27. I/O AC characteristics definition⁽¹⁾

1. Refer to [Table 73: I/O AC characteristics](#).

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} .

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 23: General operating conditions](#).

Table 74. NRST pin characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 \times V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7 \times V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	k Ω
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	350	-	-	ns

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Table 77. ADC characteristics^{(1) (2)} (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	$f_{ADC} = 80 \text{ MHz}$	0.03125	-	8.00625	μs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	μs
t_{CONV}	Total conversion time (including sampling time)	$f_{ADC} = 80 \text{ MHz}$ Resolution = 12 bits	0.1875	-	8.1625	μs
		Resolution = 12 bits	$t_s + 12.5$ cycles for successive approximation = 15 to 653			$1/f_{ADC}$
$I_{DDA}(ADC)$	ADC consumption from the V_{DDA} supply	$f_s = 5 \text{ Msps}$	-	730	830	μA
		$f_s = 1 \text{ Msps}$	-	160	220	
		$f_s = 10 \text{ ksps}$	-	16	50	
$I_{DDV_S}(ADC)$	ADC consumption from the V_{REF+} single ended mode	$f_s = 5 \text{ Msps}$	-	130	160	μA
		$f_s = 1 \text{ Msps}$	-	30	40	
		$f_s = 10 \text{ ksps}$	-	0.6	2	
$I_{DDV_D}(ADC)$	ADC consumption from the V_{REF+} differential mode	$f_s = 5 \text{ Msps}$	-	260	310	μA
		$f_s = 1 \text{ Msps}$	-	60	70	
		$f_s = 10 \text{ ksps}$	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4 \text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4\text{V}$). It is disable when $V_{DDA} \geq 2.4 \text{ V}$.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA} , depending on the package. Refer to [Section 4: Pinouts and pin description](#) for further details.

The maximum value of R_{AIN} can be found in [Table 78: Maximum ADC RAIN](#).

Table 81. ADC accuracy - limited test conditions 3⁽¹⁾(2)(3) (continued)

Sym- bol	Parameter	Conditions ⁽⁴⁾			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency $\leq$ 80 MHz, Sampling rate $\leq$ 5.33 Msps, $1.65\text{ V} \leq V_{\text{DDA}} = V_{\text{REF+}} \leq 3.6\text{ V}$, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{\text{DDA}} < 2.4\text{ V}$ (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{\text{DDA}} < 2.4\text{ V}$). It is disable when $V_{\text{DDA}} \geq 2.4\text{ V}$. No oversampling.

6.3.21 Comparator characteristics

Table 86. COMP characteristics⁽¹⁾

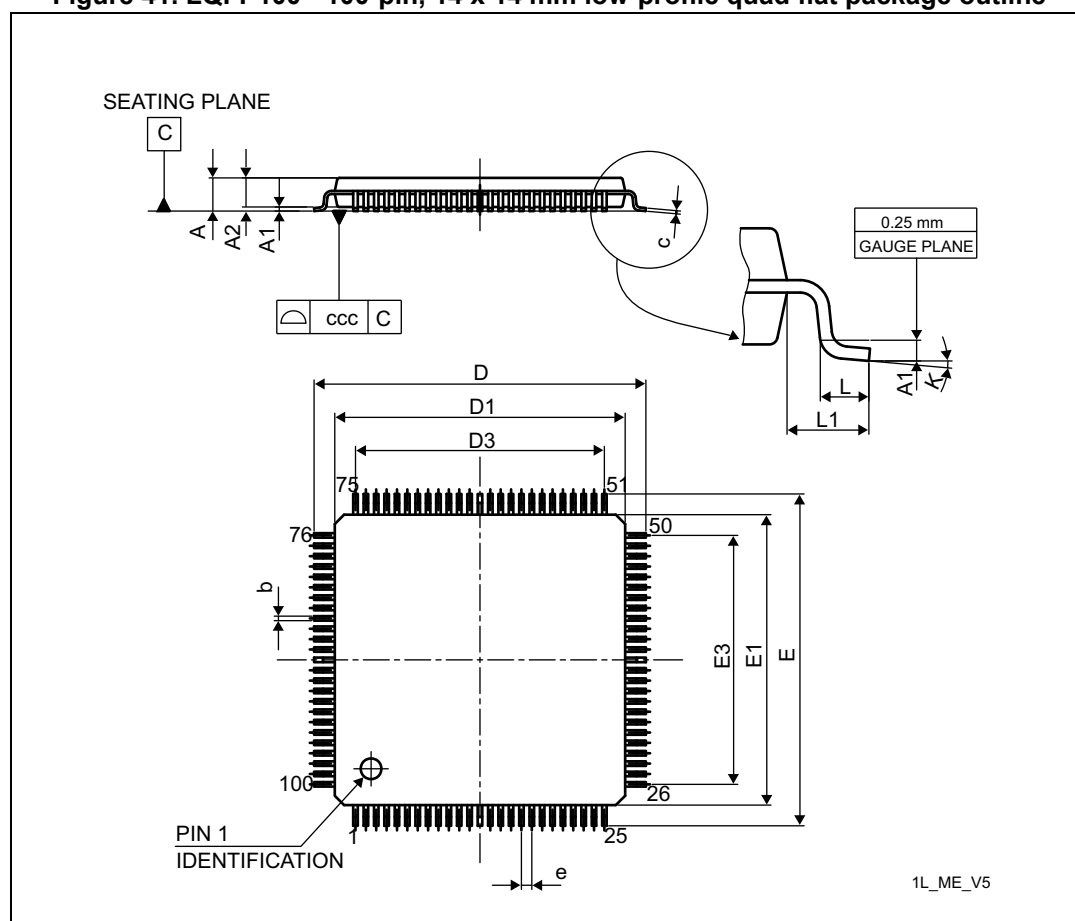
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V _{IN}	Comparator input voltage range	-		0	-	V _{DDA}	
V _{BG} ⁽²⁾	Scaler input voltage	-		V _{REFINT}			
V _{SC}	Scaler offset voltage	-		-	±5	±10	mV
I _{DDA} (SCALER)	Scaler static consumption from V _{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t _{START_SCALER}	Scaler startup time	-		-	100	200	µs
t _{START}	Comparator startup time to reach propagation delay specification	High-speed mode	V _{DDA} ≥ 2.7 V	-	-	5	µs
			V _{DDA} < 2.7 V	-	-	7	
		Medium mode	V _{DDA} ≥ 2.7 V	-	-	15	
			V _{DDA} < 2.7 V	-	-	25	
		Ultra-low-power mode		-	-	40	
t _D ⁽³⁾	Propagation delay with 100 mV overdrive	High-speed mode	V _{DDA} ≥ 2.7 V	-	55	80	ns
			V _{DDA} < 2.7 V	-	65	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V _{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V _{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 LQFP100 package information

Figure 41. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



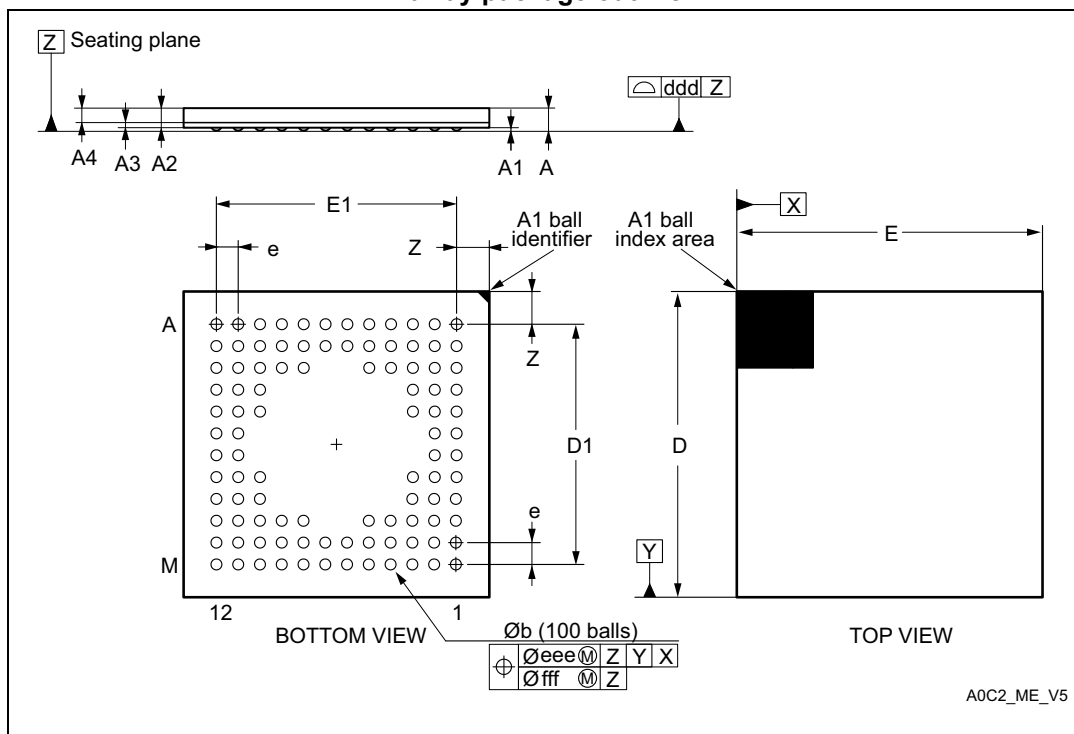
1. Drawing is not to scale.

Table 102. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059

7.2 UFBGA100 package information

Figure 44. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

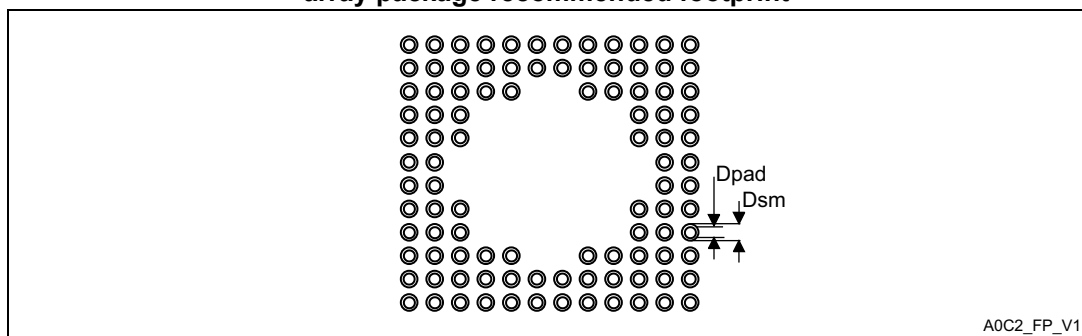
Table 103. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

Table 103. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint**Table 104. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Device marking

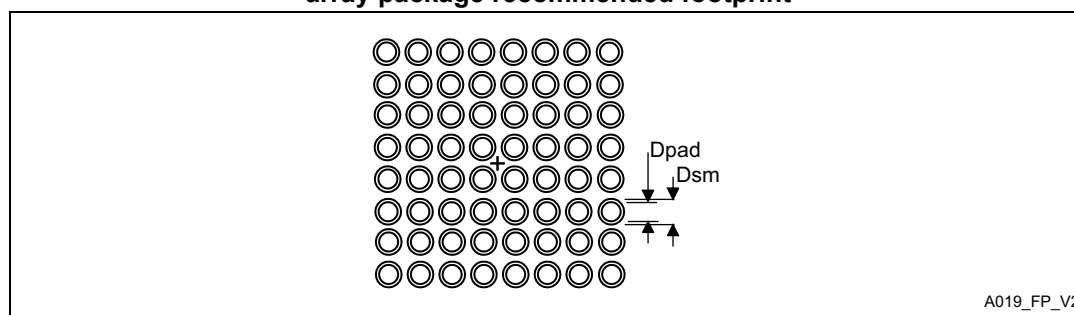
The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Table 106. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 51. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint**Table 107. UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm