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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l452rct6

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32L452xx family is compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the STM32L452xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.7 Boot modes

At startup, BOOT0 pin or nSWBOOT0 option bit, and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty check mechanism is implemented to force the boot from system flash if the first flash memory location is not programmed and if the boot selection is configured to boot from main flash.

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN or USB FS in Device mode through DFU (device firmware upgrade).

3.8 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.9 Power supply management

3.9.1 Power supply schemes

- V_{DD} = 1.71 to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- V_{DD12} = 1.05 to 1.32 V: external power supply bypassing internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option. VDD12 does not require any external decoupling capacitance and cannot support any external load.
- V_{DDA} = 1.62 V (ADC/COMPs) / 1.8 (DAC/OPAMP) / 2.4 V (VREFBUF) to 3.6 V: external analog power supply for ADC, DAC, OPAMP, Comparators and Voltage reference buffer. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- V_{DDUSB} = 3.0 to 3.6 V: external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
- V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: When the functions supplied by V_{DDA} are not used, this supply should preferably be shorted to V_{DD}.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 21 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.21 Digital filter for Sigma-Delta Modulators (DFSDM)

The device embeds one DFSDM with 2 digital filters modules and 4 external input serial channels (transceivers) or alternately 4 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in

3.26 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L452xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and one universal asynchronous receiver transmitters (UART4).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2 and USART3 also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4) to wake up the MCU from Stop mode using baudrates up to 204 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 13. STM32L452xx USART/UART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	UART4	LPUART1
Hardware flow control for modem	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X
Synchronous mode	X	X	X	-	-
Smartcard mode	X	X	X	-	-
Single-wire half-duplex communication	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	-
LIN mode	X	X	X	X	-
Dual clock domain	X	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	-	X
Receiver timeout interrupt	X	X	X	X	-
Modbus communication	X	X	X	X	-
Auto baud rate detection	X (4 modes)				-
Driver Enable	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits				

1. X = supported.

3.35 Development support

3.35.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

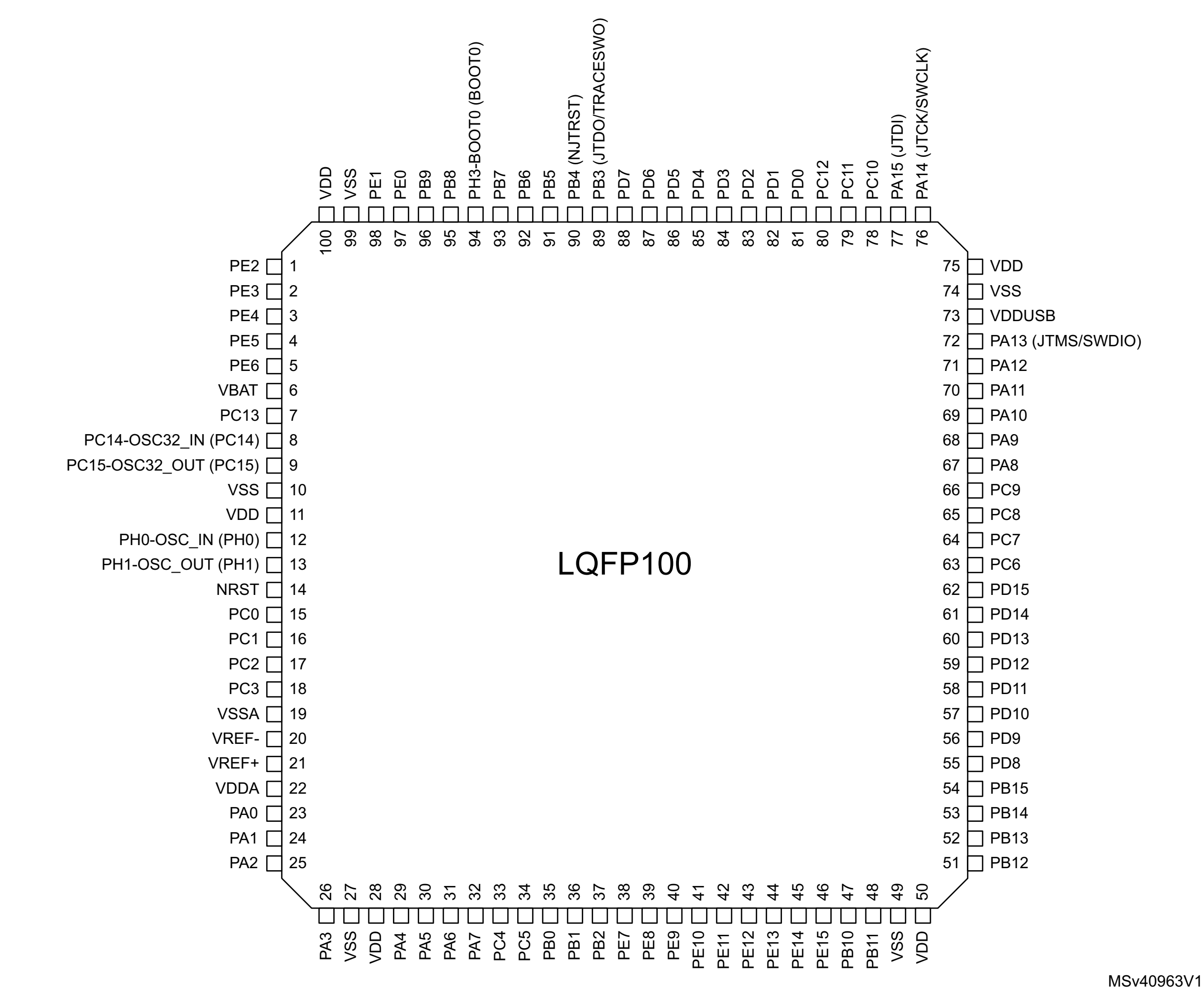
3.35.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell™ provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L452xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell™ operates with third party debugger software tools.

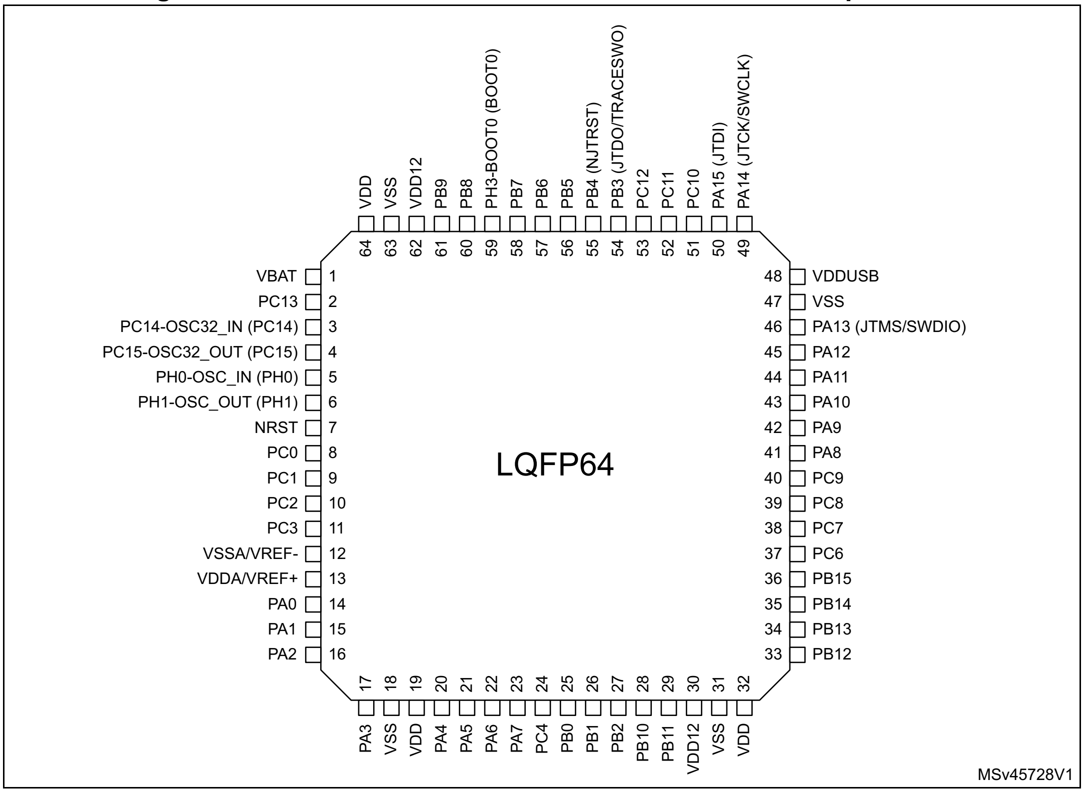
4 Pinouts and pin description

Figure 6. STM32L452Vx LQFP100 pinout[(1)]



1. The above figure shows the package top view.

Figure 9. STM32L452Rx, external SMPS device, LQFP64 pinout[1]



1. The above figure shows the package top view.

Figure 10. STM32L452Rx UFBGA64 ballout[1]

	1	2	3	4	5	6	7	8
A	PC14-OSC32_IN (PC14)	PC13	PB9	PB4 (NJTRST)	PB3 (JTDO/ TRACESWO)	PA15 (JTDI)	PA14 (JTCK/ SWCLK)	PA13 (JTMS/ SWDIO)
B	PC15-OSC32_OUT (PC15)	VBAT	PB8	PH3-BOOT0 (BOOT0)	PD2	PC11	PC10	PA12
C	PH0-OSC_IN (PH0)	VSS	PB7	PB5	PC12	PA10	PA9	PA11
D	PH1-OSC_OUT (PH1)	VDD	PB6	VSS	VSS	VSS	PA8	PC9
E	NRST	PC1	PC0	VDD	VDDUSB	VDD	PC7	PC8
F	VSSA/VREF-	PC2	PA2	PA5	PB0	PC6	PB15	PB14
G	PC3	PA0	PA3	PA6	PB1	PB2	PB10	PB13
H	VDDA/VREF+	PA1	PA4	PA7	PC4	PC5	PB11	PB12

MSv40959V1

1. The above figure shows the package top view.

Table 17. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2 LPTIM1	I2C4/TIM1/ TIM2/TIM3	I2C4/USART2/ CAN1/TIM1	I2C1/I2C2/ I2C3/I2C4	SPI1/SPI2/I2C4	SPI3/DFSDM/ COMP1	USART1/ USART2/ USART3
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH3	-	-	-	-	-	-	-	-

1. Please refer to *Table 18* for AF8 to AF15.

Table 20. Voltage characteristics(1) (continued)

Symbol	Ratings	Min	Max	Unit
$\|\Delta V_{DDx}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins(5)	-	50	mV

1. All main power (V_{DD}, V_{DDA}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 21: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 21. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)(2)	140	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	140	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(3)	100	
	Total output current sourced by sum of all I/Os and control pins(3)	100	
$I_{INJ(PIN)}$(4)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(5)	
	Injected current on PA4, PA5	-5/0	
$\sum\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)(6)	25	

1. All main power (V_{DD}, V_{DDA}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. Valid also for V_{DD12} on SMPS packages.
3. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
4. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 20: Voltage characteristics* for the maximum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP					MAX[1]					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.35	2.40	2.50	2.65	3.00	2.65	2.75	2.90	3.20	3.75	mA
				16 MHz	1.50	1.55	1.65	1.80	2.15	1.70	1.75	1.95	2.20	2.80	
				8 MHz	0.815	0.845	0.940	1.10	1.45	0.95	1.00	1.15	1.45	2.00	
				4 MHz	0.465	0.495	0.595	0.760	1.10	0.55	0.60	0.75	1.05	1.60	
				2 MHz	0.295	0.320	0.420	0.580	0.910	0.35	0.40	0.55	0.85	1.40	
				1 MHz	0.205	0.235	0.330	0.495	0.825	0.25	0.30	0.45	0.75	1.30	
				100 kHz	0.130	0.155	0.250	0.415	0.745	0.15	0.25	0.40	0.65	1.25	
			Range 1	80 MHz	8.45	8.50	8.65	8.90	9.25	9.45	9.50	9.75	10.10	10.75	
				72 MHz	7.65	7.70	7.85	8.05	8.45	8.50	8.60	8.80	9.15	9.85	
				64 MHz	6.80	6.85	7.00	7.20	7.60	7.60	7.70	7.90	8.25	8.90	
				48 MHz	5.10	5.15	5.25	5.45	5.85	5.70	5.80	6.00	6.35	7.00	
				32 MHz	3.45	3.50	3.60	3.80	4.20	3.85	3.95	4.15	4.50	5.15	
				24 MHz	2.60	2.65	2.80	2.95	3.35	2.95	3.05	3.20	3.55	4.20	
				16 MHz	1.80	1.85	1.95	2.15	2.50	2.00	2.10	2.30	2.60	3.25	
I_{DD_ALL} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	225	260	365	550	900	275	335	470	770	1400	µA
				1 MHz	130	160	270	450	800	170	225	375	670	1300	
				400 kHz	73.0	99.5	205	385	735	105	165	325	600	1250	
				100 kHz	38.0	71.0	175	355	705	70	140	315	565	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 31. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.40	2.40	2.55	2.70	3.05	2.70	2.75	2.90	3.20	3.80	mA
				16 MHz	1.50	1.55	1.65	1.80	2.15	1.70	1.80	1.95	2.25	2.80	
				8 MHz	0.820	0.850	0.950	1.10	1.45	0.95	1.00	1.15	1.45	2.00	
				4 MHz	0.470	0.500	0.600	0.765	1.10	0.55	0.60	0.75	1.05	1.60	
				2 MHz	0.295	0.325	0.420	0.585	0.915	0.35	0.40	0.55	0.85	1.40	
				1 MHz	0.210	0.235	0.330	0.495	0.825	0.25	0.30	0.45	0.75	1.30	
				100 kHz	0.130	0.155	0.250	0.415	0.750	0.15	0.25	0.35	0.65	1.25	
			Range 1	80 MHz	8.55	8.60	8.75	8.95	9.35	9.55	9.65	9.85	10.5	11.0	
				72 MHz	7.70	7.80	7.90	8.15	8.50	8.60	8.70	8.90	9.25	9.95	
				64 MHz	6.90	6.95	7.10	7.30	7.70	7.70	7.75	7.95	8.35	9.00	
				48 MHz	5.15	5.20	5.30	5.55	5.90	5.75	5.85	6.05	6.40	7.05	
				32 MHz	3.45	3.50	3.65	3.85	4.25	3.90	4.00	4.20	4.50	5.15	
				24 MHz	2.65	2.70	2.80	3.00	3.40	3.00	3.05	3.25	3.55	4.20	
				16 MHz	1.80	1.85	1.95	2.15	2.55	2.05	2.10	2.30	2.60	3.25	
I_{DD_ALL} (LPRun)	Supply current in low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable FLASH in power-down		2 MHz	220	255	360	540	895	270	330	460	760	1400	µA
				1 MHz	120	155	260	440	795	165	215	370	660	1300	
				400 kHz	60.0	92.0	195	375	730	100	160	330	585	1250	
				100 kHz	36.0	62.5	165	345	695	63.0	130	305	555	1200	

1. Guaranteed by characterization results, unless otherwise specified.

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V
2. Reduced code used for characterization results provided in *Table 27*, *Table 29*, *Table 31*.

Table 35. Typical current consumption in Run, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS (V_{DD12} = 1.05 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	f_{HCLK} = 26 MHz	Reduced code(2)	0.92	mA	36	µA/MHz
				Coremark	1.04		40	
				Dhrystone 2.1	1.08		42	
				Fibonacci	1.02		39	
				While(1)	0.92		36	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.05 V
2. Reduced code used for characterization results provided in *Table 27*, *Table 29*, *Table 31*.

Table 43. Current consumption in Sleep, Flash ON and power supplied by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions[(1)]		TYP					Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	80 MHz	0.83	0.84	0.88	0.95	1.10	mA
			72 MHz	0.75	0.77	0.81	0.88	1.01	
			64 MHz	0.68	0.68	0.74	0.81	0.93	
			48 MHz	0.50	0.50	0.56	0.63	0.77	
			32 MHz	0.35	0.36	0.41	0.47	0.61	
			24 MHz	0.28	0.29	0.33	0.40	0.54	
			16 MHz	0.20	0.21	0.25	0.32	0.45	
			8 MHz	0.13	0.14	0.18	0.25	0.40	
			4 MHz	0.09	0.10	0.14	0.22	0.36	
			2 MHz	0.07	0.08	0.13	0.20	0.34	
			1 MHz	0.06	0.07	0.11	0.19	0.33	
			100 kHz	0.05	0.06	0.11	0.18	0.32	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V

Table 44. Current consumption in Low-power sleep modes, Flash in power-down

Symbol	Parameter	Conditions			TYP					MAX[(1)]					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	76.5	105	220	410	740	110	175	350	600	1250	µA
				1 MHz	54.0	81.0	195	385	715	81.5	155	325	570	1200	
				400 kHz	28.0	64.5	175	370	695	60.5	130	305	555	1200	
				100 kHz	21.5	55.0	170	360	690	58.5	120	300	550	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 45. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	2.05	5.40	19.0	44.0	97.0	4.00	11.5	41.5	100	220	µA
			2.4 V	2.10	5.45	19.0	44.5	98.5	4.05	11.5	42.0	100	225	
			3 V	2.05	5.55	19.5	45.0	100	4.10	12.0	43.0	105	230	
			3.6 V	2.05	5.65	20.0	46.5	105	4.20	12.0	44.0	105	235	
I_{DD_ALL} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	2.30	5.65	19.0	44.0	97.0	4.50	12.0	42.0	100	220	µA
			2.4 V	2.35	5.80	19.5	44.5	99.0	4.65	12.0	42.5	100	225	
			3 V	2.50	5.90	20.0	45.5	100	4.90	12.5	43.5	105	230	
			3.6 V	2.60	6.15	20.5	47.0	105	5.20	13.0	44.5	105	235	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	2.60	6.05	21.0	48.0	97.0	-	-	-	-	-	
			2.4 V	2.55	6.20	21.0	49.0	98.5	-	-	-	-	-	
			3 V	2.80	6.35	21.5	49.5	100	-	-	-	-	-	
			3.6 V	2.85	6.60	22.5	51.5	105	-	-	-	-	-	
		RTC clocked by LSE quartz[2] in low drive mode	1.8 V	2.40	5.70	19.0	44.5	98.0	-	-	-	-	-	
			2.4 V	2.50	5.85	19.5	45.0	99.5	-	-	-	-	-	
			3 V	2.60	6.00	20.0	46.0	100	-	-	-	-	-	
			3.6 V	2.65	6.25	20.5	47.0	105	-	-	-	-	-	
I_{DD_ALL} (wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1. See [3].	3 V	1.85	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See [3].	3 V	1.50	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI16 = 16 MHz, voltage Range 1. See [3].	3 V	1.55	-	-	-	-	-	-	-	-	-	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 79. ADC accuracy - limited test conditions 1(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 83. DAC characteristics[1] (continued)

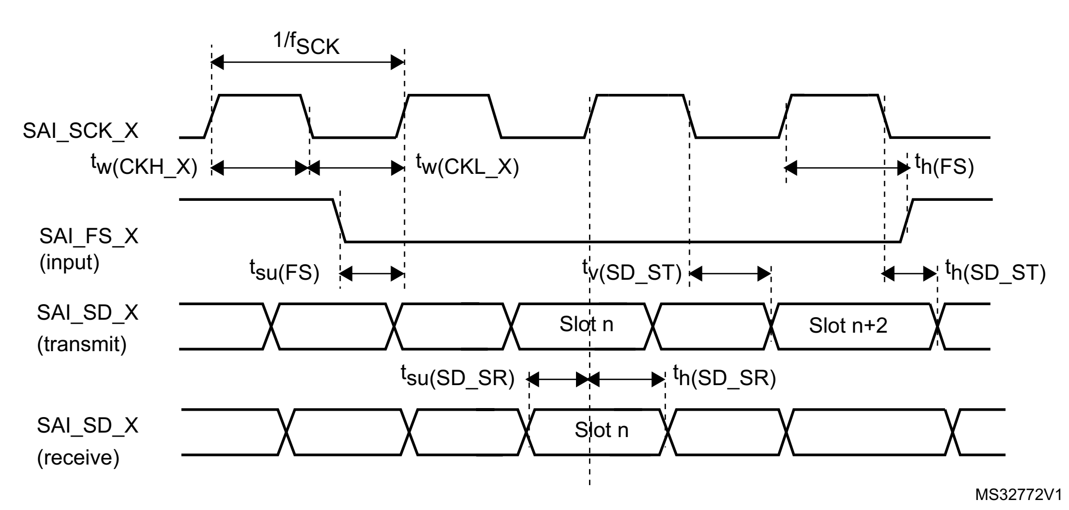
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W\_to\_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC1_OUT1 for a small variation of the input code (1 LSB)				-	-	µs
	DAC_MCR:MODEx[2:0] = 000 or 001	CL ≤ 50 pF, RL ≥ 5 kΩ		1			
	DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 10 pF		1.4			
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DAC1_OUT1 reaches final value ±1LSB)	DAC1_OUT1 pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC1_OUT1 pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC1_OUT1 pin connected		-	-	-[3]	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
$I_{DDA}(DAC)$	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff)[4]	670 x Ton/(Ton +Toff)[4]	

Table 94. I2C analog filter characteristics[(1)]

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50[(2)]	260[(3)]	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Figure 38. SAI slave timing waveforms



SDMMC characteristics

Unless otherwise specified, the parameters given in *Table 99* for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Table 99. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	2.5	-	-	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	12	13	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	10	-	-	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} = 50 MHz	3.5	-	-	ns
t_{IHD}	Input hold time SD	f_{PP} = 50 MHz	3	-	-	ns

Table 99. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} = 50 MHz	-	2	3	ns
t_{OHD}	Output hold default time SD	f_{PP} = 50 MHz	0	-	-	ns

1. Guaranteed by characterization results.

Table 100. eMMC dynamic characteristics, V_{DD} = 1.71 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	0	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	1.5	-	-	ns
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	13.5	15	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	9	-	-	ns

1. Guaranteed by characterization results.
2. C_{LOAD} = 20pF.

Figure 39. SDIO high-speed mode

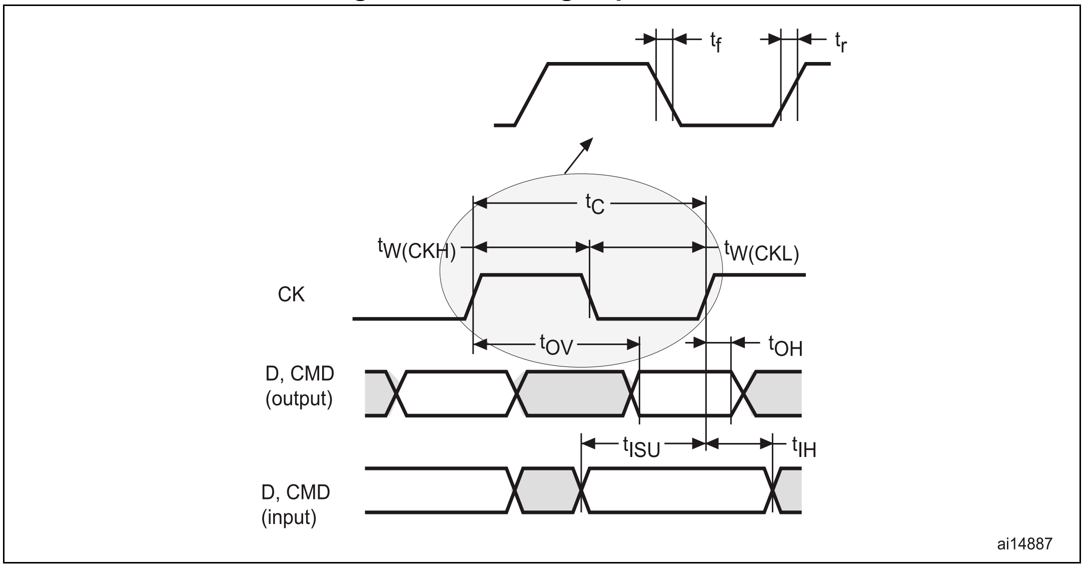


Table 113. Document revision history (continued)

Date	Revision	Changes
21-May-2018	4 (continued)	Updated *Table 51: Peripheral current consumption*. Added *Section 6.3.16: Extended interrupt and event controller input (EXTI) characteristics*. Updated *Table 71: I/O static characteristics*. Updated *Table 83: DAC characteristics*.