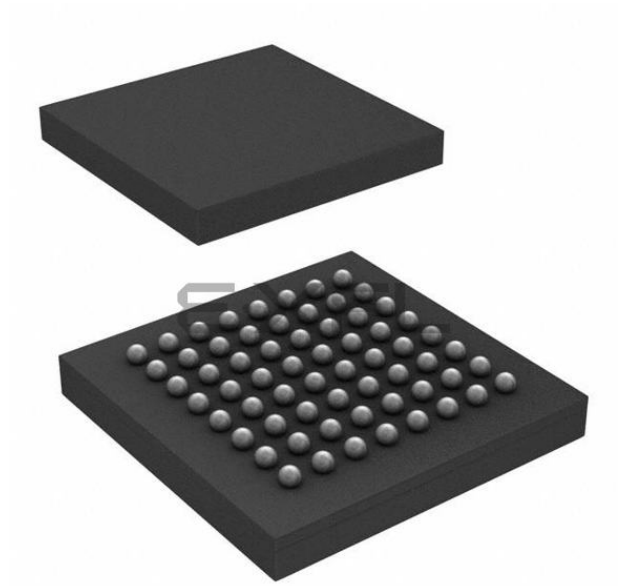

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l452rei3

List of figures

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32L452xx family is compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the STM32L452xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

Table 5. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application. Low frequency clocks (LSI, LSE) are available down to Stop 1 low power state.
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes down to Standby mode. LSE can also be output on LSCO in Shutdown mode. LSCO is not available in VBAT mode.

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 80 MHz.

Table 14. SAI implementation

SAI features	Support[1]
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X
Mute mode	X
Stereo/Mono audio frame capability.	X
16 slots	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X
FIFO Size	X (8 Word)
SPDIF	X

1. X: supported

3.30 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s
- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - 14 Scalable filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

3.31 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The card host interface (SDMMC) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

Table 16. STM32L452xx pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	LQFP64 SMPS	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	F3	39	39	E8	65	E10	PC8	I/O	FT	-	TIM3_CH3, TSC_G4_IO3, SDMMC1_D0, EVENTOUT	-
-	E2	40	40	D8	66	D12	PC9	I/O	FT	-	TIM3_CH4, TSC_G4_IO4, USB_NOE, SDMMC1_D1, EVENTOUT	-
29	E3	41	41	D7	67	D11	PA8	I/O	FT	-	MCO, TIM1_CH1, DFSDM1_CKIN1, USART1_CK, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
30	D1	42	42	C7	68	D10	PA9	I/O	FT_f	-	TIM1_CH2, I2C1_SCL, DFSDM1_DATIN1, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
31	C1	43	43	C6	69	C12	PA10	I/O	FT_f	-	TIM1_CH3, I2C1_SDA, USART1_RX, USB_CRS_SYNC, SAI1_SD_A, EVENTOUT	-
32	D2	44	44	C8	70	B12	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, COMP1_OUT, USART1_CTS, CAN1_RX, USB_DM, TIM1_BKIN2_COMP1, EVENTOUT	-
33	D3	45	45	B8	71	A12	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, USB_DP, EVENTOUT	-
34	C2	46	46	A8	72	A11	PA13 (JTMS/ SWDIO)	I/O	FT	(3)	JTMS/SWDAT, IR_OUT, USB_NOE, SAI1_SD_B, EVENTOUT	-
35	B1	47	47	D5	-	-	VSS	S	-	-	-	-
36	A1	48	48	E5	73	C11	VDDUSB	S	-	-	-	-
-	-	-	-	-	74	F11	VSS	S	-	-	-	-

Table 29. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.75	2.80	2.90	3.10	3.40	3.15	3.25	3.40	3.70	4.30	mA
				16 MHz	1.95	2.00	2.10	2.25	2.60	2.25	2.30	2.50	2.75	3.35	
				8 MHz	1.10	1.15	1.25	1.40	1.75	1.25	1.35	1.50	1.75	2.35	
				4 MHz	0.640	0.670	0.765	0.935	1.25	0.75	0.80	0.95	1.25	1.80	
				2 MHz	0.380	0.405	0.505	0.670	1.00	0.45	0.50	0.65	0.95	1.50	
				1 MHz	0.250	0.275	0.375	0.540	0.865	0.30	0.35	0.50	0.80	1.35	
				100 kHz	0.135	0.160	0.255	0.420	0.750	0.15	0.25	0.40	0.65	1.25	
			Range 1	80 MHz	8.85	8.90	9.05	9.30	9.70	10.0	10.5	10.5	11.0	11.5	
				72 MHz	8.00	8.05	8.20	8.40	8.85	9.05	9.15	9.35	9.70	10.5	
				64 MHz	7.90	7.95	8.10	8.35	8.75	8.95	9.10	9.35	9.70	10.5	
				48 MHz	6.60	6.65	6.80	7.05	7.45	7.55	7.65	7.90	8.30	9.00	
				32 MHz	4.75	4.80	4.95	5.15	5.55	5.40	5.50	5.75	6.10	6.80	
				24 MHz	3.60	3.65	3.80	4.00	4.35	4.10	4.20	4.40	4.75	5.40	
				16 MHz	2.60	2.65	2.75	2.95	3.35	3.00	3.05	3.25	3.60	4.25	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	340	360	470	650	1000	400	455	575	880	1550	µA
				1 MHz	175	215	320	500	855	225	285	420	720	1350	
				400 kHz	89.5	120	225	405	760	130	185	340	620	1250	
				100 kHz	42.5	75.5	180	360	715	75	145	320	575	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 42. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.700	0.730	0.830	1.00	1.35	0.80	0.90	1.05	1.30	1.90	mA
				16 MHz	0.475	0.505	0.605	0.775	1.10	0.55	0.65	0.80	1.05	1.65	
				8 MHz	0.300	0.325	0.425	0.590	0.920	0.35	0.45	0.60	0.85	1.45	
				4 MHz	0.210	0.235	0.335	0.500	0.830	0.25	0.30	0.45	0.75	1.35	
				2 MHz	0.165	0.190	0.290	0.455	0.785	0.20	0.25	0.40	0.70	1.25	
				1 MHz	0.145	0.170	0.265	0.430	0.760	0.15	0.25	0.40	0.65	1.25	
				100 kHz	0.125	0.150	0.245	0.410	0.740	0.15	0.20	0.35	0.65	1.20	
			Range 1	80 MHz	2.30	2.35	2.45	2.65	3.05	2.55	2.65	2.85	3.15	3.80	
				72 MHz	2.10	2.15	2.25	2.45	2.80	2.35	2.40	2.60	2.90	3.55	
				64 MHz	1.90	1.90	2.05	2.25	2.60	2.10	2.20	2.35	2.70	3.35	
				48 MHz	1.40	1.40	1.55	1.75	2.15	1.60	1.65	1.85	2.15	2.80	
				32 MHz	0.970	1.00	1.15	1.30	1.70	1.10	1.20	1.40	1.70	2.35	
				24 MHz	0.765	0.800	0.920	1.10	1.50	0.90	0.95	1.15	1.45	2.10	
				16 MHz	0.555	0.590	0.705	0.895	1.25	0.65	0.75	0.90	1.20	1.85	
I_{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	76.0	110	215	395	745	120	185	355	610	1250	µA
				1 MHz	54.0	86.5	195	370	725	88.5	160	335	585	1250	
				400 kHz	39.0	70.5	175	355	710	68.5	140	320	570	1200	
				100 kHz	35.5	75.0	195	345	715	66.0	130	305	560	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 47. Current consumption in Stop 0

Symbol	Parameter	Conditions	TYP					MAX(1)					Unit
		V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 0)	Supply current in Stop 0 mode, RTC disabled	1.8 V	125	150	240	390	645	145	190	350	600	1150	µA
		2.4 V	125	150	240	390	645	150	195	355	605	1150	
		3 V	125	150	245	395	650	155	195	360	610	1150	
		3.6 V	125	155	245	400	655	155	200	365	615	1150(2)	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 71: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 51: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

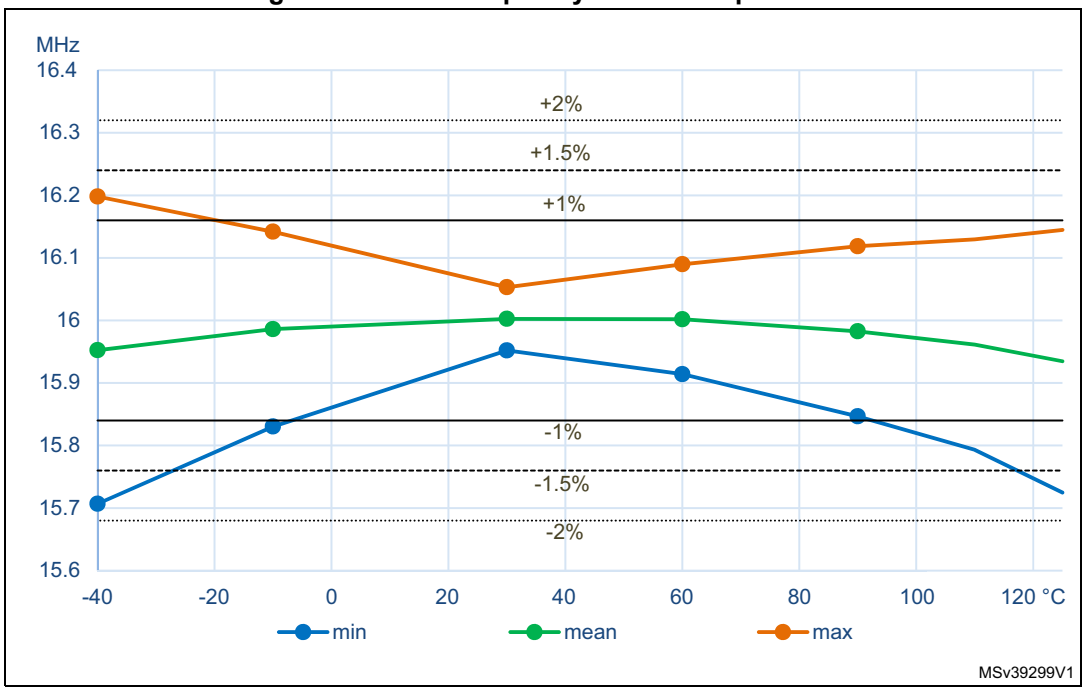
f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Figure 23. HSI16 frequency versus temperature



In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 20: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 20: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 72. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\lvert I_{IO}\rvert$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\lvert I_{IO}\rvert$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 4 mA $V_{DDIOx} \geq 1.62$ V	-	0.45	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-0.45	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	$0.35_x V_{DDIOx}$	
V_{OH}(3)	Output high level voltage for an I/O pin		$0.65_x V_{DDIOx}$	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\lvert I_{IO}\rvert$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\lvert I_{IO}\rvert$ = 10 mA $V_{DDIOx} \geq 1.62$ V	-	0.4	
		$\lvert I_{IO}\rvert$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 20: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 27* and *Table 73*, respectively.

Table 81. ADC accuracy - limited test conditions 3(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

6.3.21 Comparator characteristics

Table 86. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	40	
t_D(3)	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	

Table 87. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(3)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(3)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(3)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

6.3.24 V_{BAT} monitoring characteristics

Table 89. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 90. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.25 Timer characteristics

The parameters given in the following tables are guaranteed by design.

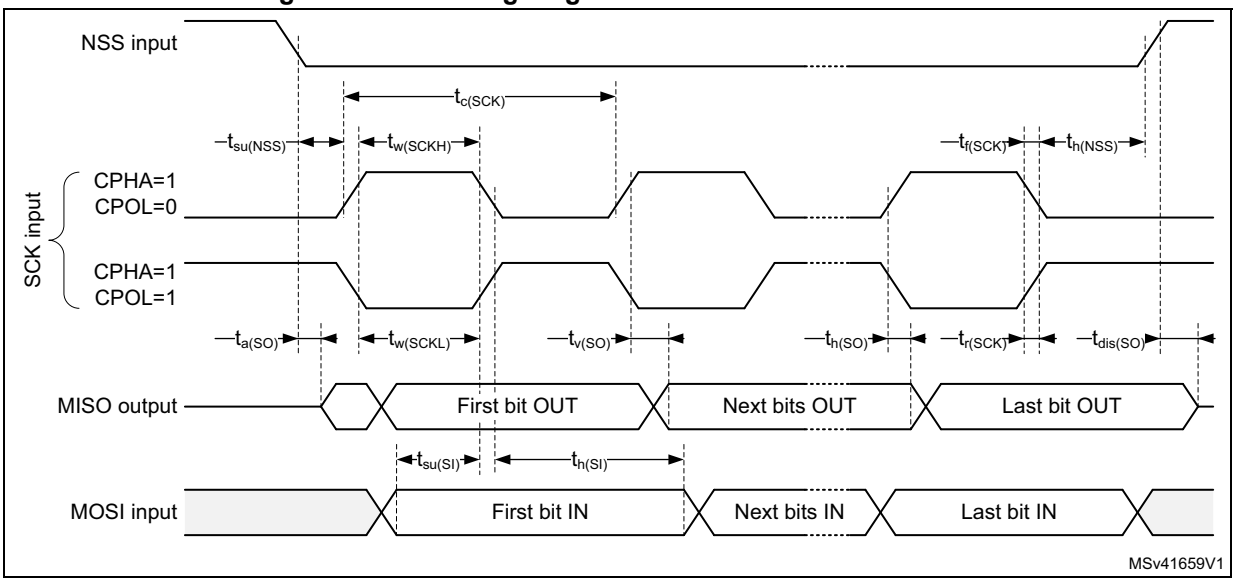
Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 91. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	12.5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 80 MHz	0	40	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	0.0125	819.2	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	-	53.68	s

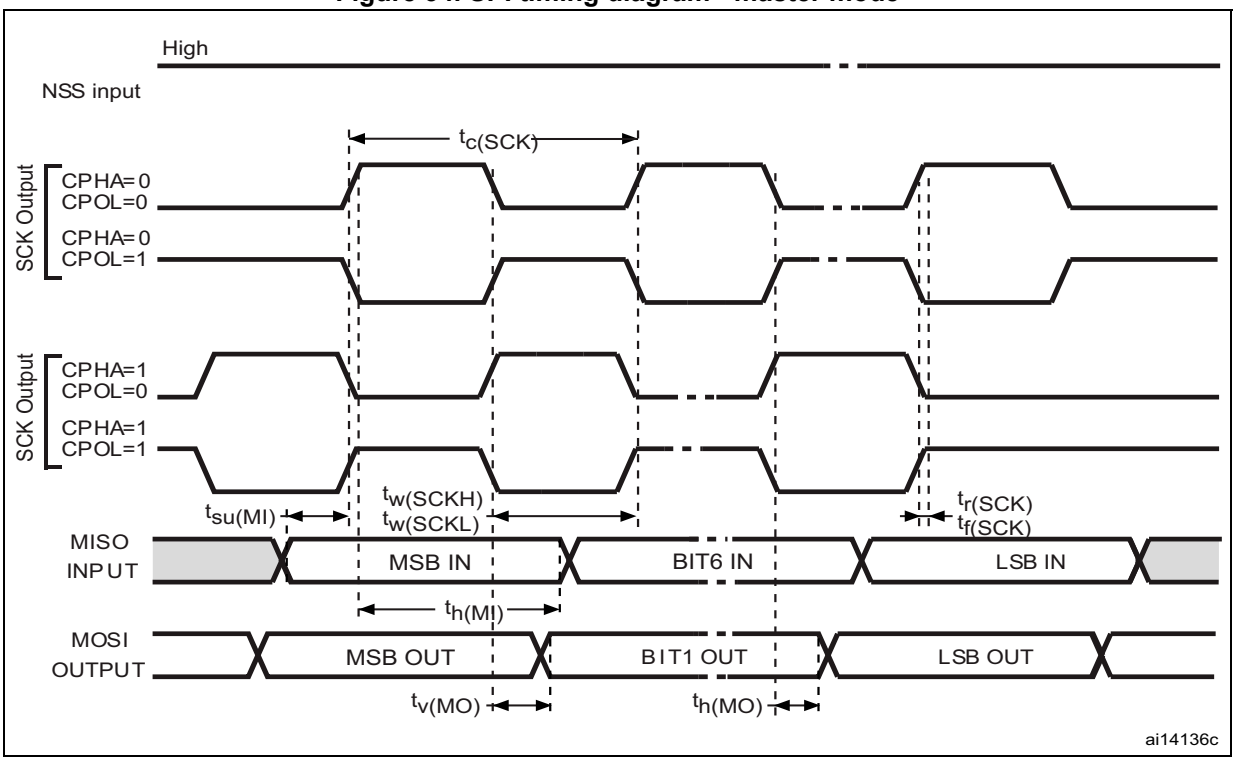
1. TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Figure 33. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 34. SPI timing diagram - master mode



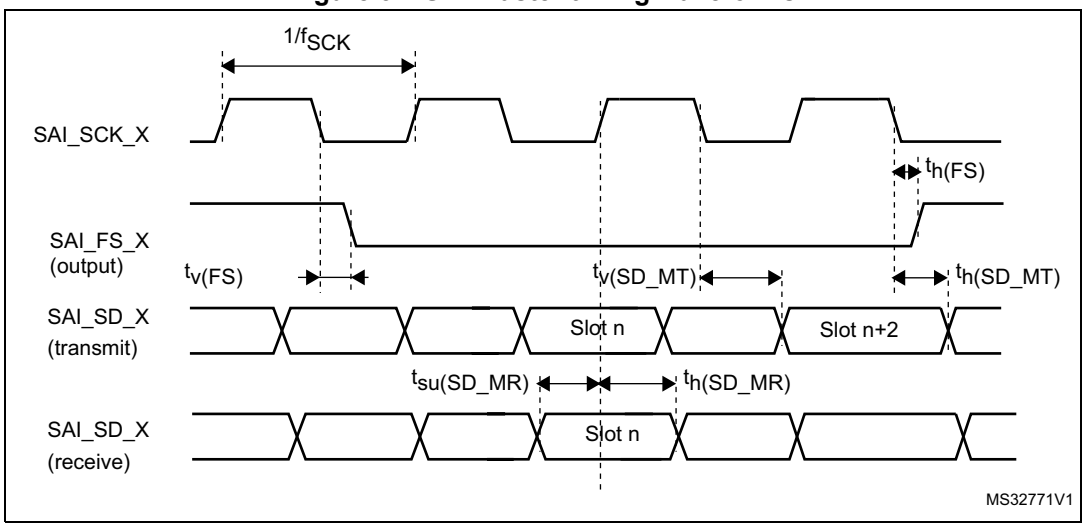
1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 98. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 ≤ V_{DD} ≤ 3.6	-	22	ns
		Slave transmitter (after enable edge) 1.71 ≤ V_{DD} ≤ 3.6	-	34	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	ns
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 ≤ V_{DD} ≤ 3.6	-	27	ns
		Master transmitter (after enable edge) 1.71 ≤ V_{DD} ≤ 3.6	-	40	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	ns

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 37. SAI master timing waveforms

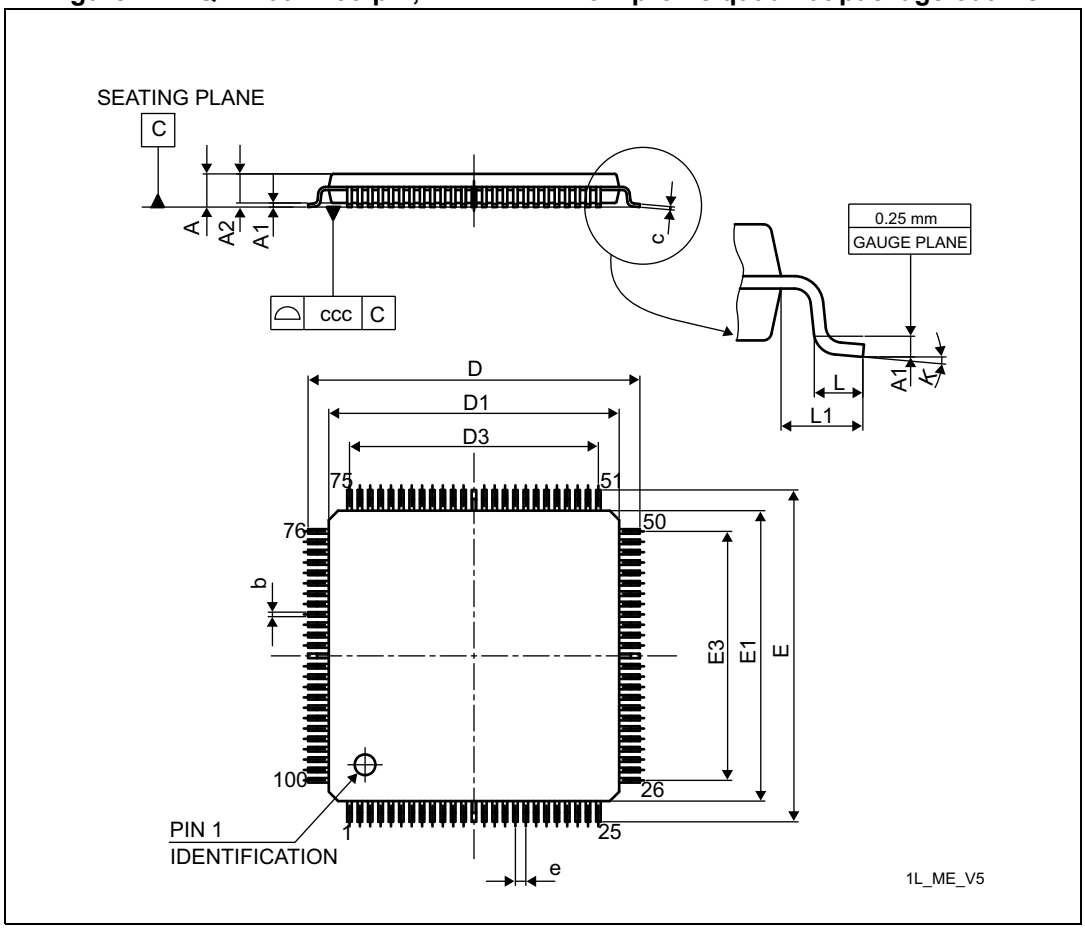


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100 package information

Figure 41. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 102. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

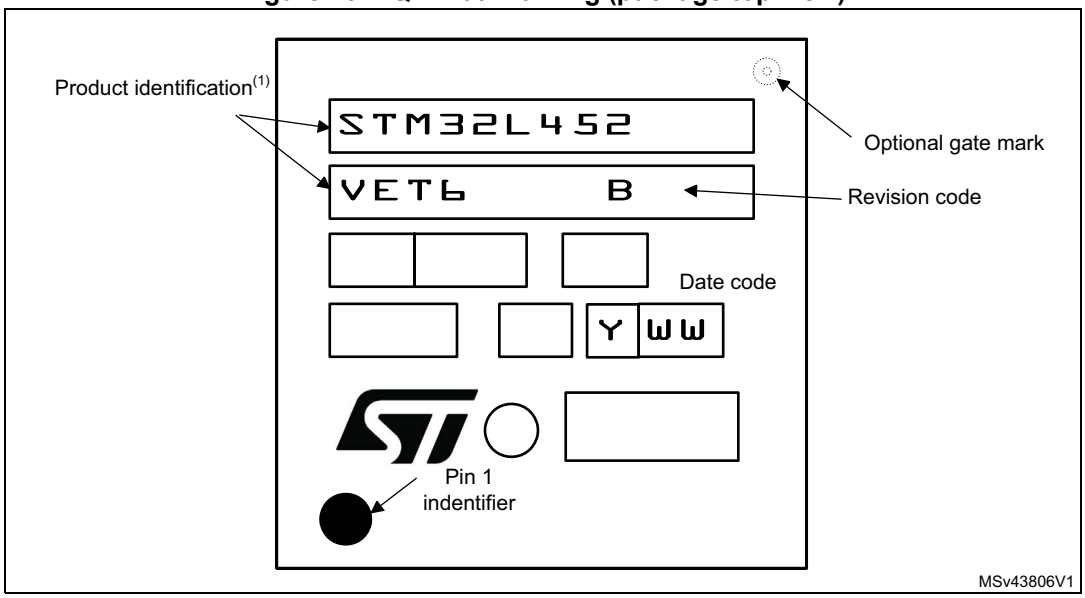
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 43. LQFP100 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.