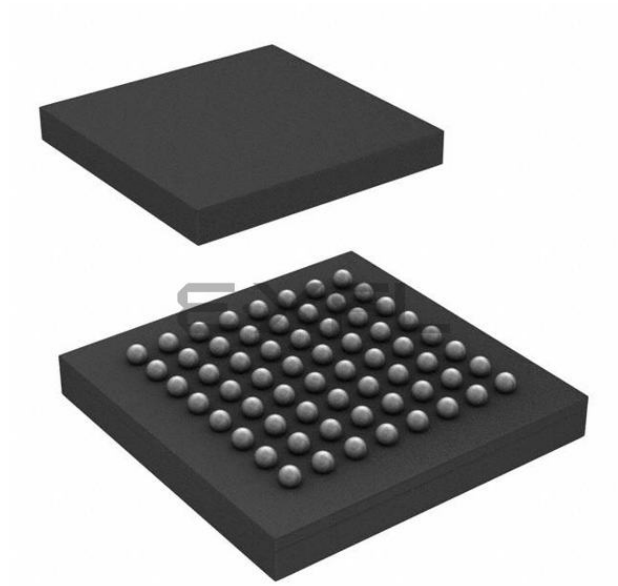

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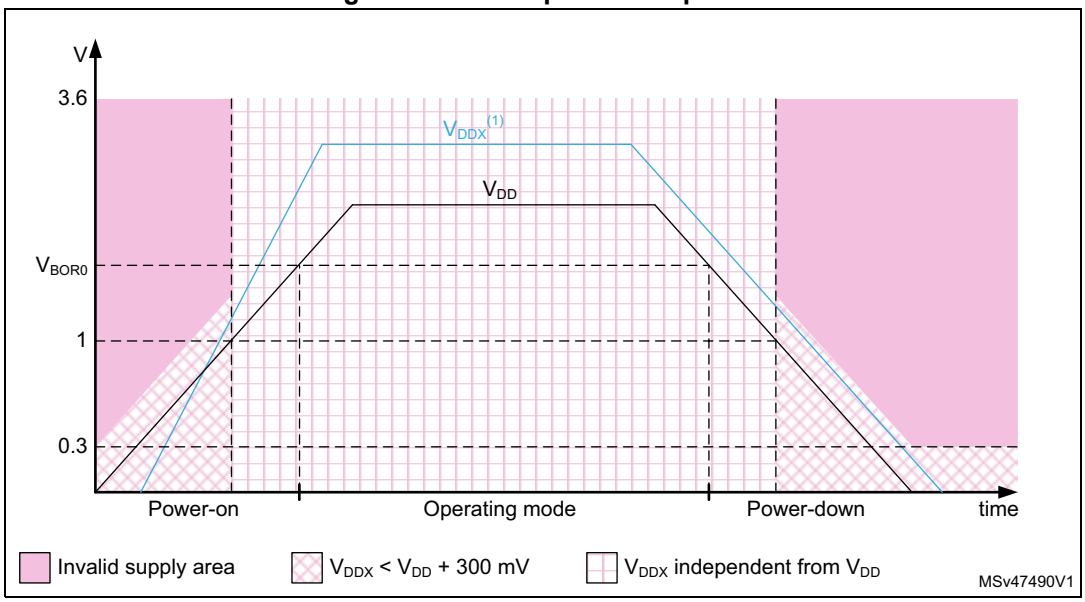
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l452rei6

Table 2. STM32L452xx family device features and peripheral counts

Peripheral		STM32L452Vx		STM32L452Rx		STM32L452Cx	
Flash memory		256KB	512KB	256KB	512KB	256KB	512KB
SRAM		160KB					
Quad SPI		Yes					
Timers	Advanced control	1 (16-bit)					
	General purpose	2 (16-bit) 1 (32-bit)					
	Basic	2 (16-bit)					
	Low -power	2 (16-bit)					
	SysTick timer	1					
	Watchdog timers (independent, window)	2					
Comm. interfaces	SPI	3					
	I^2C	4					
	USART UART LPUART	3 1 1					
	SAI	1					
	CAN	1					
	USB FS	Yes					
	SDMMC	Yes(1)				No	
RTC		Yes					
Tamper pins		3		2		2	
Random generator		Yes					
GPIOs(2) Wakeup pins		83 5		52 4(1)		38 3	
Capacitive sensing Number of channels		21		12		6	
12-bit ADC Number of channels		1 16		1 16(1)		1 10	
12-bit DAC channels		1					
Internal voltage reference buffer		Yes		No			
Analog comparator		2					
Operational amplifiers		1					
Max. CPU frequency		80 MHz					

Figure 3. Power-up/down sequence



1. V_{DDX} refers to V_{DDA}.

3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the device embeds a Peripheral Voltage Monitor which compares the independent supply voltage V_{DDA} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

without having any impact on the timing of “injected” conversions

– “injected” conversions for precise timing and with high conversion priority

Table 10. DFSDM1 implementation

DFSDM features	DFSDM1
Number of channels	8
Number of filters	4
Input from internal ADC	-
Supported trigger sources	10
Pulses skipper	-
ID registers support	-

3.22 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.23 Timers and watchdogs

The STM32L452xx includes one advanced control timers, up to five general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 11. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

3.32 Universal serial bus (USB)

The STM32L452xx devices embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.33 Clock recovery system (CRS)

The STM32L452xx devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.34 Quad SPI memory interface (QUADSPI)

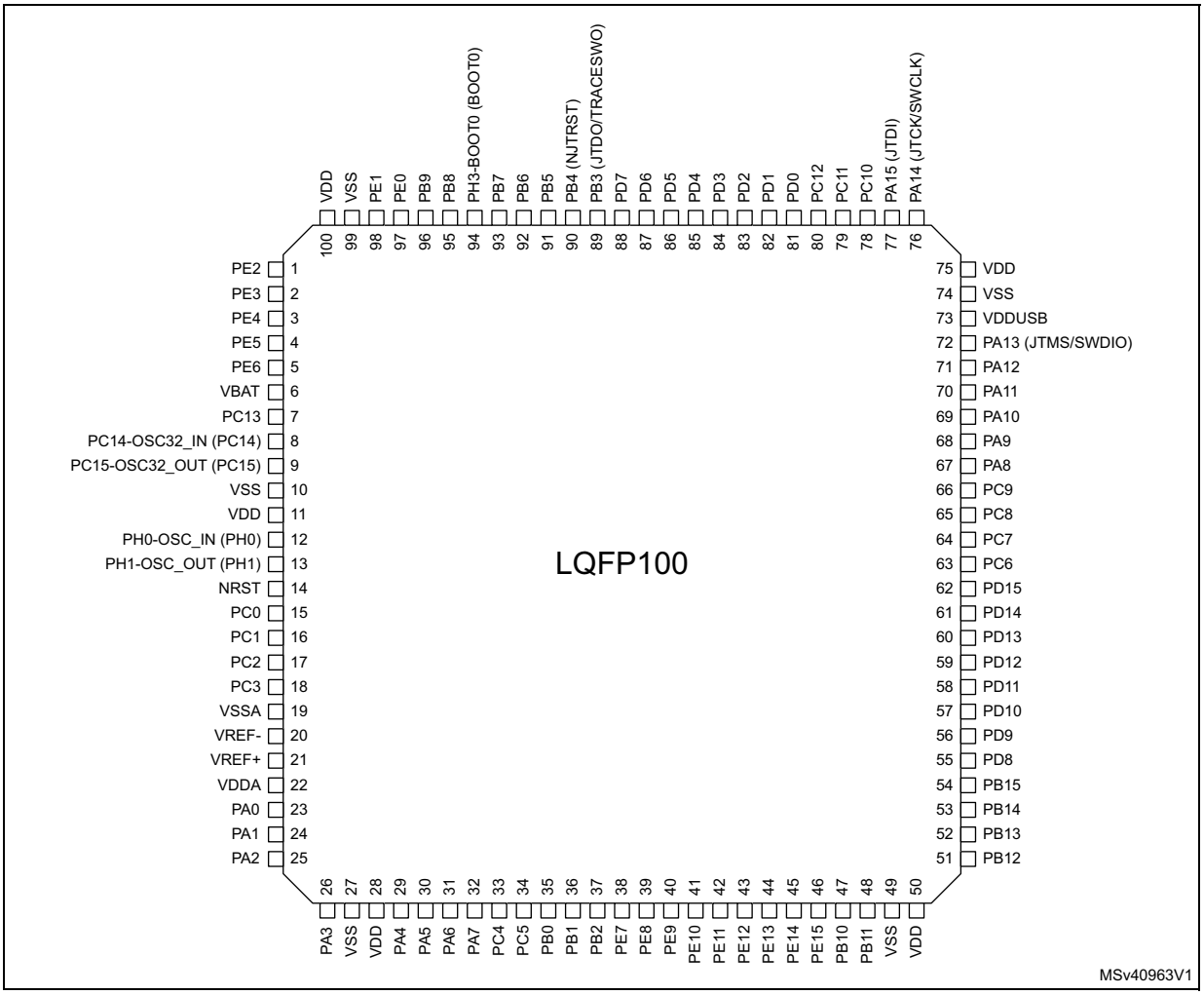
The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory

Both throughput and capacity can be increased two-fold using dual-flash mode, where two Quad SPI flash memories are accessed simultaneously.

4 Pinouts and pin description

Figure 6. STM32L452Vx LQFP100 pinout(1)



1. The above figure shows the package top view.

Table 16. STM32L452xx pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	LQFP64 SMPS	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	4	C2	PE5	I/O	FT	-	TRACED2, TIM3_CH3, DFSDM1_CKIN3, TSC_G7_IO4, SAI1_SCK_A, EVENTOUT	-
-	-	-	-	-	5	D2	PE6	I/O	FT	-	TRACED3, TIM3_CH4, SAI1_SD_A, EVENTOUT	RTC_TAMP3/WKUP3
1	B7	1	1	B2	6	E2	VBAT	S	-	-	-	-
2	B8	2	2	A2	7	C1	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1/RTC_TS/ RTC_OUT/WKUP2
3	C8	3	3	A1	8	D1	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
4	C7	4	4	B1	9	E1	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	-	-	-	-	10	F2	VSS	S	-	-	-	-
-	-	-	-	-	11	G2	VDD	S	-	-	-	-
5	D8	5	5	C1	12	F1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	E8	6	6	D1	13	G1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	F8	7	7	E1	14	H2	NRST	I/O	RST	-	-	-
-	D7	8	8	E3	15	H1	PC0	I/O	FT_fa	-	LPTIM1_IN1, I2C4_SCL, I2C3_SCL, LPUART1_RX, LPTIM2_IN1, EVENTOUT	ADC1_IN1
-	D5	9	9	E2	16	J2	PC1	I/O	FT_fa	-	TRACED0, LPTIM1_OUT, I2C4_SDA, I2C3_SDA, LPUART1_TX, EVENTOUT	ADC1_IN2

Table 17. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2 LPTIM1	I2C4/TIM1/ TIM2/TIM3	I2C4/USART2/ CAN1/TIM1	I2C1/I2C2/ I2C3/I2C4	SPI1/SPI2/I2C4	SPI3/DFSDM/ COMP1	USART1/ USART2/ USART3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	-	-	SPI1_NSS	DFSDM1_ CKIN0	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	-	-	-	DFSDM1_ DATIN0	USART3_RTS_ DE
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM1_ CKIN0	-
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_ DE
	PB4	NJTRST	-	TIM3_CH1	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS
	PB5	-	LPTIM1_IN1	TIM3_CH2	CAN1_RX	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	-	-	I2C1_SCL	I2C4_SCL	-	USART1_TX
	PB7	-	LPTIM1_IN2	-	-	I2C1_SDA	I2C4_SDA	-	USART1_RX
	PB8	-	-	-	-	I2C1_SCL	-	-	-
	PB9	-	IR_OUT	-	-	I2C1_SDA	SPI2_NSS	-	-
	PB10	-	TIM2_CH3	-	I2C4_SCL	I2C2_SCL	SPI2_SCK	-	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	-	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN_C OMP2	I2C2_SMBA	SPI2_NSS	DFSDM1_ DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM1_ CKIN1	USART3_CTS
	PB14	-	TIM1_CH2N	-	-	I2C2_SDA	SPI2_MISO	DFSDM1_ DATIN2	USART3_RTS_ DE
	PB15	RTC_REFIN	TIM1_CH3N	-	-	-	SPI2_MOSI	DFSDM1_ CKIN2	-

Table 17. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2 LPTIM1	I2C4/TIM1/ TIM2/TIM3	I2C4/USART2/ CAN1/TIM1	I2C1/I2C2/ I2C3/I2C4	SPI1/SPI2/I2C4	SPI3/DFSDM/ COMP1	USART1/ USART2/ USART3
Port E	PE0	-	-	-	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	-	-	-	DFSDM1_ DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	-	-	-	DFSDM1_ CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_ DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_ CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_ CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	-	-
	PE11	-	TIM1_CH2	-	-	-	-	-	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	-	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	-	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-

Table 18. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/ LPUART1/ CAN1	CAN1/TSC	CAN1/USB/ QUADSPI	-	SDMMC1/ COMP1/ COMP2	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port B	PB0	-	-	QUADSPI_ BK1_IO1	-	COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_RTS _DE	-	QUADSPI_ BK1_IO0	-	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	-	-	-	-	-	EVENTOUT
	PB3	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PB4	-	TSC_G2_IO1	-	-	-	SAI1_MCLK_B	-	EVENTOUT
	PB5	-	TSC_G2_IO2	-	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	CAN1_TX	TSC_G2_IO3	-	-	-	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	-	-	-	-	-	EVENTOUT
	PB8	-	CAN1_RX	-	-	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	-	CAN1_TX	-	-	SDMMC1_D5	SAI1_FS_A	-	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	QUADSPI_CLK	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	QUADSPI_ BK1_NCS	-	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RTS _DE	TSC_G1_IO1	CAN1_RX	-	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CTS	TSC_G1_IO2	CAN1_TX	-	-	SAI1_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	-	-	SAI1_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	-	-	SAI1_SD_A	TIM15_CH2	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 14*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 15*.

Figure 14. Pin loading conditions

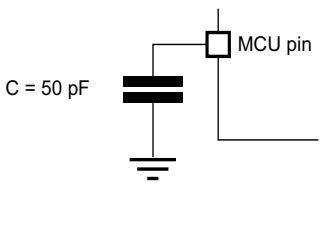


Figure 15. Pin input voltage

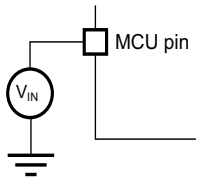


Table 23. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(5)	–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation	–40	125	
		Low-power dissipation(5)	–40	130	
T_J	Junction temperature range	Suffix 6 version	–40	105	°C
		Suffix 3 version	–40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between Min(V_{DD}, V_{DDA}, V_{DDUSB})+3.6 V and 5.5V.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDUSB}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 24* are derived from tests performed under the ambient temperature condition summarized in *Table 23*.

Table 24. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	µs/V
	V_{DDUSB} fall time rate		10	∞	

The requirements for power-up/down sequence specified in *Section 3.9.1: Power supply schemes* must be respected.

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 25* are derived from tests performed under the ambient temperature conditions summarized in *Table 23: General operating conditions*.

Table 25. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs

6.3.4 Embedded voltage reference

The parameters given in *Table 26* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 26. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 38. Typical current consumption in Run modes, with different codesrunning from Flash, ART disable and power supplied by external SMPS (V_{DD12} = 1.05 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals	f_{HCLK} = 26 MHz	Reduced code(2)	1.08	mA	42	µA/MHz
				Coremark	0.98		38	
				Dhrystone 2.1	0.98		38	
				Fibonacci	0.90		35	
				While(1)	0.86		33	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.05 V
2. Reduced code used for characterization results provided in *Table 27*, *Table 29*, *Table 31*.

Table 39. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	2.40	mA	92	µA/MHz
				Coremark	2.20		85	
				Dhrystone 2.1	2.35		90	
				Fibonacci	2.20		85	
				While(1)	2.30		88	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	8.55	mA	107	µA/MHz
				Coremark	7.75		97	
				Dhrystone 2.1	8.45		106	
				Fibonacci	7.80		98	
				While(1)	8.75		109	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2 MHz all peripherals disable		Reduced code(1)	220	µA	110	µA/MHz
				Coremark	190		95	
				Dhrystone 2.1	215		108	
				Fibonacci	200		100	
				While(1)	210		105	

1. Reduced code used for characterization results provided in *Table 27*, *Table 29*, *Table 31*.

Table 42. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.700	0.730	0.830	1.00	1.35	0.80	0.90	1.05	1.30	1.90	mA
				16 MHz	0.475	0.505	0.605	0.775	1.10	0.55	0.65	0.80	1.05	1.65	
				8 MHz	0.300	0.325	0.425	0.590	0.920	0.35	0.45	0.60	0.85	1.45	
				4 MHz	0.210	0.235	0.335	0.500	0.830	0.25	0.30	0.45	0.75	1.35	
				2 MHz	0.165	0.190	0.290	0.455	0.785	0.20	0.25	0.40	0.70	1.25	
				1 MHz	0.145	0.170	0.265	0.430	0.760	0.15	0.25	0.40	0.65	1.25	
				100 kHz	0.125	0.150	0.245	0.410	0.740	0.15	0.20	0.35	0.65	1.20	
			Range 1	80 MHz	2.30	2.35	2.45	2.65	3.05	2.55	2.65	2.85	3.15	3.80	
				72 MHz	2.10	2.15	2.25	2.45	2.80	2.35	2.40	2.60	2.90	3.55	
				64 MHz	1.90	1.90	2.05	2.25	2.60	2.10	2.20	2.35	2.70	3.35	
				48 MHz	1.40	1.40	1.55	1.75	2.15	1.60	1.65	1.85	2.15	2.80	
				32 MHz	0.970	1.00	1.15	1.30	1.70	1.10	1.20	1.40	1.70	2.35	
				24 MHz	0.765	0.800	0.920	1.10	1.50	0.90	0.95	1.15	1.45	2.10	
				16 MHz	0.555	0.590	0.705	0.895	1.25	0.65	0.75	0.90	1.20	1.85	
I_{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	76.0	110	215	395	745	120	185	355	610	1250	µA
				1 MHz	54.0	86.5	195	370	725	88.5	160	335	585	1250	
				400 kHz	39.0	70.5	175	355	710	68.5	140	320	570	1200	
				100 kHz	35.5	75.0	195	345	715	66.0	130	305	560	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 49. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	165	275	950	2600	6550	-	-	-	-	-	nA
			2.4 V	235	370	1150	3100	7650	-	-	-	-	-	
			3 V	325	485	1450	3750	9050	-	-	-	-	-	
			3.6 V	445	655	1900	4800	11500	-	-	-	-	-	
		RTC clocked by LSE quartz (2) in low drive mode	1.8 V	290	410	1050	2550	6700	-	-	-	-	-	
			2.4 V	375	515	1250	3050	7800	-	-	-	-	-	
			3 V	480	645	1550	3700	8800	-	-	-	-	-	
			3.6 V	625	840	1950	4950	11500	-	-	-	-	-	
I_{DD_ALL} (wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz. See (3).	3 V	1.00	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 52: Low-power mode wakeup timings*.

Table 50. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{BAT}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_VBAT} (VBAT)	Backup domain supply current	RTC disabled	1.8 V	3.00	-	-	-	-	-	-	-	-	-	nA
			2.4 V	4.00	-	-	-	-	-	-	-	-	-	
			3 V	5.00	-	-	-	-	-	-	-	-	-	
			3.6 V	11.0	-	-	-	-	-	-	-	-	-	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	145	165	285	550	-	-	-	-	-	-	
			2.4 V	205	235	370	670	-	-	-	-	-	-	
			3 V	285	315	470	820	-	-	-	-	-	-	
			3.6 V	375	430	715	1350	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 20: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 20: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 72. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\lvert I_{IO}\rvert$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\lvert I_{IO}\rvert$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 4 mA $V_{DDIOx} \geq 1.62$ V	-	0.45	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-0.45	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	$0.35_x V_{DDIOx}$	
V_{OH}(3)	Output high level voltage for an I/O pin		$0.65_x V_{DDIOx}$	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\lvert I_{IO}\rvert$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\lvert I_{IO}\rvert$ = 10 mA $V_{DDIOx} \geq 1.62$ V	-	0.4	
		$\lvert I_{IO}\rvert$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 20: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

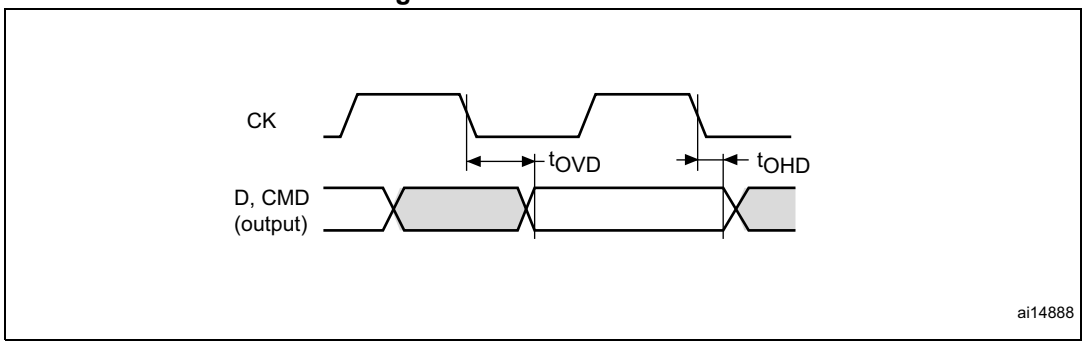
Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 27* and *Table 73*, respectively.

Table 87. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(3)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(3)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(3)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

Figure 40. SD default mode



USB characteristics

The STM32L452xx USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 101. USB electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating voltage		3.0(2)	-	3.6	V
$T_{crystal\_less}$	USB crystal less operation temperature		-15	-	85	°C
R_{PUI}	Embedded USB_DP pull-up value during idle		900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception		1400	2300	3200	
Z_{DRV}(3)	Output driver impedance(4)	Driving high and low	28	36	44	Ω

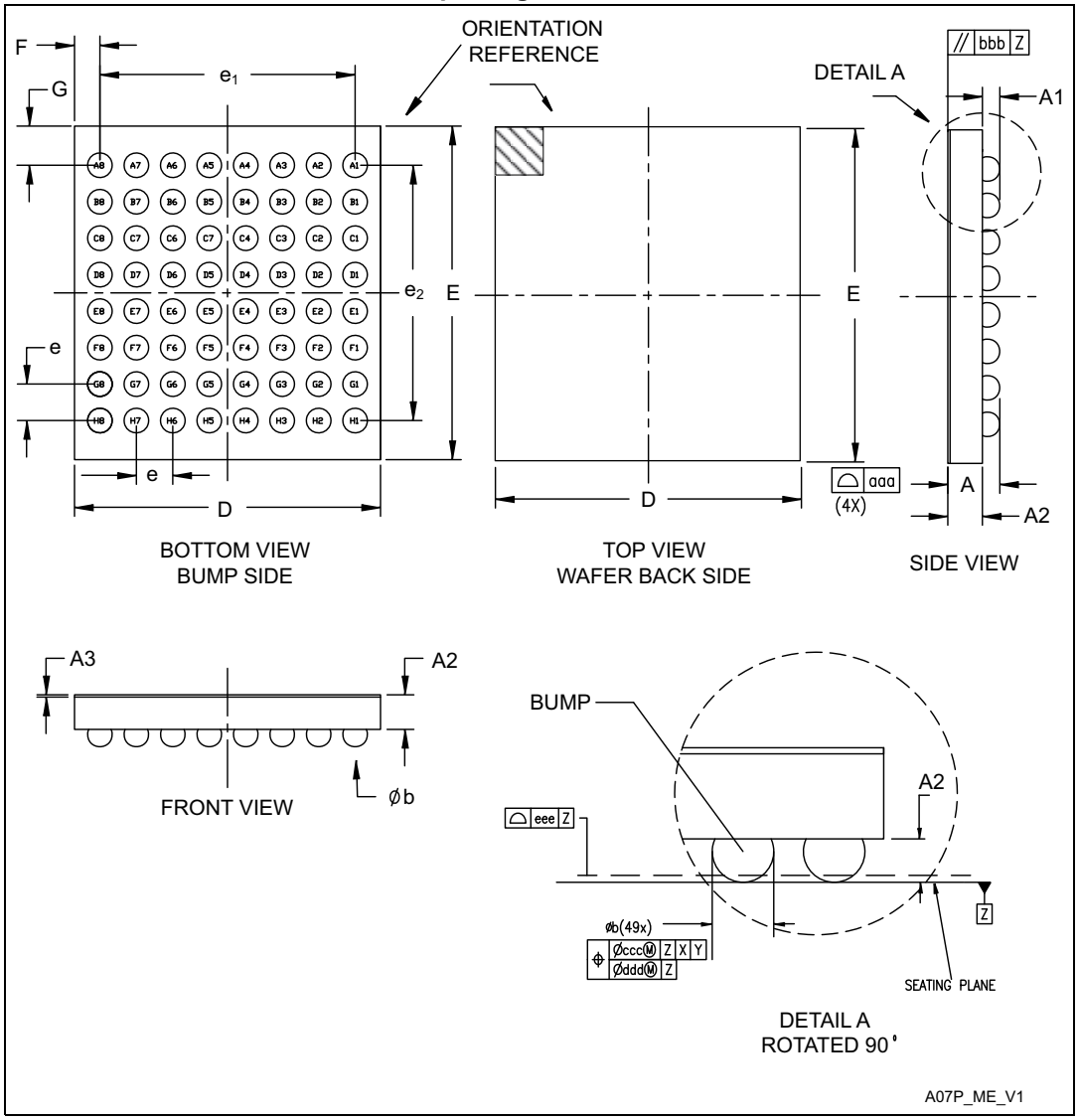
1. T_A = -40 to 125 °C unless otherwise specified.
2. The STM32L452xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V voltage range.
3. Guaranteed by design.
4. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

7.5 WLCSP64 package information

Figure 53. WLCSP64 - 64-ball, 3.357x3.657 mm 0.4 mm pitch wafer level chip scale package outline



1. Dimensions are expressed in millimeters.