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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l452ret6

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3.25 Inter-integrated circuit interface (I^2C)

The device embeds four I2C. Refer to *Table 12: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 4: Clock tree*.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 12. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop 1 mode on address match	X	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X	-

1. X: supported

3.27 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

Table 16. STM32L452xx pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	LQFP64 SMPS	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	D6	10	10	F2	17	J3	PC2	I/O	FT_a	-	LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, EVENTOUT	ADC1_IN3
-	E7	11	11	G1	18	K2	PC3	I/O	FT_a	-	LPTIM1_ETR, SPI2_MOSI, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC1_IN4
-	-	-	-	-	19	J1	VSSA	S	-	-	-	-
-	-	-	-	-	20	K1	VREF-	S	-	-	-	-
8	G8	12	12	F1	-	-	VSSA/ VREF-	S	-	-	-	-
-	-	-	-	-	21	L1	VREF+	S	-	-	-	VREFBUF_OUT
-	-	-	-	-	22	M1	VDDA	S	-	-	-	-
9	F7	13	13	H1	-	-	VDDA/ VREF+	S	-	-	-	-
10	H8	14	14	G2	23	L2	PA0	I/O	FT_a	-	TIM2_CH1, USART2_CTS, UART4_TX, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, COMP1_INM, ADC1_IN5, RTC_TAMP2/WKUP1
11	E6	15	15	H2	24	M2	PA1	I/O	FT_a	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, UART4_RX, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, COMP1_INP, ADC1_IN6
12	G7	16	16	F3	25	K3	PA2	I/O	FT_a	-	TIM2_CH3, USART2_TX, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, TIM15_CH1, EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4/LSCO
13	F6	17	17	G3	26	L3	PA3	I/O	TT_a	-	TIM2_CH4, USART2_RX, LPUART1_RX, QUADSPI_CLK, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, COMP2_INP, ADC1_IN8
-	-	18	18	C2	27	E3	VSS	S	-	-	-	-
-	H7	19	19	D2	28	H3	VDD	S	-	-	-	-

Table 16. STM32L452xx pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	LQFP64 SMPS	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	F3	39	39	E8	65	E10	PC8	I/O	FT	-	TIM3_CH3, TSC_G4_IO3, SDMMC1_D0, EVENTOUT	-
-	E2	40	40	D8	66	D12	PC9	I/O	FT	-	TIM3_CH4, TSC_G4_IO4, USB_NOE, SDMMC1_D1, EVENTOUT	-
29	E3	41	41	D7	67	D11	PA8	I/O	FT	-	MCO, TIM1_CH1, DFSDM1_CKIN1, USART1_CK, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
30	D1	42	42	C7	68	D10	PA9	I/O	FT_f	-	TIM1_CH2, I2C1_SCL, DFSDM1_DATIN1, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
31	C1	43	43	C6	69	C12	PA10	I/O	FT_f	-	TIM1_CH3, I2C1_SDA, USART1_RX, USB_CRS_SYNC, SAI1_SD_A, EVENTOUT	-
32	D2	44	44	C8	70	B12	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, COMP1_OUT, USART1_CTS, CAN1_RX, USB_DM, TIM1_BKIN2_COMP1, EVENTOUT	-
33	D3	45	45	B8	71	A12	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, USB_DP, EVENTOUT	-
34	C2	46	46	A8	72	A11	PA13 (JTMS/ SWDIO)	I/O	FT	(3)	JTMS/SWDAT, IR_OUT, USB_NOE, SAI1_SD_B, EVENTOUT	-
35	B1	47	47	D5	-	-	VSS	S	-	-	-	-
36	A1	48	48	E5	73	C11	VDDUSB	S	-	-	-	-
-	-	-	-	-	74	F11	VSS	S	-	-	-	-

Table 16. STM32L452xx pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	LQFP64 SMPS	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	84	B8	PD3	I/O	FT	-	SPI2_MISO, DFSDM1_DATIN0, USART2_CTS, QUADSPI_BK2_NCS, EVENTOUT	-
-	-	-	-	-	85	B7	PD4	I/O	FT	-	SPI2_MOSI, DFSDM1_CKIN0, USART2_RTS_DE, QUADSPI_BK2_IO0, EVENTOUT	-
-	-	-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX, QUADSPI_BK2_IO1, EVENTOUT	-
-	-	-	-	-	87	B6	PD6	I/O	FT	-	DFSDM1_DATIN1, USART2_RX, QUADSPI_BK2_IO2, SAI1_SD_A, EVENTOUT	-
-	-	-	-	-	88	A5	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, QUADSPI_BK2_IO3, EVENTOUT	-
39	B4	55	54	A5	89	A8	PB3 (JTDO/ TRACE SWO)	I/O	FT_a	(3)	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, SAI1_SCK_B, EVENTOUT	COMP2_INM
40	A4	56	55	A4	90	A7	PB4 (NJTRST)	I/O	FT_fa	(3)	NJTRST, TIM3_CH1, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS, TSC_G2_IO1, SAI1_MCLK_B, EVENTOUT	COMP2_INP
41	C5	57	56	C4	91	C5	PB5	I/O	FT	-	LPTIM1_IN1, TIM3_CH2, CAN1_RX, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, TSC_G2_IO2, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	-

6.3 Operating conditions

6.3.1 General operating conditions

Table 23. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	80	
f_{PCLK2}	Internal APB2 clock frequency	-	0	80	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
V_{DD12}	Standard operating voltage	Full frequency range	1.08	1.32	V
		Up to 26 MHz	1.05		
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	V
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	V
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	V
		USB not used	0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O	-0.3	V_{DDIOx}+0.3	V
		All I/O except TT_xx	-0.3	Min(Min(V_{DD}, V_{DDA}, V_{DDUSB})+3.6 V, 5.5 V)(2)(3)	
P_D	Power dissipation at T_A = 85 °C for suffix 6	LQFP100	-	357	mW
		UFBGA100	-	267	
		LQFP64	-	345	
		UFBGA64	-	308	
		WLCSP64	-	377	
		UFQFPN48	-	690	
P_D	Power dissipation at T_A = 125 °C for suffix 3(4)	LQFP100	-	89	mW
		UFBGA100	-	67	
		LQFP64	-	86	
		UFBGA64	-	77	
		WLCSP64	-	94	
		UFQFPN48	-	172	

Table 25. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1) (2)	PVM1 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4) (2)	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.35	2.40	2.50	2.65	3.00	2.65	2.75	2.90	3.20	3.75	mA
				16 MHz	1.50	1.55	1.65	1.80	2.15	1.70	1.75	1.95	2.20	2.80	
				8 MHz	0.815	0.845	0.940	1.10	1.45	0.95	1.00	1.15	1.45	2.00	
				4 MHz	0.465	0.495	0.595	0.760	1.10	0.55	0.60	0.75	1.05	1.60	
				2 MHz	0.295	0.320	0.420	0.580	0.910	0.35	0.40	0.55	0.85	1.40	
				1 MHz	0.205	0.235	0.330	0.495	0.825	0.25	0.30	0.45	0.75	1.30	
				100 kHz	0.130	0.155	0.250	0.415	0.745	0.15	0.25	0.40	0.65	1.25	
			Range 1	80 MHz	8.45	8.50	8.65	8.90	9.25	9.45	9.50	9.75	10.10	10.75	
				72 MHz	7.65	7.70	7.85	8.05	8.45	8.50	8.60	8.80	9.15	9.85	
				64 MHz	6.80	6.85	7.00	7.20	7.60	7.60	7.70	7.90	8.25	8.90	
				48 MHz	5.10	5.15	5.25	5.45	5.85	5.70	5.80	6.00	6.35	7.00	
				32 MHz	3.45	3.50	3.60	3.80	4.20	3.85	3.95	4.15	4.50	5.15	
				24 MHz	2.60	2.65	2.80	2.95	3.35	2.95	3.05	3.20	3.55	4.20	
				16 MHz	1.80	1.85	1.95	2.15	2.50	2.00	2.10	2.30	2.60	3.25	
I_{DD_ALL} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	225	260	365	550	900	275	335	470	770	1400	µA
				1 MHz	130	160	270	450	800	170	225	375	670	1300	
				400 kHz	73.0	99.5	205	385	735	105	165	325	600	1250	
				100 kHz	38.0	71.0	175	355	705	70	140	315	565	1200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 32. Current consumption in Run, code with data processing running from SRAM1 and power supplied by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions(1)		TYP					Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	80 MHz	3.10	3.12	3.14	3.18	3.24	mA
			72 MHz	2.80	2.81	2.84	2.87	2.94	
			64 MHz	2.50	2.51	2.53	2.57	2.63	
			48 MHz	1.87	1.88	1.90	1.93	2.00	
			32 MHz	1.26	1.27	1.29	1.32	1.38	
			24 MHz	0.96	0.96	0.98	1.02	1.07	
			16 MHz	0.65	0.66	0.68	0.71	0.77	
			8 MHz	0.35	0.36	0.38	0.41	0.47	
			4 MHz	0.20	0.21	0.22	0.25	0.31	
			2 MHz	0.13	0.13	0.15	0.18	0.24	
			1 MHz	0.09	0.09	0.11	0.14	0.20	
			100 kHz	0.05	0.06	0.07	0.10	0.16	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V

Table 42. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.700	0.730	0.830	1.00	1.35	0.80	0.90	1.05	1.30	1.90	mA
				16 MHz	0.475	0.505	0.605	0.775	1.10	0.55	0.65	0.80	1.05	1.65	
				8 MHz	0.300	0.325	0.425	0.590	0.920	0.35	0.45	0.60	0.85	1.45	
				4 MHz	0.210	0.235	0.335	0.500	0.830	0.25	0.30	0.45	0.75	1.35	
				2 MHz	0.165	0.190	0.290	0.455	0.785	0.20	0.25	0.40	0.70	1.25	
				1 MHz	0.145	0.170	0.265	0.430	0.760	0.15	0.25	0.40	0.65	1.25	
				100 kHz	0.125	0.150	0.245	0.410	0.740	0.15	0.20	0.35	0.65	1.20	
			Range 1	80 MHz	2.30	2.35	2.45	2.65	3.05	2.55	2.65	2.85	3.15	3.80	
				72 MHz	2.10	2.15	2.25	2.45	2.80	2.35	2.40	2.60	2.90	3.55	
				64 MHz	1.90	1.90	2.05	2.25	2.60	2.10	2.20	2.35	2.70	3.35	
				48 MHz	1.40	1.40	1.55	1.75	2.15	1.60	1.65	1.85	2.15	2.80	
				32 MHz	0.970	1.00	1.15	1.30	1.70	1.10	1.20	1.40	1.70	2.35	
				24 MHz	0.765	0.800	0.920	1.10	1.50	0.90	0.95	1.15	1.45	2.10	
				16 MHz	0.555	0.590	0.705	0.895	1.25	0.65	0.75	0.90	1.20	1.85	
I_{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	76.0	110	215	395	745	120	185	355	610	1250	µA
				1 MHz	54.0	86.5	195	370	725	88.5	160	335	585	1250	
				400 kHz	39.0	70.5	175	355	710	68.5	140	320	570	1200	
				100 kHz	35.5	75.0	195	345	715	66.0	130	305	560	1200	

1. Guaranteed by characterization results, unless otherwise specified.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 71: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 51: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 57*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 57. HSE oscillator characteristics(1)

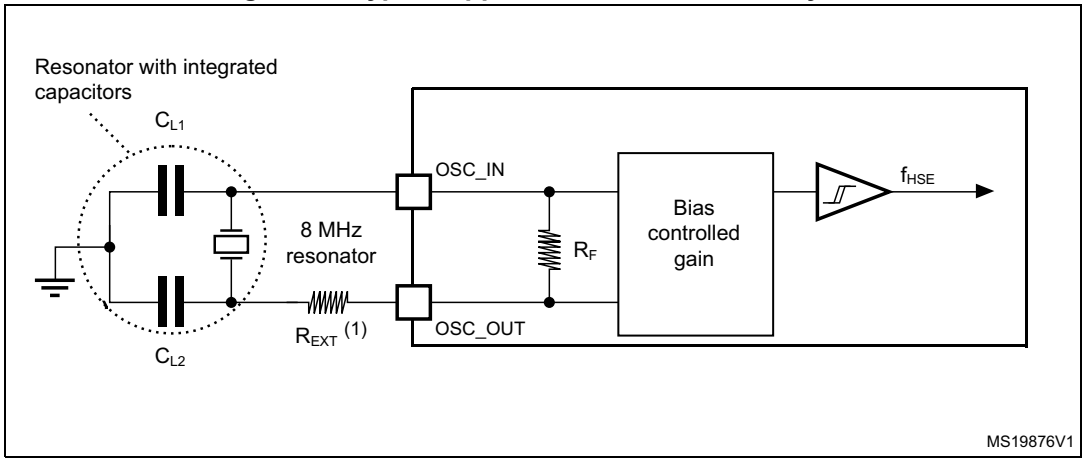
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 21. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 58*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 58. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

6.3.8 Internal clock source characteristics

The parameters given in *Table 59* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 59. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)(2)	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	µs
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.10 Flash memory characteristics

Table 64. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.69	90.76	µs
t_{prog_row}	one row (32 double word) programming time	normal programming	2.61	2.90	ms
		fast programming	1.91	2.12	
t_{prog_page}	one page (2 Kbyte) programming time	normal programming	20.91	23.24	
		fast programming	15.29	16.98	
t_{ERASE}	Page (2 KB) erase time	-	22.02	24.47	
t_{prog_bank}	one bank (512 Kbyte) programming time	normal programming	5.35	5.95	s
		fast programming	3.91	4.35	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.59	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 2 µs)	-	
		Erase mode	7 (for 41 µs)	-	

1. Guaranteed by design.

Table 65. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 67. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8 MHz/ 80 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	-8	dBµV
			30 MHz to 130 MHz	2	
			130 MHz to 1 GHz	5	
			1 GHz to 2 GHz	8	
			EMI Level	2.5	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 68. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Guaranteed by characterization results.

Table 73. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	28	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(4)		-	5	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0394 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of all I_{DDXXX} and V_{DDXXX}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 111. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 × 14 mm / 0.5 mm pitch	56	°C/W
	Thermal resistance junction-ambient UFBGA100 - 7 × 7 mm / 0.5 mm pitch	75	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	58	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient WLCSP64 3.141 x 3.127 / 0.35 mm pitch	53	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm / 0.5 mm pitch	29	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L452xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

In this case, parts must be ordered at least with the temperature range suffix 3 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 59* to select the required temperature range (suffix 6 or 3) according to your ambient temperature or power requirements.

Figure 59. LQFP64 P_D max vs. T_A