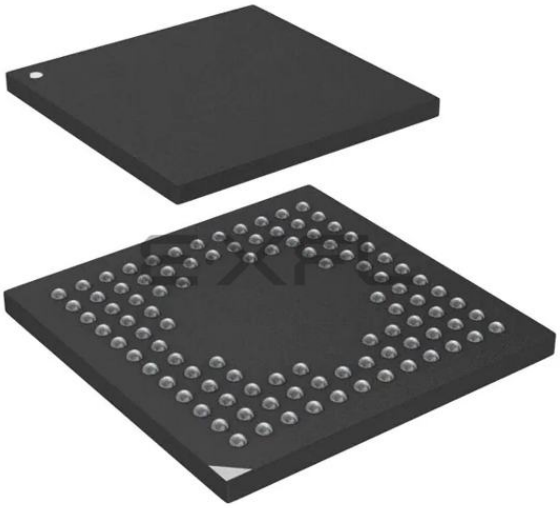

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l452vci6

2 Description

The STM32L452xx devices are the ultra-low-power microcontrollers based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L452xx devices embed high-speed memories (Flash memory up to 512 Kbyte, 160 Kbyte of SRAM), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L452xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer a fast 12-bit ADC (5 Msps), two comparators, one operational amplifier, one DAC channel, an internal voltage reference buffer, a low-power RTC, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, four general-purpose 16-bit timers, and two 16-bit low-power timers.

In addition, up to 21 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces.

- Four I2Cs
- Three SPIs
- Three USARTs, one UART and one Low-Power UART.
- One SAI (Serial Audio Interfaces)
- One SDMMC
- One CAN
- One USB full-speed device crystal less

The STM32L452xx operates in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V V_{DD} power supply when using internal LDO regulator and a 1.05 to 1.32V V_{DD12} power supply when using external SMPS supply. A comprehensive set of power-saving modes allows the design of low-power applications.

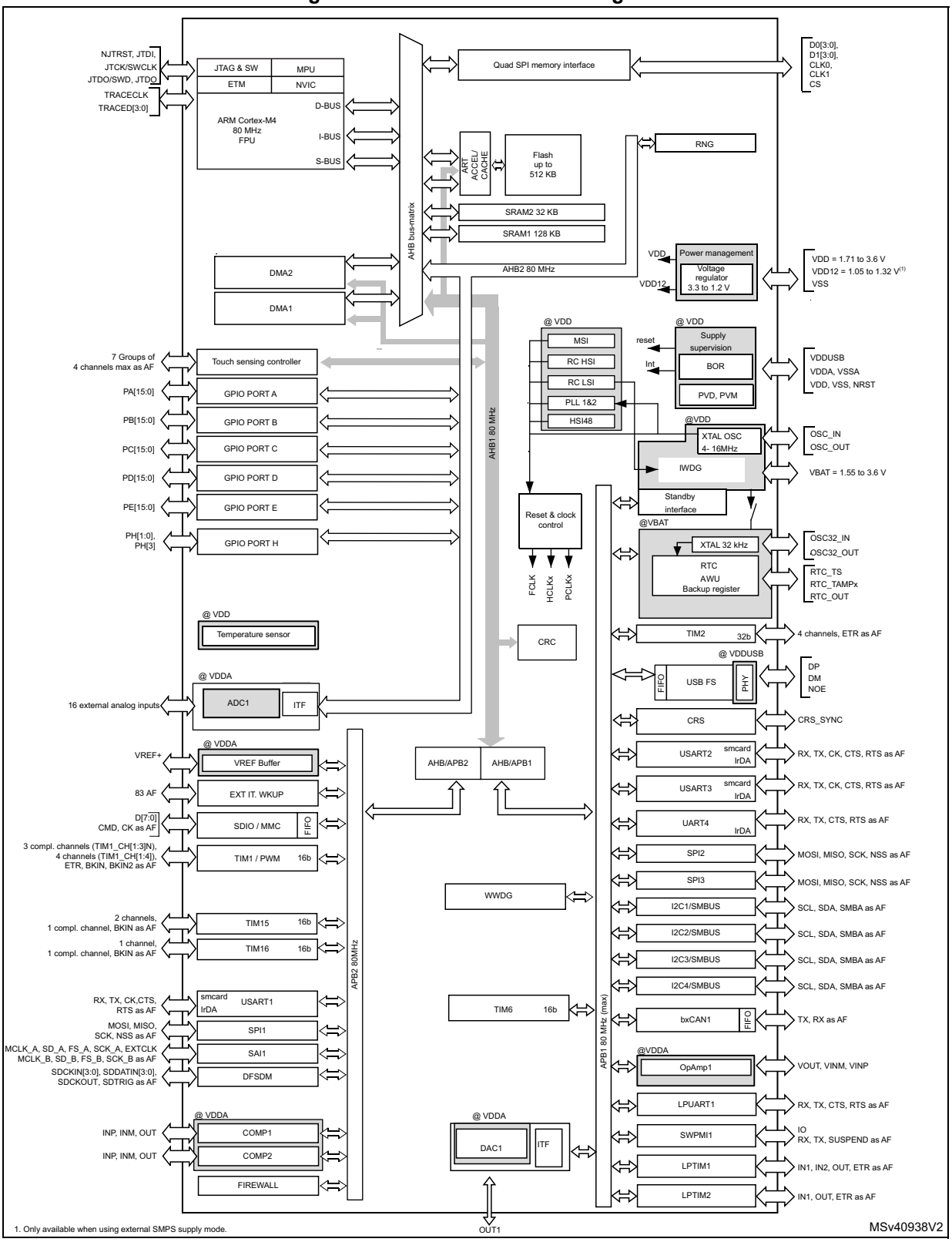
Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMP and comparators. A VBAT input allows to backup the RTC and backup registers. Dedicated V_{DD12} power supplies can be used to bypass the internal LDO regulator when connected to an external SMPS.

The STM32L452xx family offers six packages from 48 to 100-pin packages.

Table 2. STM32L452xx family device features and peripheral counts

Peripheral		STM32L452Vx		STM32L452Rx		STM32L452Cx	
Flash memory		256KB	512KB	256KB	512KB	256KB	512KB
SRAM		160KB					
Quad SPI		Yes					
Timers	Advanced control	1 (16-bit)					
	General purpose	2 (16-bit) 1 (32-bit)					
	Basic	2 (16-bit)					
	Low -power	2 (16-bit)					
	SysTick timer	1					
	Watchdog timers (independent, window)	2					
Comm. interfaces	SPI	3					
	I^2C	4					
	USART UART LPUART	3 1 1					
	SAI	1					
	CAN	1					
	USB FS	Yes					
	SDMMC	Yes(1)				No	
RTC		Yes					
Tamper pins		3		2		2	
Random generator		Yes					
GPIOs(2) Wakeup pins		83 5		52 4(1)		38 3	
Capacitive sensing Number of channels		21		12		6	
12-bit ADC Number of channels		1 16		1 16(1)		1 10	
12-bit DAC channels		1					
Internal voltage reference buffer		Yes		No			
Analog comparator		2					
Operational amplifiers		1					
Max. CPU frequency		80 MHz					

Figure 1. STM32L452xx block diagram

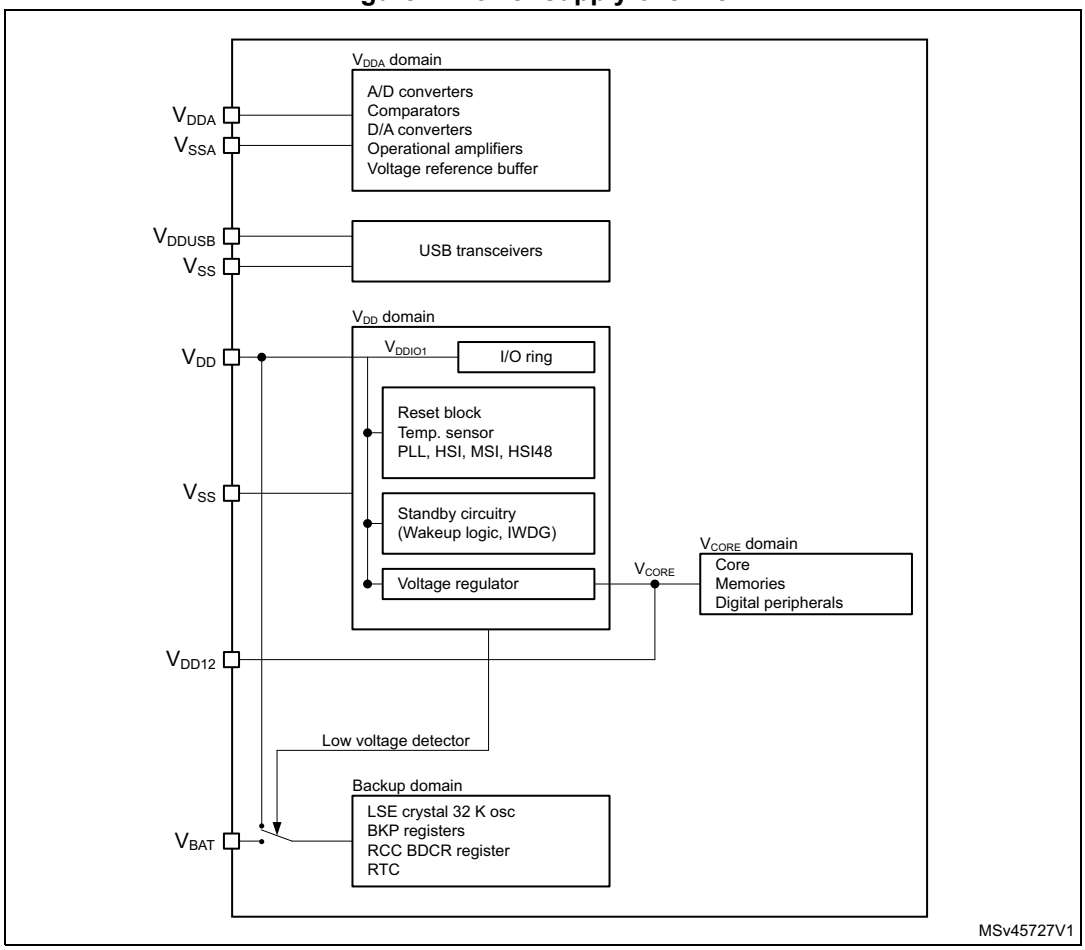


Note: AF: alternate function on I/O pins.

Note: If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant.

Note: V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1}, with $V_{DDIO1} = V_{DD}$.

Figure 2. Power supply overview



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power- down transient phase.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application. Low frequency clocks (LSI, LSE) are available down to Stop 1 low power state.
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes down to Standby mode. LSE can also be output on LSCO in Shutdown mode. LSCO is not available in VBAT mode.

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 80 MHz.

3.14 Interrupts and events

3.14.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 67 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

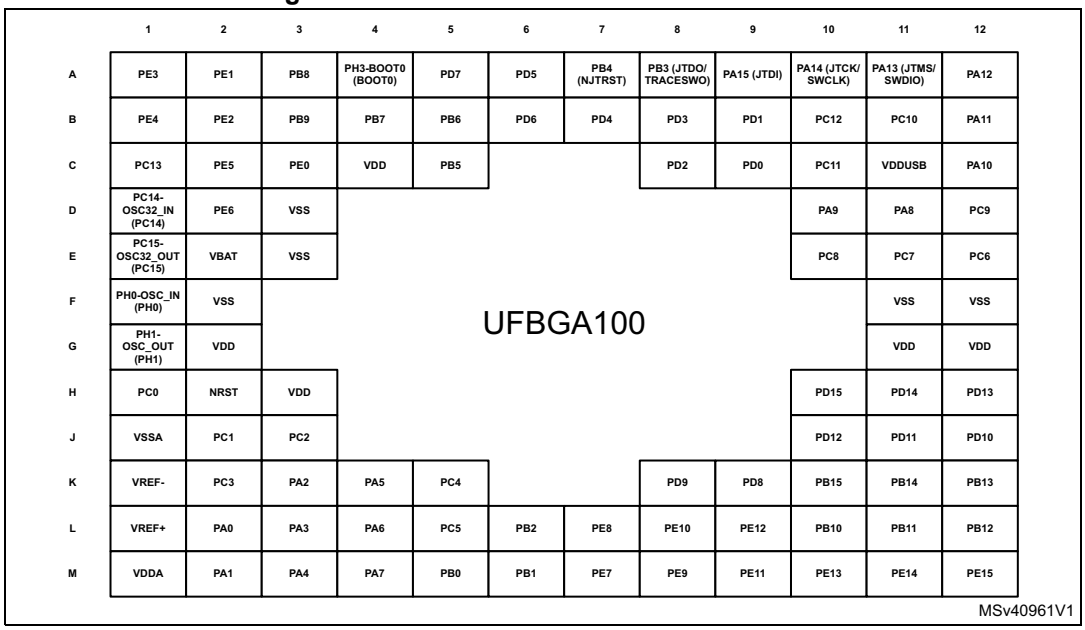
- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.14.2 Extended interrupt/event controller (EXTI)

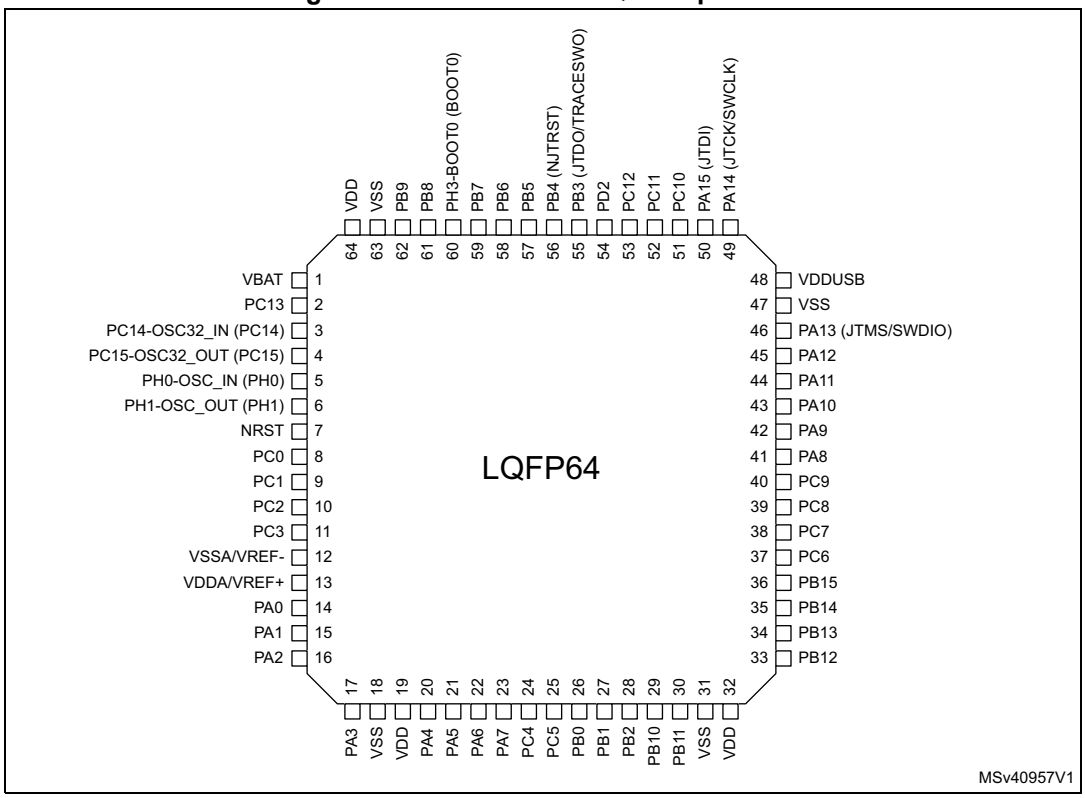
The extended interrupt/event controller consists of 37 edge detector lines used to generate interrupt/event requests and wake-up the system from Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines.

Figure 7. STM32L452Vx UFBGA100 ballout(1)



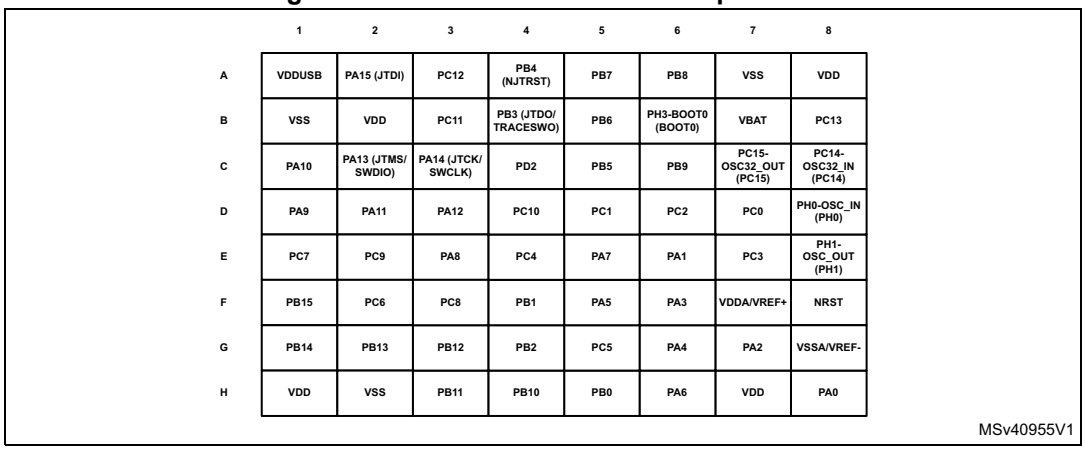
1. The above figure shows the package top view.

Figure 8. STM32L452Rx LQFP64 pinout(1)



1. The above figure shows the package top view.

Figure 11. STM32L452Rx WLCSP64 pinout(1)

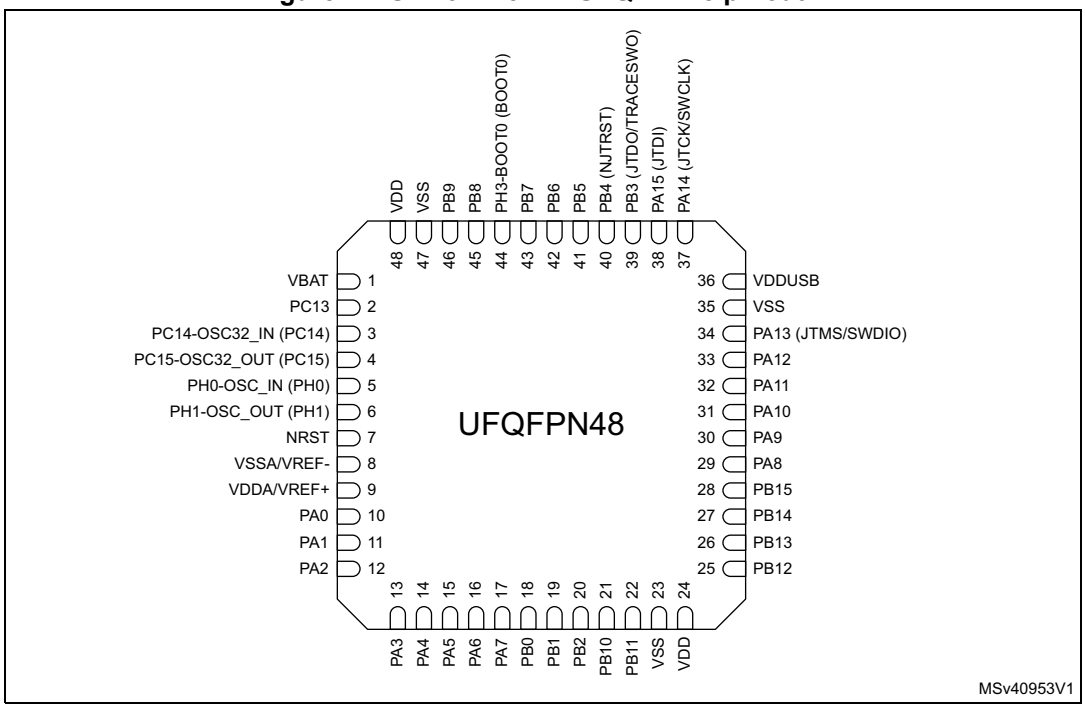


	1	2	3	4	5	6	7	8
A	VDDUSB	PA15 (JTDI)	PC12	PB4 (NJTRST)	PB7	PB8	VSS	VDD
B	VSS	VDD	PC11	PB3 (JTDO/ TRACESWO)	PB6	PH3-BOOT0 (BOOT0)	VBAT	PC13
C	PA10	PA13 (JTMS/ SWDIO)	PA14 (JTCK/ SWCLK)	PD2	PB5	PB9	PC15-OSC32_OUT (PC15)	PC14-OSC32_IN (PC14)
D	PA9	PA11	PA12	PC10	PC1	PC2	PC0	PH0-OSC_IN (PH0)
E	PC7	PC9	PA8	PC4	PA7	PA1	PC3	PH1-OSC_OUT (PH1)
F	PB15	PC6	PC8	PB1	PA5	PA3	VDDA/VREF+	NRST
G	PB14	PB13	PB12	PB2	PC5	PA4	PA2	VSSA/VREF-
H	VDD	VSS	PB11	PB10	PB0	PA6	VDD	PA0

MSv40955V1

1. The above figure shows the package top view.

Figure 12. STM32L452Cx UFQFPN48 pinout(1)



MSv40953V1

1. The above figure shows the package top view.

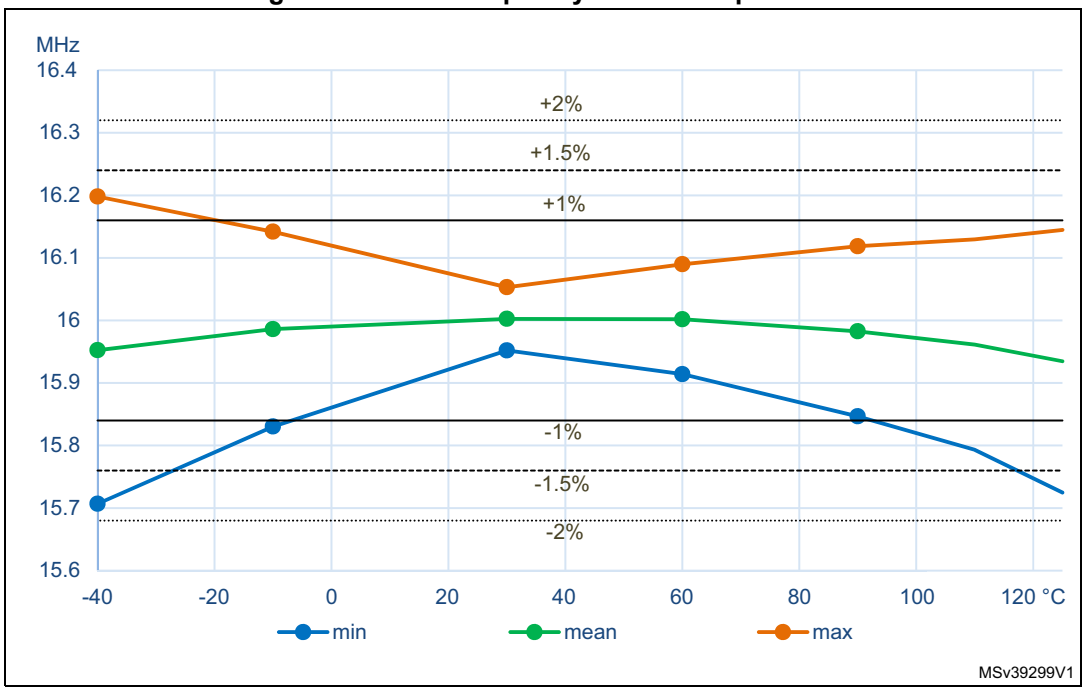
Table 16. STM32L452xx pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN48	WLCSP64	LQFP64	LQFP64 SMPS	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
28	F1	36	36	F7	54	K10	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, SPI2_MOSI, DFSDM1_CKIN2, TSC_G1_IO4, SAI1_SD_A, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	55	K9	PD8	I/O	FT	-	USART3_TX, EVENTOUT	-
-	-	-	-	-	56	K8	PD9	I/O	FT	-	USART3_RX, EVENTOUT	-
-	-	-	-	-	57	J12	PD10	I/O	FT	-	USART3_CK, TSC_G6_IO1, EVENTOUT	-
-	-	-	-	-	58	J11	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS, TSC_G6_IO2, LPTIM2_ETR, EVENTOUT	-
-	-	-	-	-	59	J10	PD12	I/O	FT	-	I2C4_SCL, USART3_RTS_DE, TSC_G6_IO3, LPTIM2_IN1, EVENTOUT	-
-	-	-	-	-	60	H12	PD13	I/O	FT	-	I2C4_SDA, TSC_G6_IO4, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	-	61	H11	PD14	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	62	H10	PD15	I/O	FT	-	EVENTOUT	-
-	F2	37	37	F6	63	E12	PC6	I/O	FT	-	TIM3_CH1, DFSDM1_CKIN3, TSC_G4_IO1, SDMMC1_D6, EVENTOUT	-
-	E1	38	38	E7	64	E11	PC7	I/O	FT	-	TIM3_CH2, DFSDM1_DATIN3, TSC_G4_IO2, SDMMC1_D7, EVENTOUT	-

Table 17. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2 LPTIM1	I2C4/TIM1/ TIM2/TIM3	I2C4/USART2/ CAN1/TIM1	I2C1/I2C2/ I2C3/I2C4	SPI1/SPI2/I2C4	SPI3/DFSDM/ COMP1	USART1/ USART2/ USART3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	-	-	SPI1_NSS	DFSDM1_ CKIN0	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	-	-	-	DFSDM1_ DATIN0	USART3_RTS_ DE
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM1_ CKIN0	-
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_ DE
	PB4	NJTRST	-	TIM3_CH1	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS
	PB5	-	LPTIM1_IN1	TIM3_CH2	CAN1_RX	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	-	-	I2C1_SCL	I2C4_SCL	-	USART1_TX
	PB7	-	LPTIM1_IN2	-	-	I2C1_SDA	I2C4_SDA	-	USART1_RX
	PB8	-	-	-	-	I2C1_SCL	-	-	-
	PB9	-	IR_OUT	-	-	I2C1_SDA	SPI2_NSS	-	-
	PB10	-	TIM2_CH3	-	I2C4_SCL	I2C2_SCL	SPI2_SCK	-	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	-	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN_C OMP2	I2C2_SMBA	SPI2_NSS	DFSDM1_ DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM1_ CKIN1	USART3_CTS
	PB14	-	TIM1_CH2N	-	-	I2C2_SDA	SPI2_MISO	DFSDM1_ DATIN2	USART3_RTS_ DE
	PB15	RTC_REFIN	TIM1_CH3N	-	-	-	SPI2_MOSI	DFSDM1_ CKIN2	-

Figure 23. HSI16 frequency versus temperature



Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 67. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8 MHz/ 80 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	-8	dBµV
			30 MHz to 130 MHz	2	
			130 MHz to 1 GHz	5	
			1 GHz to 2 GHz	8	
			EMI Level	2.5	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 68. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 69. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 70*.

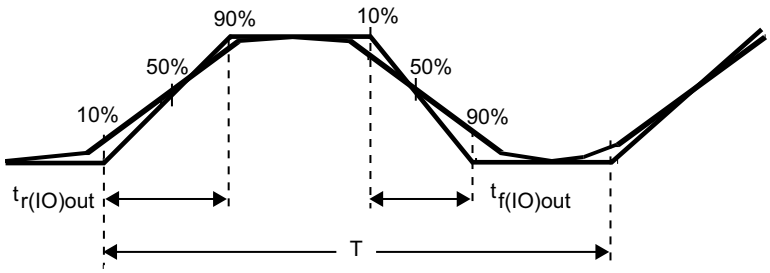
Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 70. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PA4, PA5, PE8, PE9, PE10, PE11, PE12	-5	N/A(2)	mA
	Injected current on PE8, PE9, PE10, PE11, PE12	-0	N/A(2)	
	Injected current on PA4, PA5 pins	-5	0	

1. Guaranteed by characterization results.
2. Injection is not possible.

Figure 27. I/O AC characteristics definition(1)



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 73: I/O AC characteristics*.

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 74. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 \times V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7 \times V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0, PA1.
4. Slow channels are: all ADC inputs except the fast channels.

Table 97. QUADSPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		2 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	48	
		1.71 < V_{DD} < 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		1.71 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK} = 48 MHz, presc=0	$t_{(CK)}$/2-2	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$			$t_{(CK)}$/2	-	$t_{(CK)}$/2+2	
$t_{sr(IN)}$	Data input setup time on rising edge	Voltage Range 1	1	-	-	
		Voltage Range 2	3.5			
$t_{sf(IN)}$	Data input setup time on falling edge	Voltage Range 1	1	-	-	
		Voltage Range 2	1.5			
$t_{hr(IN)}$	Data input hold time on rising edge	Voltage Range 1	6	-	-	
		Voltage Range 2	6.5			
$t_{hf(IN)}$	Data input hold time on falling edge	Voltage Range 1	5.5	-	-	
		Voltage Range 2	5.5			
$t_{vr(OUT)}$	Data output valid time on rising edge	Voltage Range 1	-	5	5.5	
		Voltage Range 2		9.5	14	
$t_{vf(OUT)}$	Data output valid time on falling edge	Voltage Range 1	-	5	8.5	
		Voltage Range 2		15	19	
$t_{hr(OUT)}$	Data output hold time on rising edge	Voltage Range 1	3.5	-	-	
		Voltage Range 2	8	-		
$t_{hf(OUT)}$	Data output hold time on falling edge	Voltage Range 1	3.5	-	-	
		Voltage Range 2	13	-		

1. Guaranteed by characterization results.

Figure 35. Quad SPI timing diagram - SDR mode

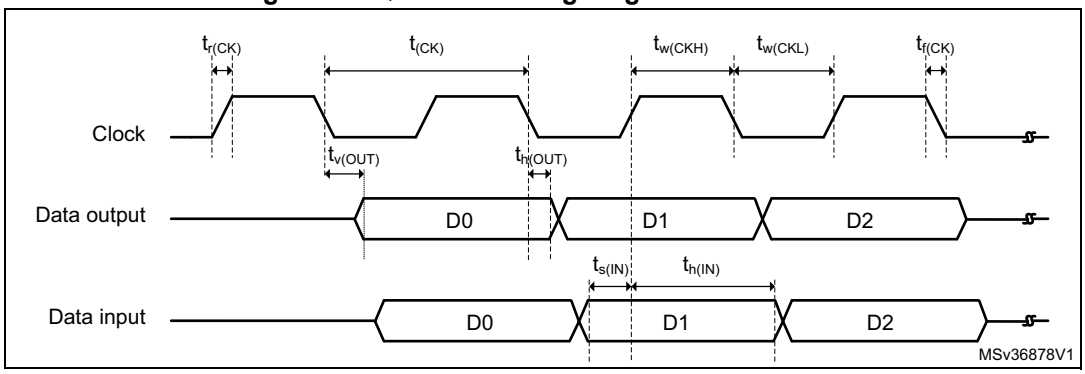
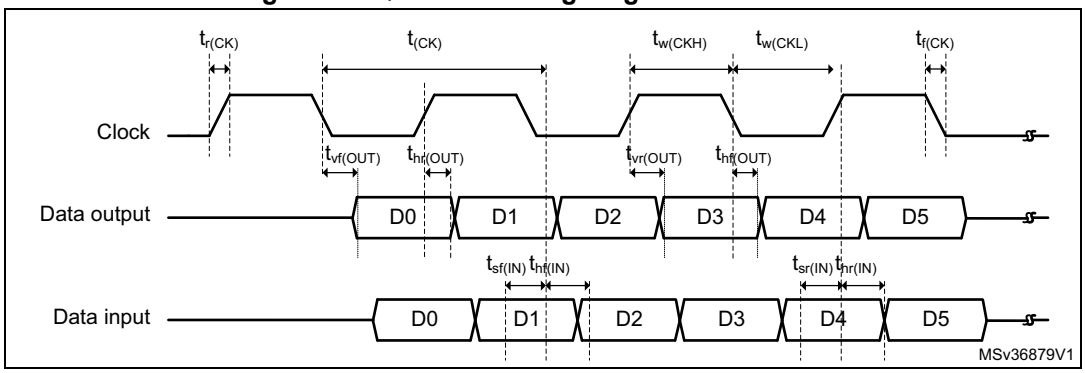


Figure 36. Quad SPI timing diagram - DDR mode



SAI characteristics

Unless otherwise specified, the parameters given in *Table 98* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

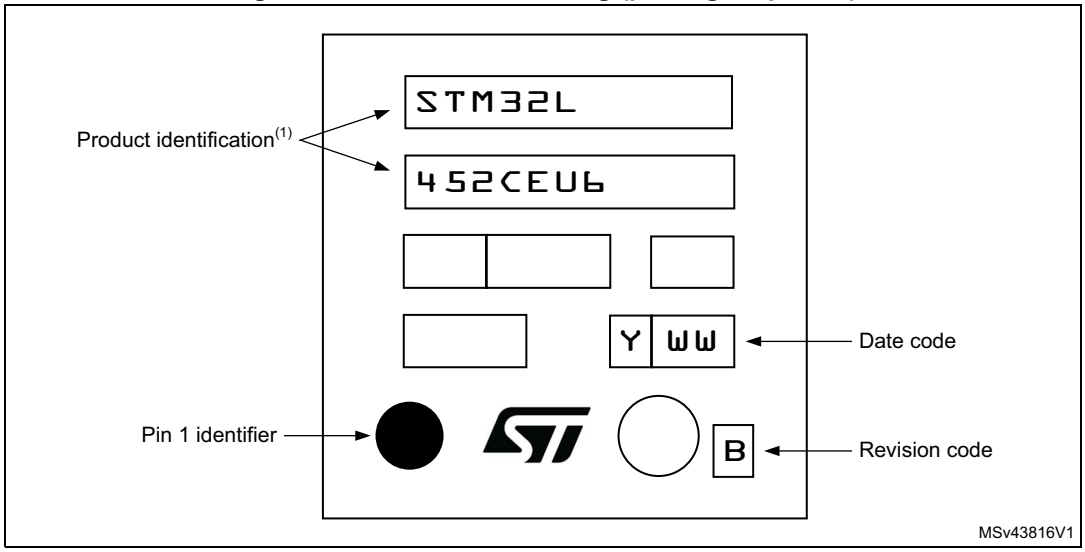
Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 98. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter $2.7 \le V_{DD} \le 3.6$ Voltage Range 1	-	18.5	MHz
		Master transmitter $1.71 \le V_{DD} \le 3.6$ Voltage Range 1	-	12.5	
		Master receiver Voltage Range 1	-	25	
		Slave transmitter $2.7 \le V_{DD} \le 3.6$ Voltage Range 1	-	22.5	
		Slave transmitter $1.71 \le V_{DD} \le 3.6$ Voltage Range 1	-	14.5	
		Slave receiver Voltage Range 1	-	25	
		Voltage Range 2	-	12.5	
$t_{v(FS)}$	FS valid time	Master mode $2.7 \le V_{DD} \le 3.6$	-	22	ns
		Master mode $1.71 \le V_{DD} \le 3.6$	-	40	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	1	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	2	-	ns
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	2	-	ns
$t_{su(SD\_B\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5	-	ns
$t_{h(SD\_B\_SR)}$		Slave receiver	2.5	-	

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 58. UFQFPN48 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.