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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l452vct6

Table 2. STM32L452xx family device features and peripheral counts (continued)

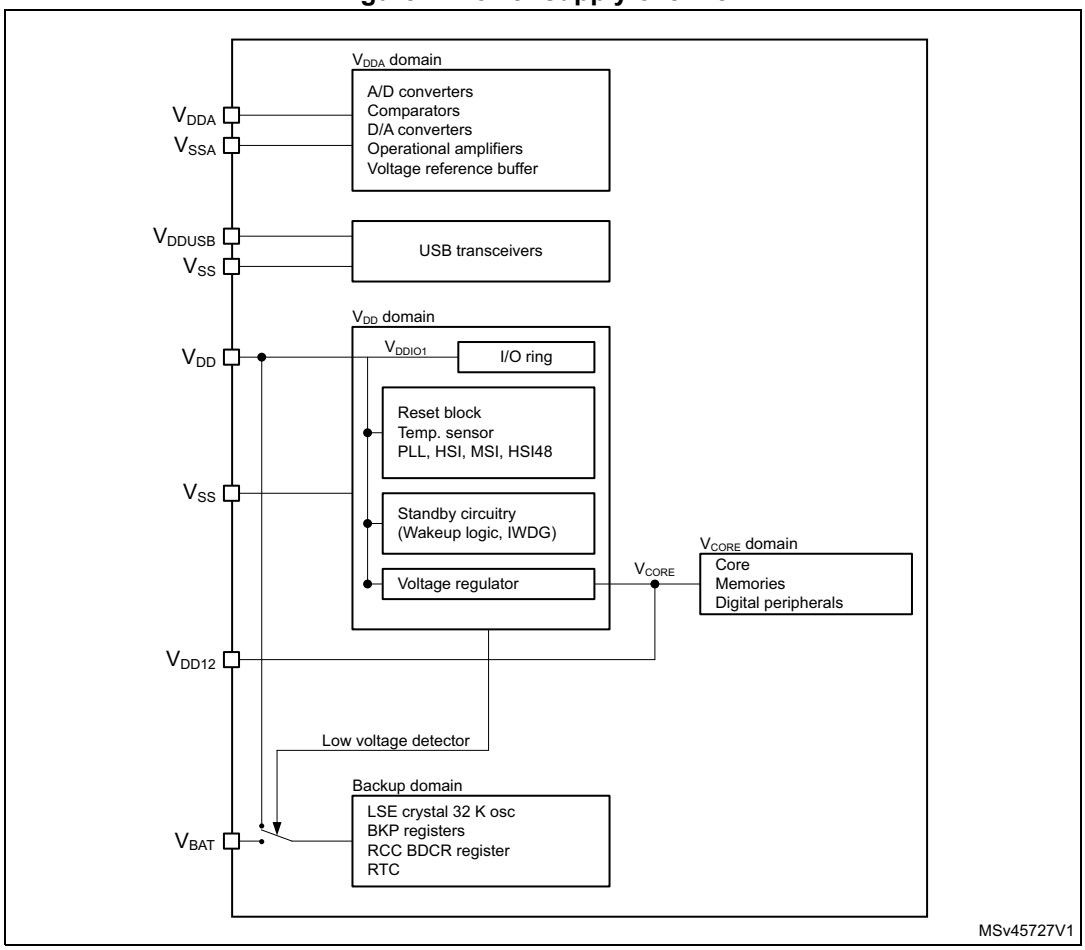
Peripheral	STM32L452Vx	STM32L452Rx	STM32L452Cx
Operating voltage	1.71 to 3.6 V		
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 130 °C		
Packages	LQFP100 UFBGA100	WLCSP64 LQFP64 UFBGA64	UFQFPN48

1. WKUP5, ADC1_IN14 and SDMMC interface are not supported by 64-pin packages with SMPS option.
2. In case external SMPS package type is used, 2 GPIO's are replaced by VDD12 pins to connect the SMPS power supplies hence reducing the number of available GPIO's by 2.

Note: If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant.

Note: V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1}, with $V_{DDIO1} = V_{DD}$.

Figure 2. Power supply overview



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power- down transient phase.

Table 4. STM32L452xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1) USARTx (x=1...3)[9] UART4[9] LPUART1[9] I2Cx (x=1...4)[10] LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...3)[9] UART4[9] LPUART1[9] I2Cx (x=1...4)[10] LPTIMx (x=1,2) USB_FS[11]	9.85 µA w/o RTC 10.5 µA w RTC	5.7 µs in SRAM 7 µs in Flash
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3[10] LPUART1[9] LPTIM1 *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3[10] LPUART1[9] LPTIM1	2.05 µA w/o RTC 2.30 µA w/RTC	5.8 µs in SRAM 8.3 µs in Flash

Table 4. STM32L452xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Standby	LPR	Powered Off	Off	SRAM 2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx)[12] BOR, RTC, IWDG	0.35 µA w/o RTC 0.52 µA w/ RTC	16.1 µs
	OFF			Powered Off				0.10 µA w/o RTC 0.27 µA w/ RTC	
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down[13]	Reset pin 5 I/Os (WKUPx)[12] RTC	0.02 µA w/o RTC 0.17 µA w/ RTC	256 µs

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. Typical current at V_{DD} = 1.8 V, 25°C. Consumptions values provided running from SRAM, Flash memory Off, 80 MHz in Range 1, 26 MHz in Range 2, 2 MHz in LPRun/LPSleep.
4. Theoretical value based on V_{DD} = 3.3 V, DC/DC Efficiency of 85%, V_{CORE} = 1.10 V
5. Theoretical value based on V_{DD} = 3.3 V, DC/DC Efficiency of 85%, V_{CORE} = 1.05 V
6. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
7. The SRAM1 and SRAM2 clocks can be gated on or off independently.
8. SMPS mode can be used in STOP0 Mode, but no significant power gain can be expected.
9. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
10. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
11. USB_FS wakeup by resume from suspend and attach detection protocol event.
12. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
13. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 21 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.21 Digital filter for Sigma-Delta Modulators (DFSDM)

The device embeds one DFSDM with 2 digital filters modules and 4 external input serial channels (transceivers) or alternately 4 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

3.32 Universal serial bus (USB)

The STM32L452xx devices embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.33 Clock recovery system (CRS)

The STM32L452xx devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

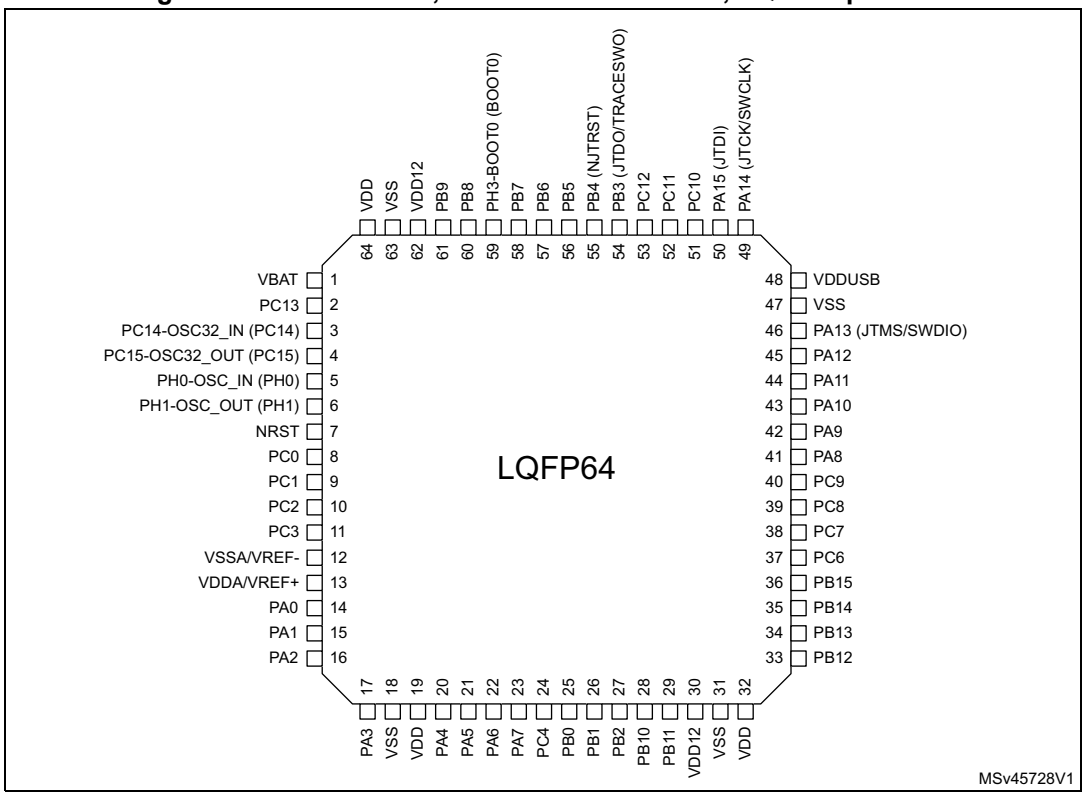
3.34 Quad SPI memory interface (QUADSPI)

The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory

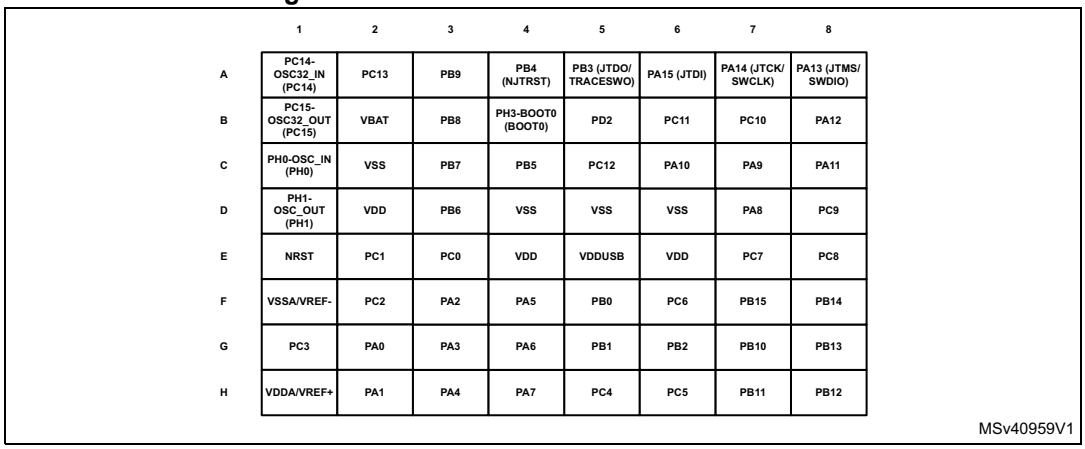
Both throughput and capacity can be increased two-fold using dual-flash mode, where two Quad SPI flash memories are accessed simultaneously.

Figure 9. STM32L452Rx, external SMPS device, LQFP64 pinout(1)



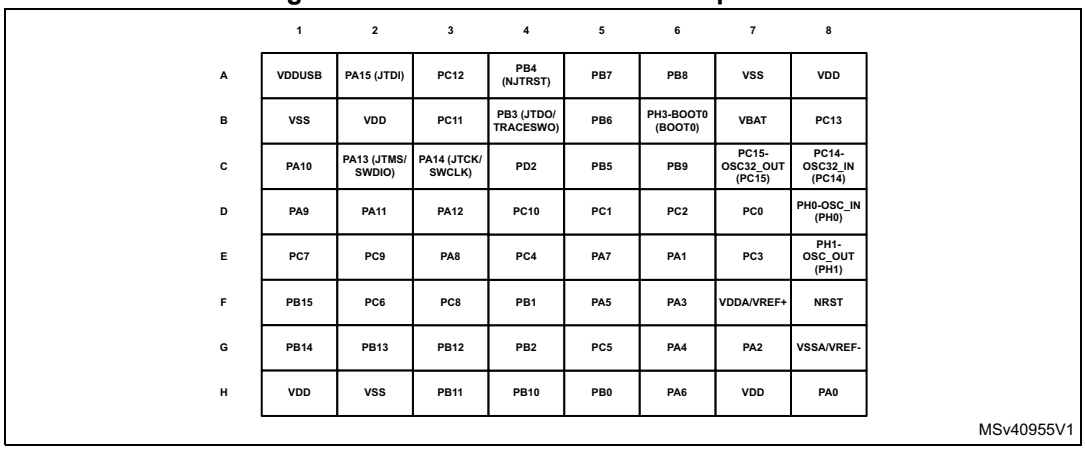
1. The above figure shows the package top view.

Figure 10. STM32L452Rx UFBGA64 ballout(1)



1. The above figure shows the package top view.

Figure 11. STM32L452Rx WLCSP64 pinout(1)

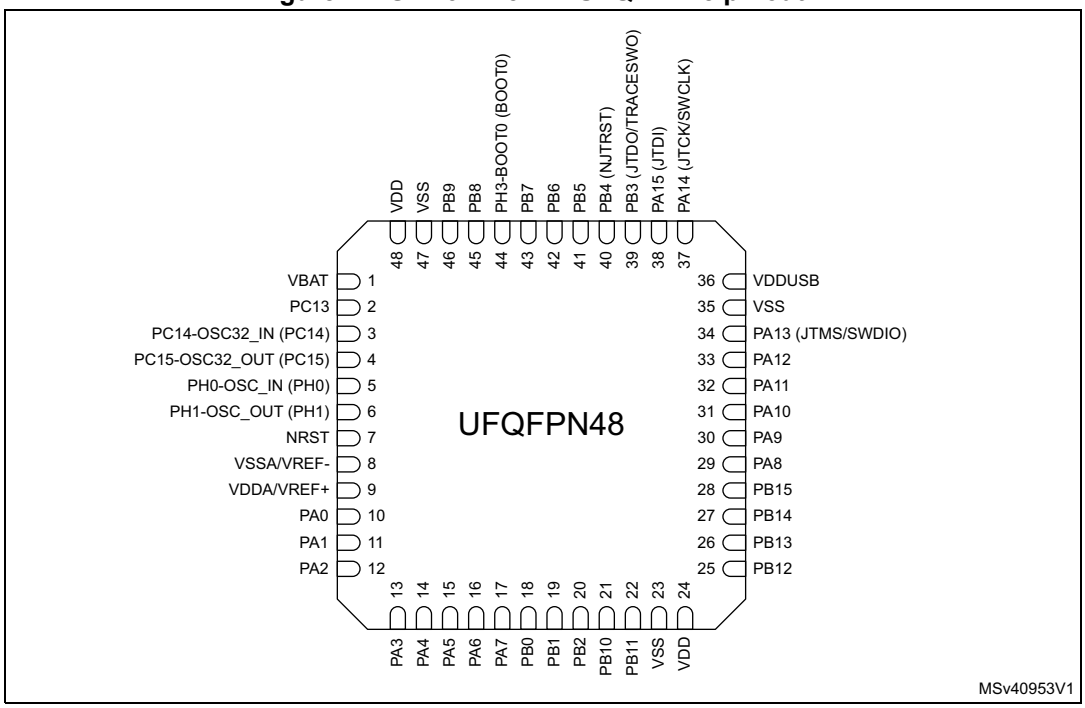


	1	2	3	4	5	6	7	8
A	VDDUSB	PA15 (JTDI)	PC12	PB4 (NJTRST)	PB7	PB8	VSS	VDD
B	VSS	VDD	PC11	PB3 (JTDO/ TRACESWO)	PB6	PH3-BOOT0 (BOOT0)	VBAT	PC13
C	PA10	PA13 (JTMS/ SWDIO)	PA14 (JTCK/ SWCLK)	PD2	PB5	PB9	PC15-OSC32_OUT (PC15)	PC14-OSC32_IN (PC14)
D	PA9	PA11	PA12	PC10	PC1	PC2	PC0	PH0-OSC_IN (PH0)
E	PC7	PC9	PA8	PC4	PA7	PA1	PC3	PH1-OSC_OUT (PH1)
F	PB15	PC6	PC8	PB1	PA5	PA3	VDDA/VREF+	NRST
G	PB14	PB13	PB12	PB2	PC5	PA4	PA2	VSSA/VREF-
H	VDD	VSS	PB11	PB10	PB0	PA6	VDD	PA0

MSv40955V1

1. The above figure shows the package top view.

Figure 12. STM32L452Cx UFQFPN48 pinout(1)

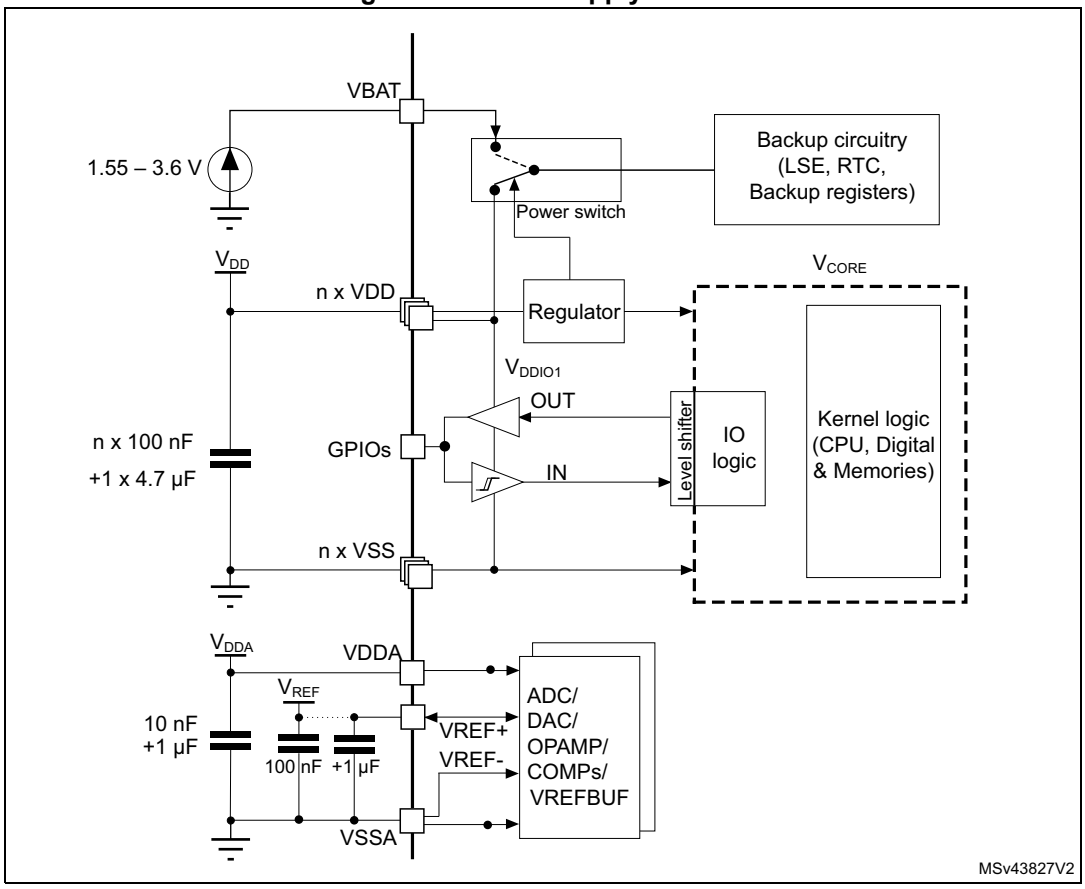


MSv40953V1

1. The above figure shows the package top view.

6.1.6 Power supply scheme

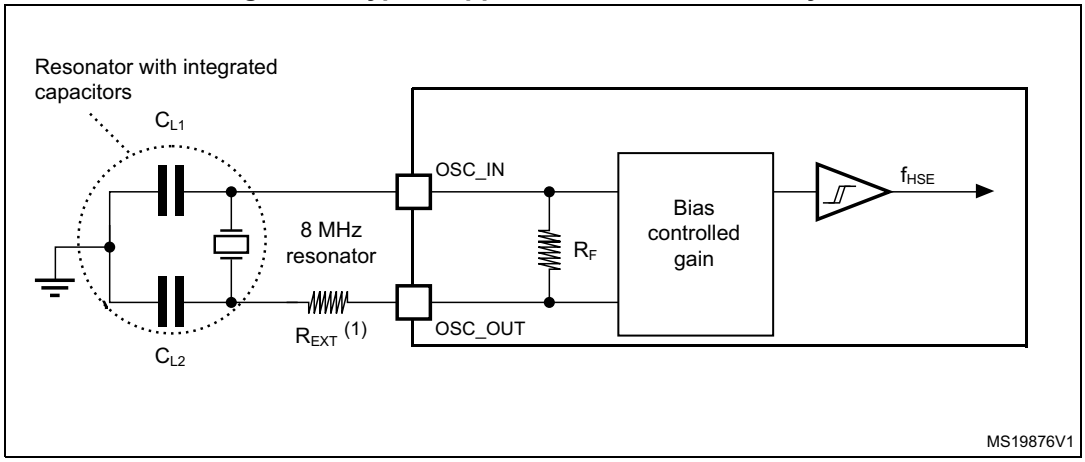
Figure 16. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 21. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 58*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 58. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 69. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 70*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 70. I/O current injection susceptibility(1)

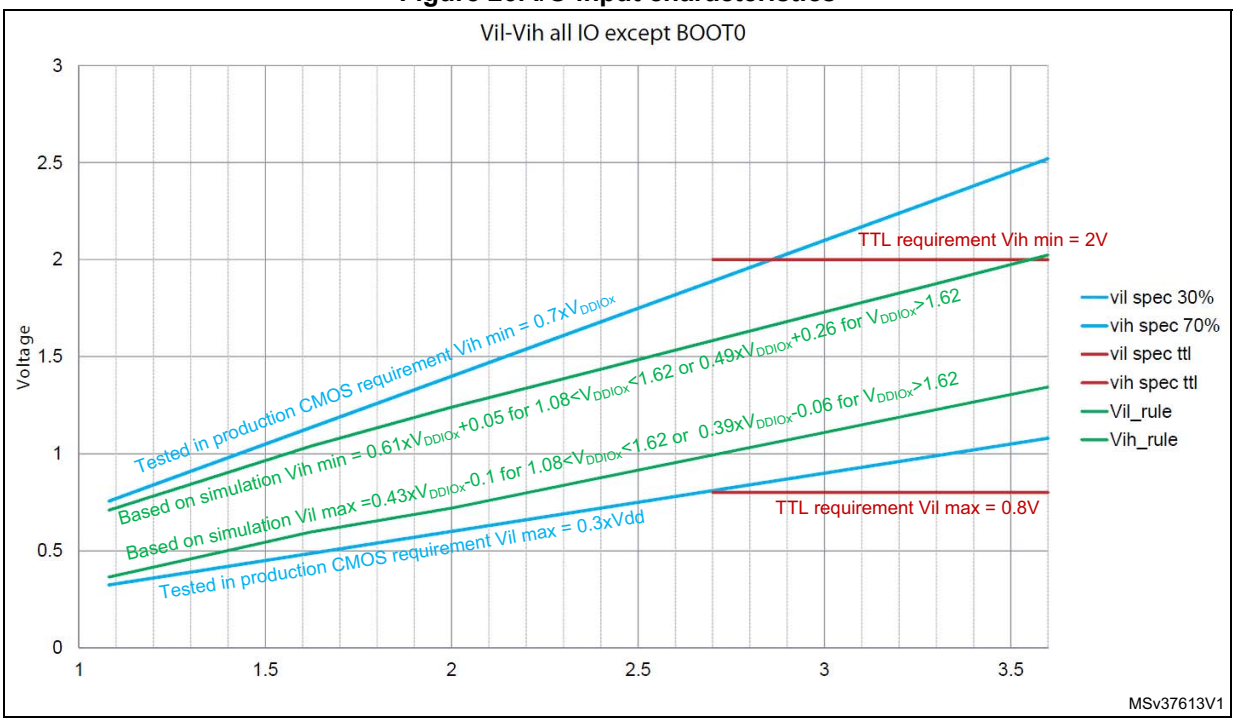
Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PA4, PA5, PE8, PE9, PE10, PE11, PE12	-5	N/A(2)	mA
	Injected current on PE8, PE9, PE10, PE11, PE12	-0	N/A(2)	
	Injected current on PA4, PA5 pins	-5	0	

1. Guaranteed by characterization results.
2. Injection is not possible.

1. Refer to *Figure 26: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. All FT_xx IO except FT_u and PC3 I/O.
5. Max(V_{DDXXX}) is the maximum value of all the I/O supplies.
6. To sustain a voltage higher than Min(V_{DD}, V_{DDA}, V_{DDUSB}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
7. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 26* for standard I/Os, and in *Figure 26* for 5 V tolerant I/Os.

Figure 26. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

Table 73. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	28	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(4)		-	5	ns

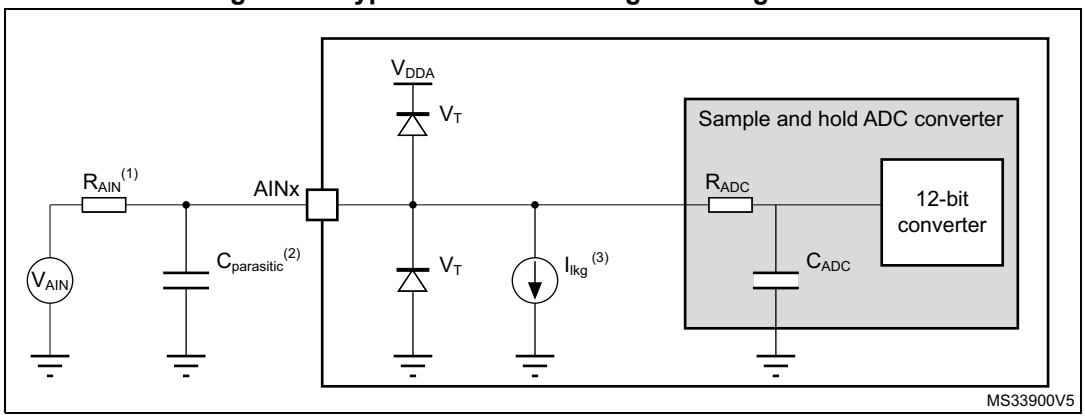
1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0394 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

Table 78. Maximum ADC R_{AIN}(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

1. Guaranteed by design.

Figure 30. Typical connection diagram using the ADC



1. Refer to *Table 77: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 71: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 71: I/O static characteristics* for the values of Ilkg.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 16: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.21 Comparator characteristics

Table 86. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	40	
t_D(3)	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	

Table 106. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 51. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint

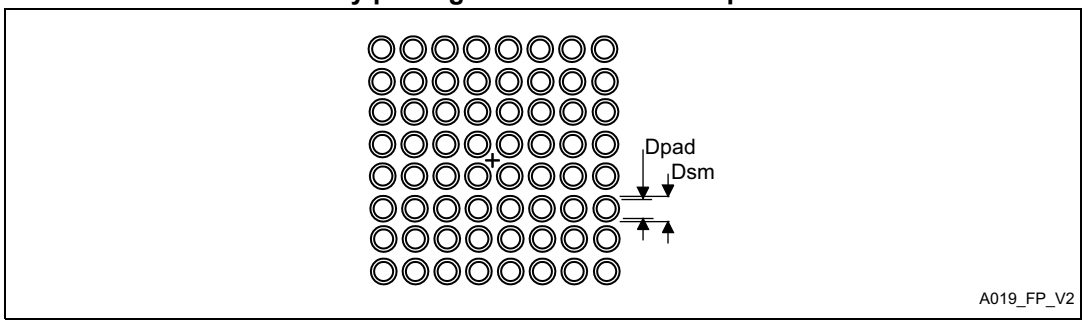


Table 107. UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm

Table 109. WLCSP64 recommended PCB design rules (0.4 mm pitch)

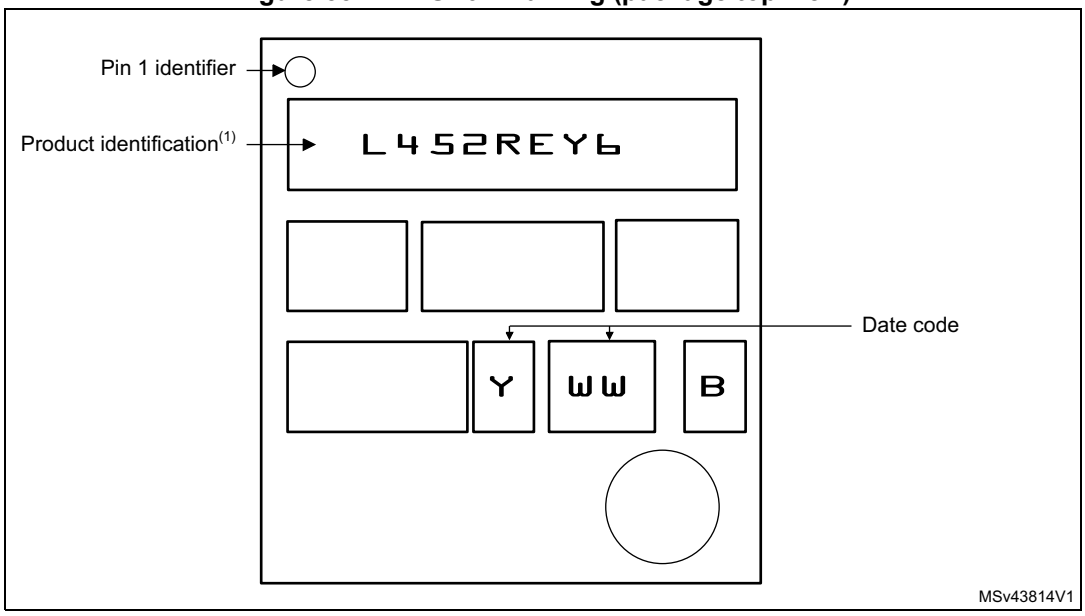
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 55. WLCSP64 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.