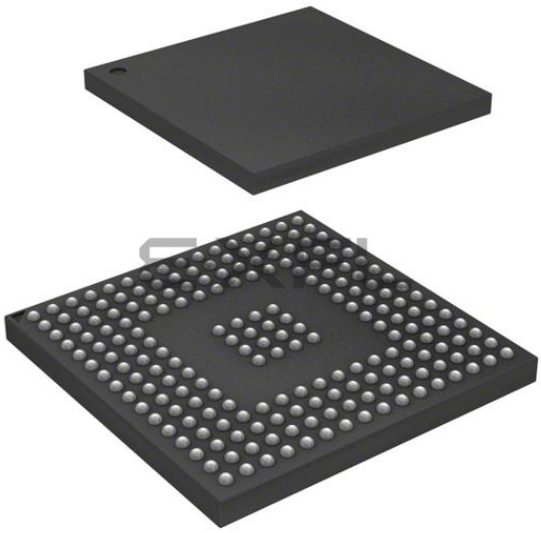
Infineon Technologies - SAF-TC1100-L100EB BB Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1100-l100eb-bb

TC1100 Data Sheet
Advance Information
Revision History: 2005-02 V1.0

Previous Version: none

Page	Subjects (major changes since last revision)

Controller Area Network (CAN): License of Robert Bosch GmbH

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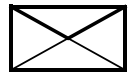


Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P1		I/O		**Port 1** Port 1 serves as 16-bit bi-directional general purpose I/O port which can be used for input/output for OCDS L2, SSC0/1, EBU and SCU.	
P1.0	D11	I	PUC	SWCFG0	Software configuration 0
		O		OCDSA_0	OCDS L2 Debug Line A0
P1.1	C12	I	PUC	SWCFG1	Software configuration 1
		O		OCDSA_1	OCDS L2 Debug Line A1
P1.2	D12	I	PUC	SWCFG2	Software configuration 2
		O		OCDSA_2	OCDS L2 Debug Line A2
P1.3	B12	I	PUC	SWCFG3	Software configuration 3
		O		OCDSA_3	OCDS L2 Debug Line A3
P1.4	C11	I	PUC	SWCFG4	Software configuration 4
		O		OCDSA_4	OCDS L2 Debug Line A4
P1.5	C13	I	PUC	SWCFG5	Software configuration 5
		O		OCDSA_5	OCDS L2 Debug Line A5
P1.6	A12	I	PUC	SWCFG6	Software configuration 6
		O		OCDSA_6	OCDS L2 Debug Line A6
P1.7	B13	I	PUC	SWCFG7	Software configuration 7
		O		OCDSA_7	OCDS L2 Debug Line A7
P1.8	A13	I	PUC	SWCFG8	Software configuration 8
		O		OCDSA_8	OCDS L2 Debug Line A8
P1.9	A14	I	PUC	SWCFG9	Software configuration 9
		O		OCDSA_9	OCDS L2 Debug Line A9
P1.10	B14	I	PUC	SWCFG10	Software configuration 10
		O		OCDSA_10	OCDS L2 Debug Line A10
P1.11	C14	I	PUC	SWCFG11	Software configuration 11
		O		OCDSA_11	OCDS L2 Debug Line A1
		O		SLSO0_1	SSC0 Slave Select output 1
P1.12	F13	I	PUC	SWCFG12	Software configuration 12
		O		OCDSA_12	OCDS L2 Debug Line A12
		O		SLSO1_1	SSC1 Slave Select output 1
P1.13	E14	I	PUC	SWCFG13	Software configuration 13
		O		OCDSA_13	OCDS L2 Debug Line A13
		O		SLSO0_2	SSC0 Slave Select output 2
P1.14	D14	O	PUC	SLSO1_2	SSC1 Slave Select output 2
		I		SWCFG14	Software configuration 14
		O		OCDSA_14	OCDS L2 Debug Line A14

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P1.15	F14	I O I O	PUC	SLSI0 RMW SWCFG15 OCDSA_15	SSC0 Slave Select Input EBU Read Modify Write Software configuration 15 OCDS L2 Debug Line A15
P2		I/O		**Port 2** Port 2 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for ASC0/1, SSC0/1, IIC, EBU and SCU.	
P2.0	P12	I/O O	PUC	RXD0 CSEMU	ASC0 receiver input/output line EBU Chip Select Output for Emulator Region
P2.1	P11	O I	PUC	TXD0 TESTMODE	ASC0 transmitter output line Test Mode Select Input
P2.2	P13	I/O	PUC	MRST0	SSC0 master receive/slave transmit input/output
P2.3	P14	I/O	PUC	MTSR0	SSC0 master transmit/slave receive input/output
P2.4	N15	I/O	PUC	SCLK0	SSC0 clock input/output line
P2.5	N14	I/O	PUC	MRST1A	SSC1 master receive/slave transmit input/output A
P2.6	N12	I/O	PUC	MTSR1A	SSC1 master transmit/slave receive input/output A
P2.7	K16	I/O	PUC	SCLK1A	SSC1 clock input/output line A
P2.8	J16	I/O	PUC	RXD1A	ASC1 receiver input/output line A
P2.9	H16	O	PUC	TXD1A	ASC1 transmitter output line A
P2.10	L13	—	PUC	—	
P2.11	G16	—	PUC	—	
P2.12	K15	I/O O	—	SDA0 SLSO0_3	IIC Serial Data line 0 SSC0 Slave Select output 3
P2.13	K14	I/O O	—	SCL0 SLSO1_3	IIC clock line 0 SSC1 Slave Select output 3
P2.14	F16	I/O O	—	SDA1 SLSO0_4	IIC Serial Data line 1 SSC0 Slave Select output 4
P2.15	E16	I/O O	—	SCL1 SLSO1_4	IIC clock line 1 SSC1 Slave Select output 4

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
BFCLKI	D1	I	—	**Burst Flash Clock Input (Clock Feedback)**
BFCLKO	E1	O	—	**Burst Flash Clock Output** Accesses to Burst Flash devices are synchronized to this clock.
$\overline{RD}$	P2	O	PUC	**EBU Read Control Line** Output in master mode Input in slave mode
RD/$\overline{WR}$	T3	O	PUC	**EBU Write Control Line** Output in master mode Input in slave mode
$\overline{WAIT}$	B9	I	PUC	**EBU Wait Control Line**
ALE	R3	O	PDC	**EBU Address Latch Enable Output**
MR/$\overline{W}$	P3	O	PUC	**EBU Motorola-style Read/Write Output**
$\overline{BAA}$	A11	O	PUC	**EBU Burst Address Advance Output** For advancing address in a Burst Flash access
$\overline{ADV}$	B11	O	PUC	**EBU Burst Flash Address Valid Output**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
				EBU Address Bus Input/Output Lines
A0	K1	O	PUC	EBU Address Bus Line 0
A1	L1	O	PUC	EBU Address Bus Line 1
A2	M1	O	PUC	EBU Address Bus Line 2
A3	N1	O	PUC	EBU Address Bus Line 3
A4	P1	O	PUC	EBU Address Bus Line 4
A5	J2	O	PUC	EBU Address Bus Line 5
A6	K2	O	PUC	EBU Address Bus Line 6
A7	L2	O	PUC	EBU Address Bus Line 7
A8	M2	O	PUC	EBU Address Bus Line 8
A9	N2	O	PUC	EBU Address Bus Line 9
A10	J3	O	PUC	EBU Address Bus Line 10
A11	K3	O	PUC	EBU Address Bus Line 11
A12	L3	O	PUC	EBU Address Bus Line 12
A13	M3	O	PUC	EBU Address Bus Line 13
A14	K4	O	PUC	EBU Address Bus Line 14
A15	A8	O	PUC	EBU Address Bus Line 15
A16	A9	O	PUC	EBU Address Bus Line 16
A17	A10	O	PUC	EBU Address Bus Line 17
A18	B10	O	PUC	EBU Address Bus Line 18
A19	C10	O	PUC	EBU Address Bus Line 19
A20	D10	O	PUC	EBU Address Bus Line 20
A21	T4	O	PUC	EBU Address Bus Line 21
A22	R4	O	PUC	EBU Address Bus Line 22
A23	P4	O	PUC	EBU Address Bus Line 23
XTAL1	M16	I	—	**Oscillator/PLL/Clock Generator Input/Output Pins**
XTAL2	N16	O	—	XTAL1 is the input to the main oscillator amplifier and input to the internal clock generator. XTAL2 is the output of the main oscillator amplifier circuit. For clocking of the device from an external source, XTAL1 is driven with the clock signal while XTAL2 is left unconnected. For crystal oscillator operation, XTAL1 and XTAL2 are connected to the crystal with the appropriate recommended oscillator circuitry.
V_{DDOSC3}	P16	—	—	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC3}	R16	—	—	**Main Oscillator Ground**
V_{DDOSC}	L16	—	—	**Main Oscillator Power Supply (1.5 V)**

Table 3-1 TC1100 Block Address Map (cont'd)

Seg-ment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
13	D000 0000$_H$ – D000 6FFF$_H$	28 KB	DMI Local Data RAM (LDRAM)	DMI local	via LMB	non-cached
	D000 7000$_H$ – D3FF FFFF$_H$	~ 64 MB	Reserved			
	D400 0000$_H$ – D400 7FFF$_H$	32 KB	PMI Local Code Scratch Pad RAM (SPRAM)	via LMB	PMI local	
	D400 8000$_H$ – D7FF FFFF$_H$	~64 MB	Reserved			
	D800 0000$_H$ – DDFF FFFF$_H$	96 MB	External Memory Space	via LMB	via LMB	
	DE00 0000$_H$ – DEFF FFFF$_H$	16 MB	Emulator Memory Space			
	DF00 0000$_H$ – DFFF BFFF$_H$	~16 MB	Reserved	–	–	
	DFFF C000$_H$ – DFFF FFFF$_H$	16 KB	Boot ROM Space	via FPI	via FPI	
14	E000 0000$_H$ – E7FF FFFF$_H$	128 MB	External Memory Space	via LMB	via LMB	
	E800 0000$_H$ – E83F FFFF$_H$	4 MB	Reserved for mapped space for lower 4 Mbytes of Local Memory in Segment 12 (Transformed by LFI bridge to C000 0000$_H$ – C03F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E840 0000$_H$ – E84F FFFF$_H$	1 MB	Reserved for mapped space for lower 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D000 0000$_H$ – D00F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E850 0000$_H$ – E85F FFFF$_H$	1 MB	Reserved for mapped space for 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D400 0000$_H$ – D40F FFFF$_H$)			

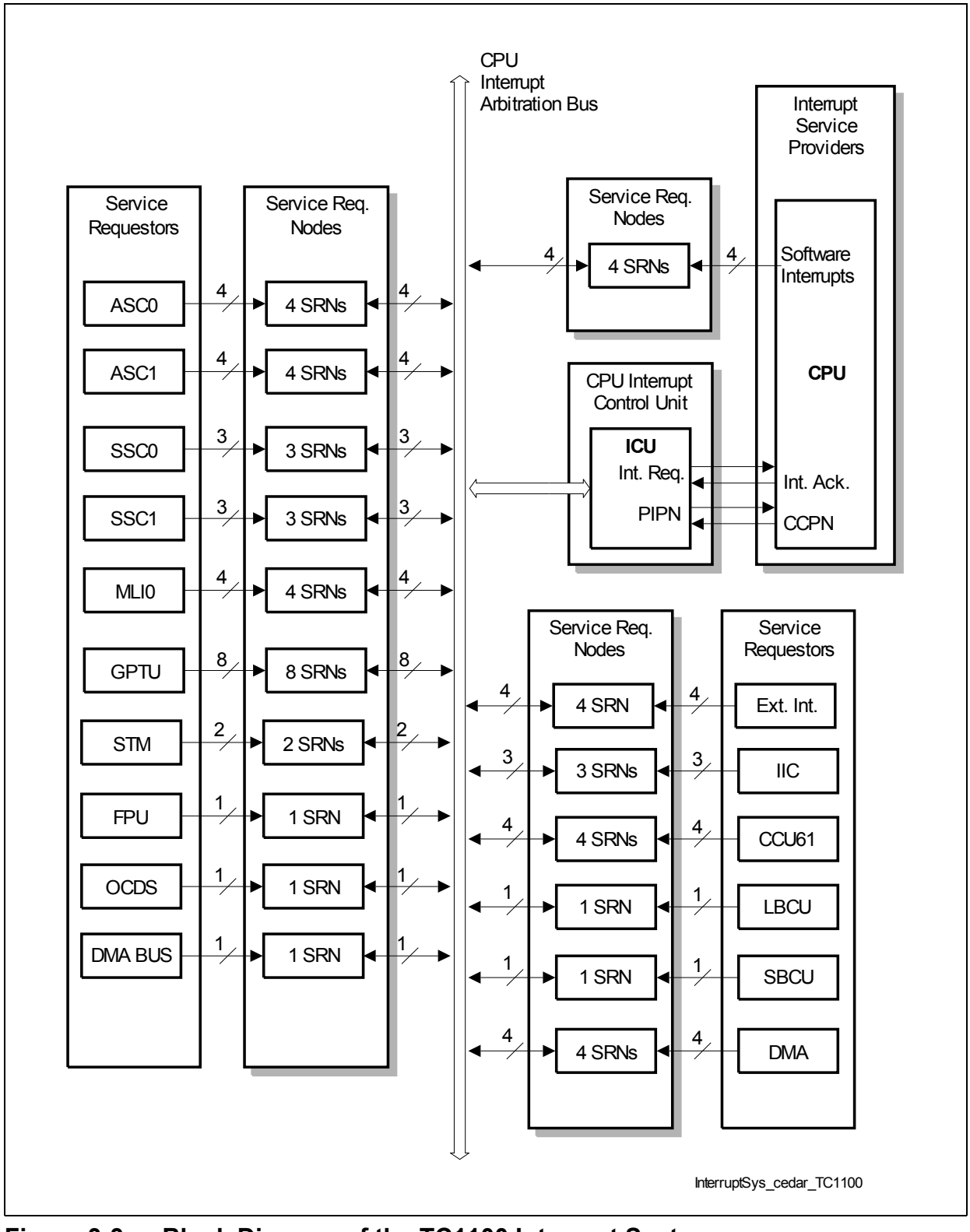


Figure 3-3 Block Diagram of the TC1100 Interrupt System

3.8 Parallel Ports

The TC1100 has 72 digital input/output port lines, which are organized into four parallel 16-bit ports and one parallel 8-bit port, Port P0 to Port P4 with 3.3 V nominal voltage.

The digital parallel ports can be used as general purpose I/O lines or they can perform input/output functions for the on-chip peripheral units. An overview on the port-to-peripheral unit assignment is shown in **Figure 3-4**.

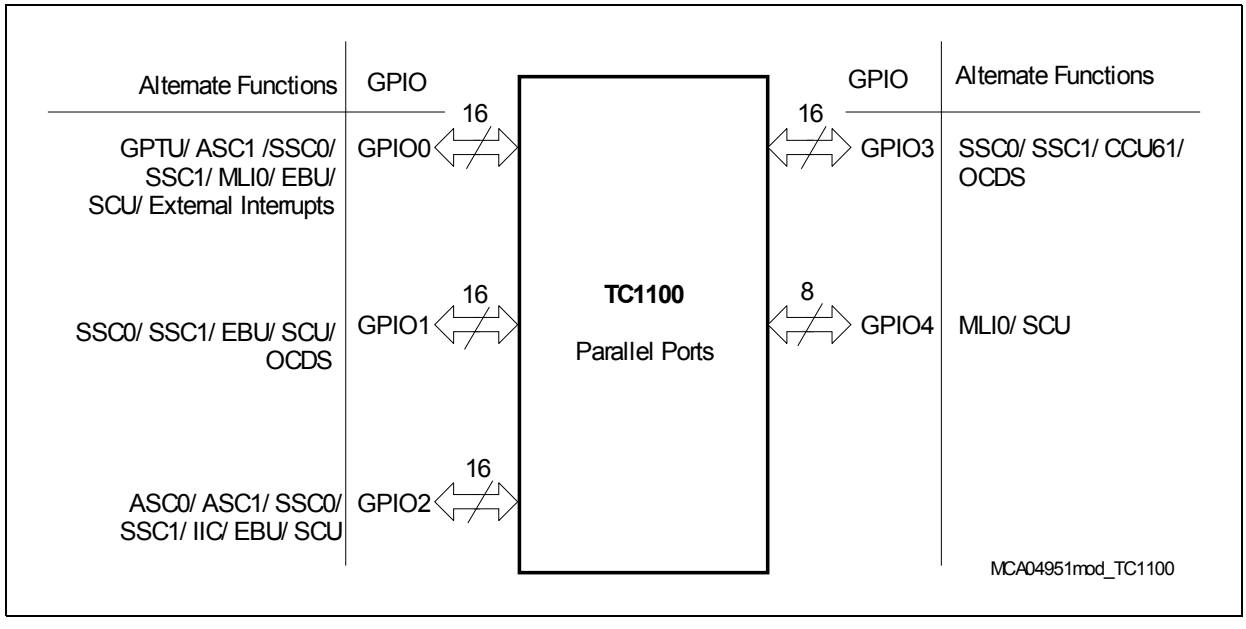


Figure 3-4 Parallel Ports of the TC1100

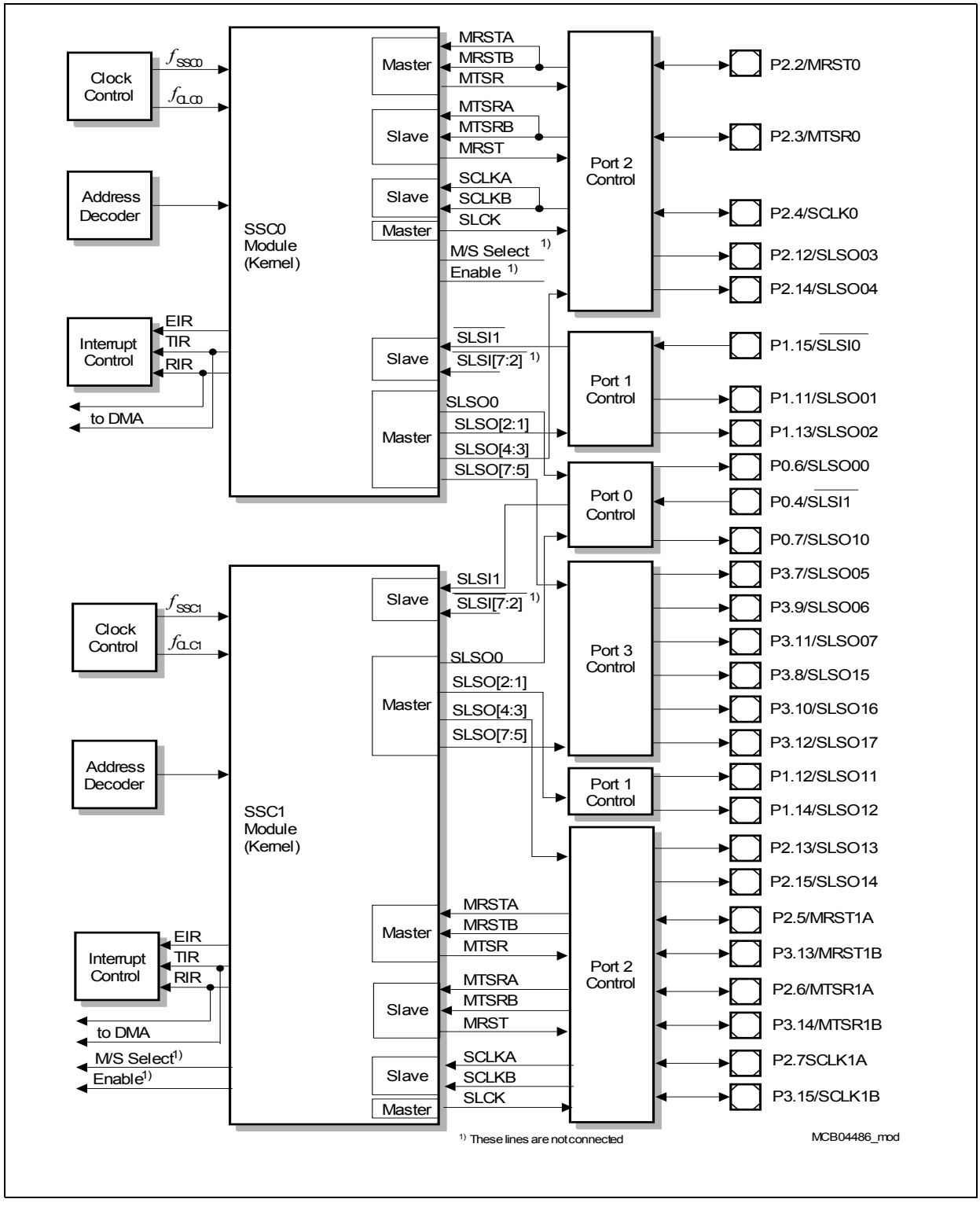


Figure 3-6 General Block Diagram of the SSC Interfaces

- Evaluation of the device address in slave mode
- Bus access arbitration in multimaster mode

Features:

- Extended buffer allows up to 4 send/receive data bytes to be stored
- Selectable baud rate generation
- Support of standard 100 kBaud and extended 400 kBaud data rates
- Operation in 7-bit addressing mode or 10-bit addressing mode
- Flexible control via interrupt service routines or by polling
- Dynamic access to up to 2 physical IIC buses

3.15 System Timer

The STM within the TC1100 is designed for global system timing applications requiring both high precision and long range. The STM provides the following features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible interrupt generation on partial STM content compare match
- Driven by clock f_{STM} after reset (default after reset is $f_{STM} = f_{SYS} = 150$ MHz)
- Counting starts automatically after a reset operation
- STM is reset under following reset causes:
  - Wake-up reset (PMG_CON.DSRW must be set)
  - Software reset (RST_REQ.RRSTM must be set)
  - Power-on reset
- STM (and the clock divider) is not reset at watchdog reset and hardware reset ($\overline{\text{HDRST}}$ = 0)

The STM is an upward counter, running with the system clock frequency f_{SYS} (after reset $f_{STM} = f_{SYS}$). It is enabled per default after reset, and immediately starts counting up. Other than via reset, it is not possible to affect the contents of the timer during normal operation of the application; it can only be read, but not written to. Depending on the implementation of the clock control of the STM, the timer can optionally be disabled or suspended for power-saving and debugging purposes via a clock control register.

The maximum clock period is $2^{56}/f_{STM}$. At f_{STM} = 150 MHz (maximum), for example, the STM counts 15.2 years before overflowing. Thus, it is capable of continuously timing the entire expected product lifetime of a system without overflowing.

3.19 Power Management System

The TC1100 power management system allows software to configure the various processing units to adjust automatically in order to draw the minimum necessary power for the application.

There are four power management modes:

- Run Mode
- Idle Mode
- Sleep Mode
- Deep Sleep Mode

Table 3-4 describes the features of the power management modes.

Table 3-4 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to run mode. Idle mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the NMI pin, or any enabled interrupt event will return the system to run mode.
Sleep	The system clock continues to be distributed only to those peripherals programmed to operate in sleep mode. The other peripheral modules will be shut down by the suspend signal. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the NMI pin, or a reset event will return the system to run mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.
Deep Sleep	The system clock is shut off; only an external signal will restart the system. Entering this state requires an orderly shut-down controlled by the Power Management State Machine (PMSM).

Besides these explicit software-controlled power-saving modes, special attention has been paid in the TC1100 to automatic power-saving in operating units that are currently not required or idle. In this case, they are shut off automatically until their operation is required again.

The oscillator circuit, which is designed to work with an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as input and XTAL2 as output.

Figure 3-14 shows the recommended external oscillator circuitries for both operating modes, i.e. external crystal mode and external input clock mode.

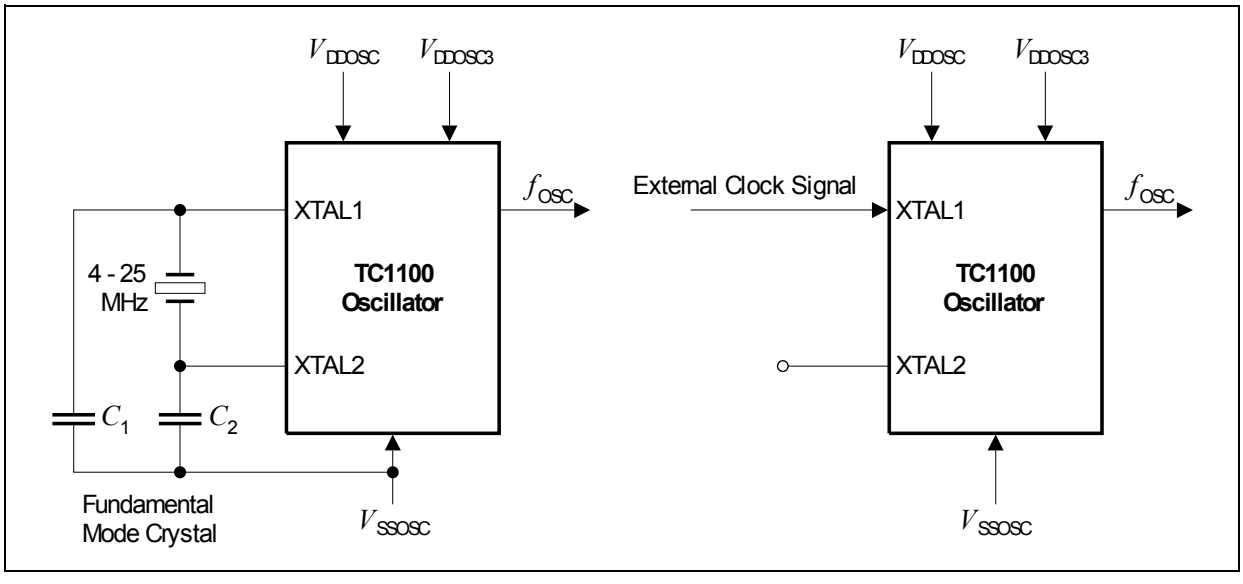


Figure 3-14 Oscillator Circuitries

When using an external clock signal, it must be connected to XTAL1 and XTAL2 is left open (unconnected). When supplying the clock signal directly, not using a crystal and the oscillator, the input frequency can be in the range of 0 - 40 MHz if the PLL is not used, 4 - 40 MHz in case the PLL is used.

When using a crystal, its frequency can be within the range of 4 MHz to 25 MHz. An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It consists normally of the two load capacitances, C1 and C2. For some crystals, a series damp resistor may be necessary. The exact values and related operating range are dependant on the crystal and have to be determined and optimized together with the crystal vendor using the negative resistance method. As starting point for the evaluation and for non-productive systems, the following load capacitor values might be used.

Table 3-5 Load Capacitors Select

Fundamental Mode Crystal Frequency (approx., MHz)	Load Capacitors C1, C2 (pF)
4	33
8	18
12	12
16	10

3.22 Power Supply

The TC1100 provides an ingenious power supply concept in order to improve the EMI behavior as well as to minimize the crosstalk within on-chip modules.

Figure 3-15 shows the TC1100's power supply concept, where certain logic modules are individually supplied with power. This concept improves the EMI behavior by reduction of the noise cross coupling.

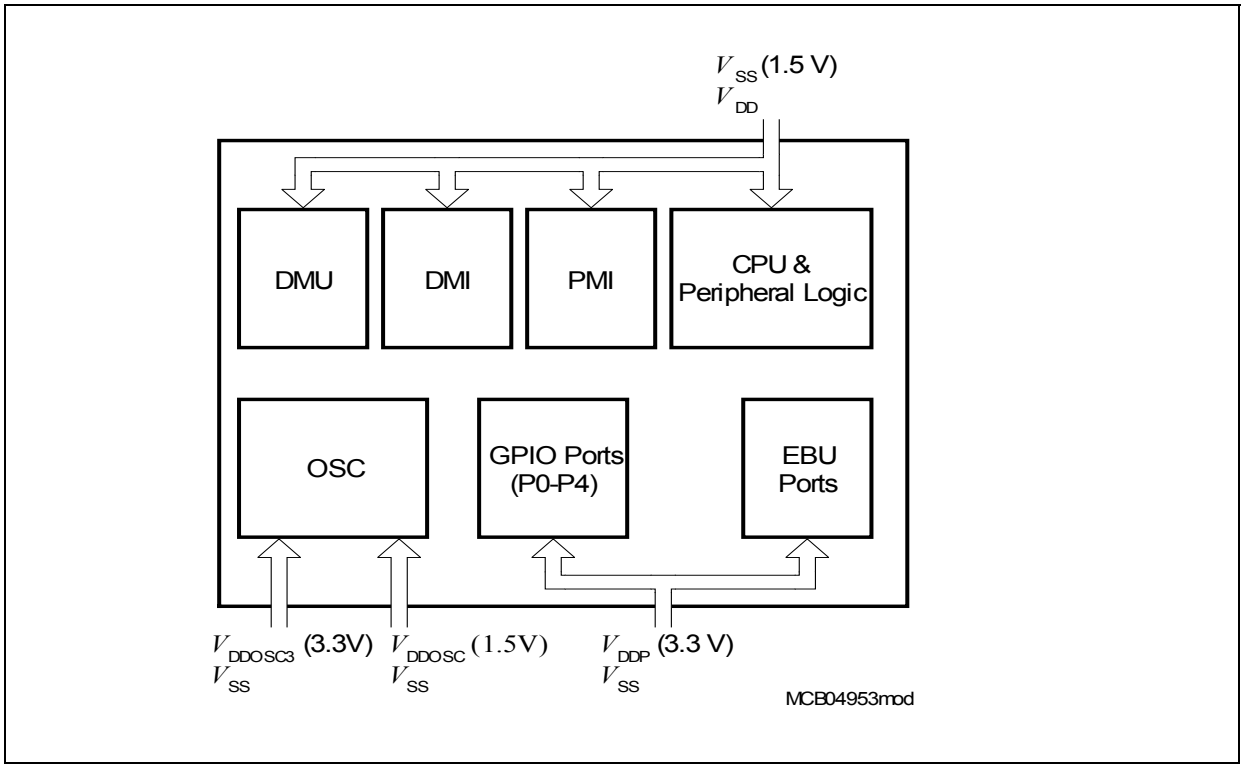


Figure 3-15 TC1100 Power Supply Concept

4 Electrical Parameters

4.1 General Parameters

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the TC1100 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for design purposes, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the TC1100 and must be considered for system design.
- **SR**
  These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the TC1100 is included.

4.1.3 Operating Condition

The following operating conditions must be complied with in order to ensure correct operation of the TC1100. All parameters specified in the following table refer to these operating conditions, unless otherwise indicated.

Parameter	Symbol	Limit Values		Unit	Notes Conditions
		min.	max.		
Digital supply voltage	V_{DD}	1.43	1.58	V	–
	V_{DDP}	3.14	3.47	V	–
Digital ground voltage	V_{SS}	0		V	–
Digital core supply current	I_{DD}	–	525	mA	–
Ambient temperature under bias	T_A	-40	+85	°C	–
CPU clock	f_{SYS}	–[1]	150	MHz	–
Overload current	I_{OV}	-1	1	mA	[2][3]
		-3	3		duty cycle ≤ 25%
Short circuit current	I_{SC}	-1	1	mA	[4]
		-3	3		duty cycle ≤ 25%
Absolute sum of overload + short circuit currents	$\Sigma\|I_{OV}\| + \|I_{SC}\|$	–	|50|	mA	[3]
			|100|		duty cycle ≤ 25%
Inactive device pin current (V_{DD} = V_{DDP} = 0)	I_{ID}	-1	1	mA	–
External load capacitance	C_L	–	50	pF	–
ESD strength	–	2000	–	V	Human Body Model (HBM)

[1] The TC1100 uses a static design, so the minimum operation frequency is 0 MHz. However, due to test time restriction no lower frequency boundary is tested.

[2] Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DDP}$ + 0.5 V or $V_{OV} < V_{SS}$ - 0.5 V). The absolute sum of input overload currents on all digital I/O pins may not exceed **50 mA**. The supply voltage must remain within the specified limits.

[3] Not subject to production test, verified by design/characterization.

[4] Applicable for digital inputs.

4.3.4 Input Clock Timing

(Operating Conditions apply)

Parameter		Symbol	Limits		Unit
			min	max	
Oscillator clock frequency	with PLL	f_{OSC} SR	4	25	MHz
Input clock frequency driving at XTAL1	with PLL	f_{OSCDD} SR	-	40	MHz
Input Clock Duty Cycle (t_1 /t_2)		SR	45	55	%

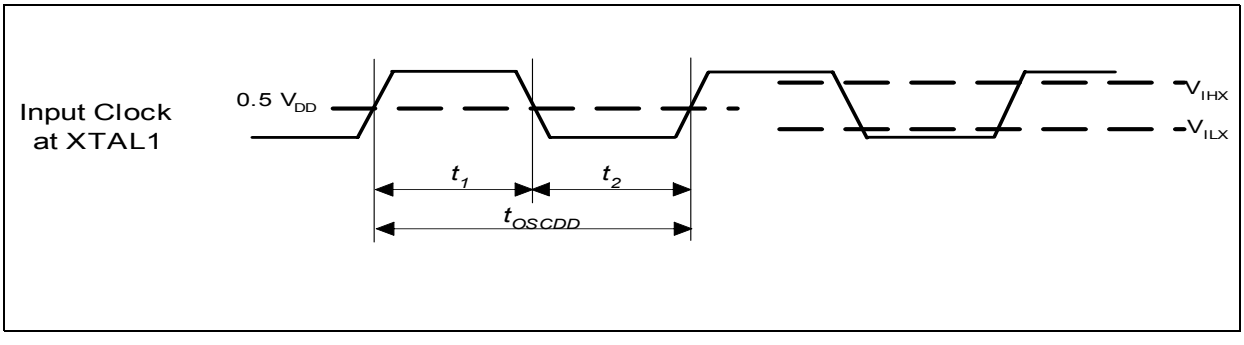
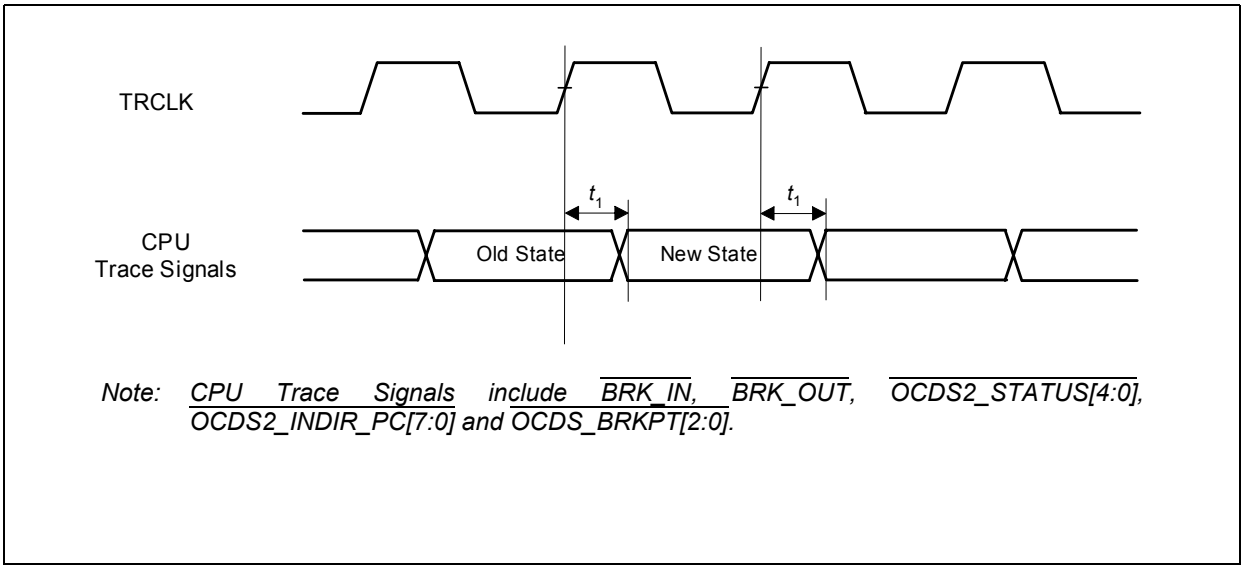


Figure 4-4 Input Clock Timing

4.3.7 Timing for OCDS Trace and Breakpoint Signals

(Operating Conditions apply; C_L(TRCLK) = 25 pF, C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
$\overline{\text{BRK\_OUT}}$ valid from TRCLK ↓	t_1	CC	–	5.2	ns
$\overline{\text{OCDS2\_STATUS[4:0]}}$ valid from TRCLK ↓	t_1	CC	0	5	ns
$\overline{\text{OCDS2\_INDIR\_PC[7:0]}}$ valid from TRCLK ↓	t_1	CC	0	5	ns
$\overline{\text{OCDS2\_BRKPT[2:0]}}$ valid from TRCLK ↓	t_1	CC	0	5	ns



Note: CPU Trace Signals include $\overline{\text{BRK\_IN}}$, $\overline{\text{BRK\_OUT}}$, $\overline{\text{OCDS2\_STATUS[4:0]}}$, $\overline{\text{OCDS2\_INDIR\_PC[7:0]}}$ and $\overline{\text{OCDS\_BRKPT[2:0]}}$.

Figure 4-8 OCDS Trace Signals Timing

4.3.8.6 Timing for Multiplexed Access Signals

(Operating Conditions apply; C_L = 50 pF)[1)]

Parameter	Symbol		Limits		Unit
			min	max	
ALE, $\overline{\text{CSx}}$, RD/$\overline{\text{WR}}$, $\overline{\text{RD}}$, MR/$\overline{\text{W}}$, $\overline{\text{BC(3:0)}}$ output valid time from output clock ↑	t_1	CC	–	9	ns
ALE, $\overline{\text{CSx}}$, RD/$\overline{\text{WR}}$, $\overline{\text{RD}}$, MR/$\overline{\text{W}}$, $\overline{\text{BC(3:0)}}$ output hold time from output clock ↑	t_2	CC	0.0	–	ns
AD(31:0) output valid time from output clock ↑	t_3	CC	–	9	ns
AD(31:0) output hold time from output clock ↑	t_4	CC	0.0	–	ns
AD(31:0) input setup time to output clock ↑	t_5	SR	1.4	–	ns
AD(31:0) input hold time from output clock ↑	t_6	SR	3	–	ns
$\overline{\text{WAIT}}$ input setup time to output clock ↑	t_9	SR	12	–	ns
$\overline{\text{WAIT}}$ input hold time from output clock ↑	t_{10}	SR	3	–	ns
$\overline{\text{RMW}}$ output valid time from output clock ↑	t_{11}	CC	–	8	ns
$\overline{\text{RMW}}$ output hold time from output clock ↑	t_{12}	CC	1.3	–	ns
ALE width	t_{13}	CC	8.5	–	ns
AD(31:0) output hold time from RD/$\overline{\text{WR}}$ ↑	t_{14}	CC	0	–	ns

1) The purpose for characterization of Asynchronous access is to provide the performance of all of the signals to user. User can decide whether an extra cycle is needed or not based on above parameters to generate signals with correct timing sequence. It is user's responsibility to program the correct phase length according to the memory/peripheral device specification and EBU Specification.

4.3.9.2 MLI Interface Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit Values		Unit
			min.	max.	
TCLK/RCLK clock period	t_0	CC/SR	2*T_{MLI} 1)	–	ns
MLI outputs delay from TCLK ↓	t_5	CC	0	8	ns
MLI inputs setup to RCLK ↓	t_6	SR	4	–	ns
MLI inputs hold to RCLK ↓	t_7	SR	4	–	ns
RREADY output delay from TCLK ↓	t_8	CC	0	8	ns

1) $T_{MLImin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 120MHz, t_0 = 16.7ns

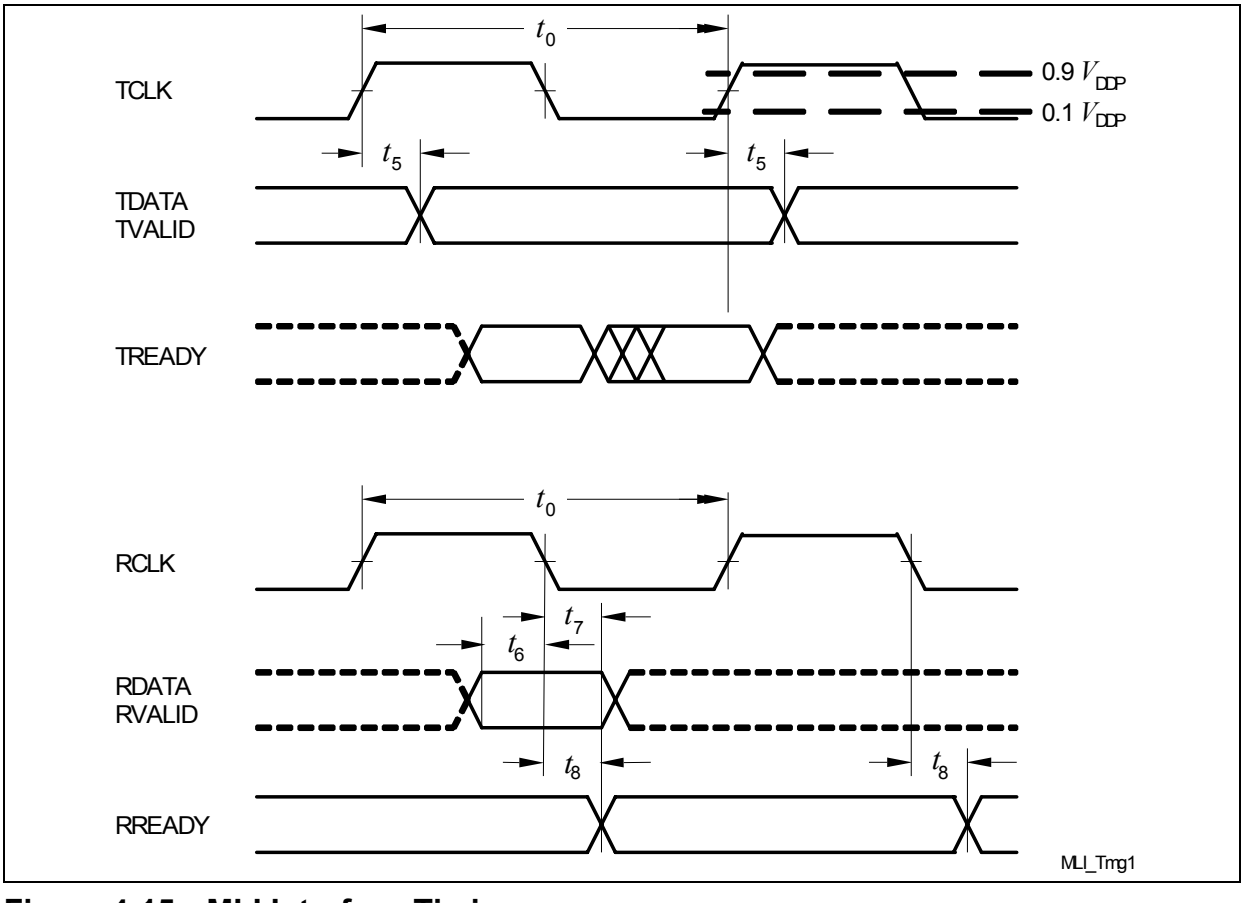


Figure 4-15 MLI Interface Timing

Note: The generation of RREADY is in the input clock domain of the receiver. The reception of TREADY is asynchronous to TCLK.