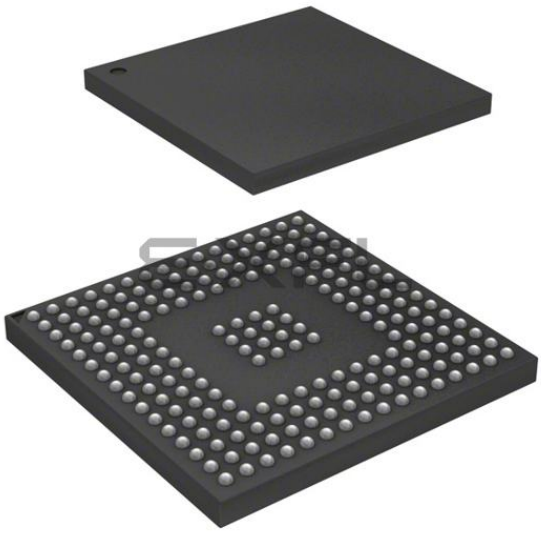
Infineon Technologies - SAF-TC1100-L100EB-G BB Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1100-l100eb-g-bb

2 General Device Information

2.1 Block Diagram

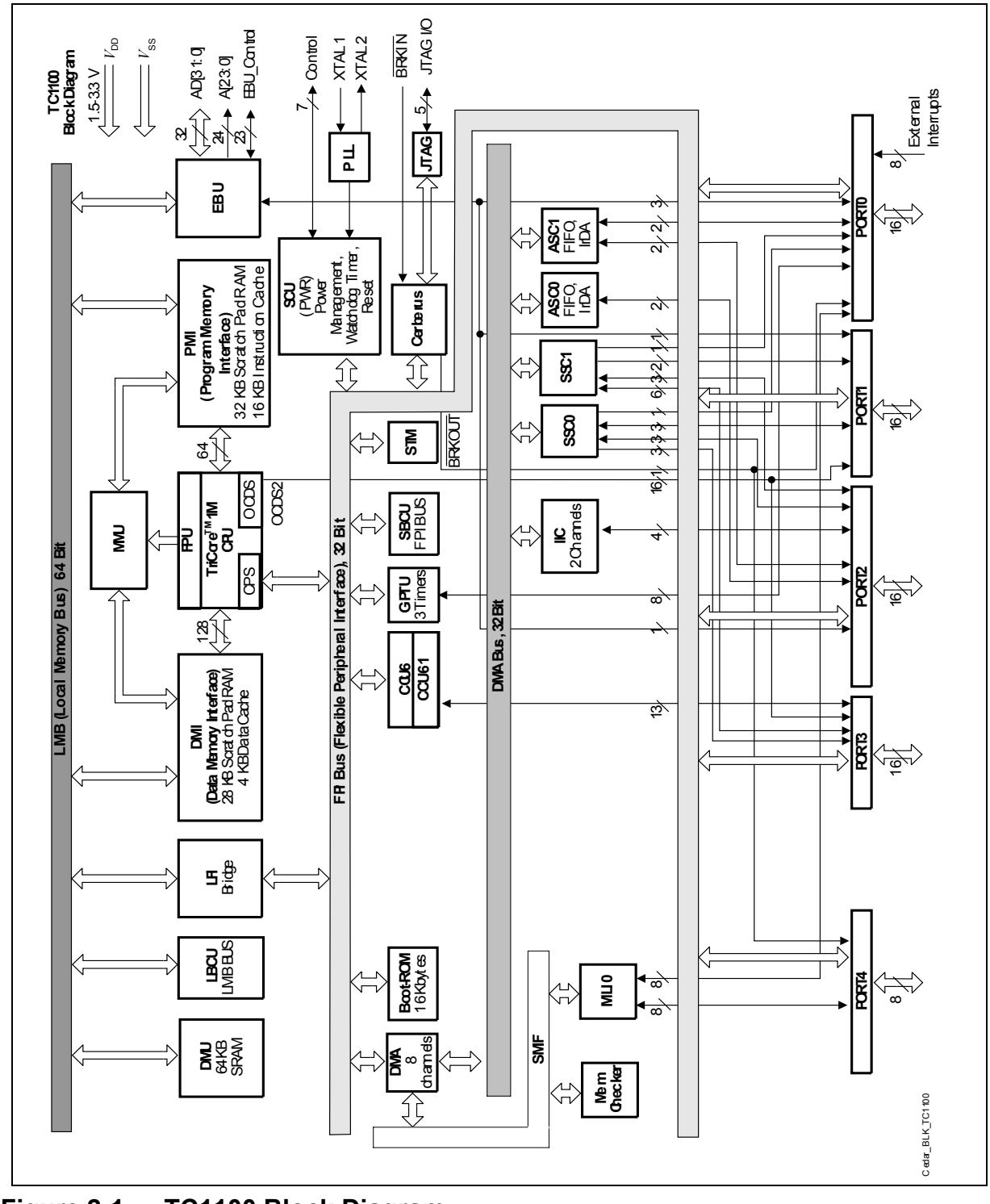

Figure 2-1 TC1100 Block Diagram

2.2 Logic Symbol

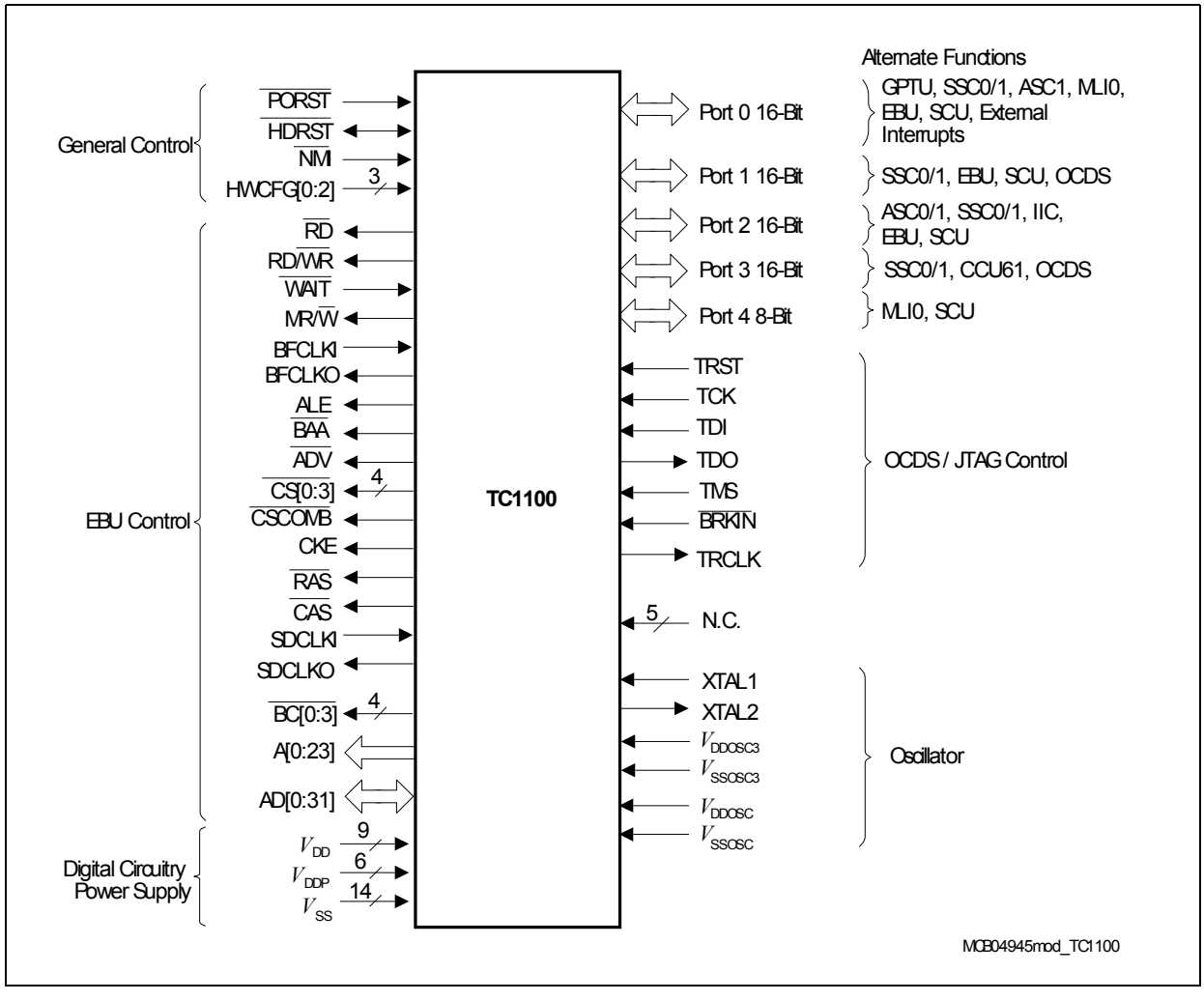

Figure 2-2 TC1100 Logic Symbol

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P1		I/O		**Port 1** Port 1 serves as 16-bit bi-directional general purpose I/O port which can be used for input/output for OCDS L2, SSC0/1, EBU and SCU.	
P1.0	D11	I	PUC	SWCFG0	Software configuration 0
		O		OCDSA_0	OCDS L2 Debug Line A0
P1.1	C12	I	PUC	SWCFG1	Software configuration 1
		O		OCDSA_1	OCDS L2 Debug Line A1
P1.2	D12	I	PUC	SWCFG2	Software configuration 2
		O		OCDSA_2	OCDS L2 Debug Line A2
P1.3	B12	I	PUC	SWCFG3	Software configuration 3
		O		OCDSA_3	OCDS L2 Debug Line A3
P1.4	C11	I	PUC	SWCFG4	Software configuration 4
		O		OCDSA_4	OCDS L2 Debug Line A4
P1.5	C13	I	PUC	SWCFG5	Software configuration 5
		O		OCDSA_5	OCDS L2 Debug Line A5
P1.6	A12	I	PUC	SWCFG6	Software configuration 6
		O		OCDSA_6	OCDS L2 Debug Line A6
P1.7	B13	I	PUC	SWCFG7	Software configuration 7
		O		OCDSA_7	OCDS L2 Debug Line A7
P1.8	A13	I	PUC	SWCFG8	Software configuration 8
		O		OCDSA_8	OCDS L2 Debug Line A8
P1.9	A14	I	PUC	SWCFG9	Software configuration 9
		O		OCDSA_9	OCDS L2 Debug Line A9
P1.10	B14	I	PUC	SWCFG10	Software configuration 10
		O		OCDSA_10	OCDS L2 Debug Line A10
P1.11	C14	I	PUC	SWCFG11	Software configuration 11
		O		OCDSA_11	OCDS L2 Debug Line A1
		O		SLSO0_1	SSC0 Slave Select output 1
P1.12	F13	I	PUC	SWCFG12	Software configuration 12
		O		OCDSA_12	OCDS L2 Debug Line A12
		O		SLSO1_1	SSC1 Slave Select output 1
P1.13	E14	I	PUC	SWCFG13	Software configuration 13
		O		OCDSA_13	OCDS L2 Debug Line A13
		O		SLSO0_2	SSC0 Slave Select output 2
P1.14	D14	O	PUC	SLSO1_2	SSC1 Slave Select output 2
		I		SWCFG14	Software configuration 14
		O		OCDSA_14	OCDS L2 Debug Line A14

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
NMI	T7	I	PUC	**Non-Maskable Interrupt Input** A high-to-low transition on this pin causes a NMI-Trap request to the CPU.
TRST	T11	I	PDC	**JTAG Module Reset/Enable Input** A low level at this pin resets and disables the JTAG module. A high level enables the JTAG module.
TCK	T12	I	PUC	**JTAG Module Clock Input**
TDI	T13	I	PUC	**JTAG Module Serial Data Input**
TDO	T10	O	—	**JTAG Module Serial Data Output**
TMS	T9	I	PUC	**JTAG Module State Machine Control Input**
TRCLK	T8	O	—	**Trace Clock for OCDS_L2 Lines**
HWCFG0 **HWCFG1** **HWCFG2**	M14 L14 T6	I I I	PUC PUC PDC	**Hardware Configuration Inputs** The Configuration Inputs define the boot options of the TC1100 after a hardware invoked reset operation.
BRKIN	T5	I	PUC	**OCDS Break Input** A low level on this pin causes a break in the chip's execution when the OCDS is enabled. In addition, the level of this pin during power-on reset determines the boot configuration.
CS0 **CS1** **CS2** **CS3**	D9 D8 C9 B8	O O O O	PUC PUC PUC PUC	**EBU Chip Select Output Line 0** **EBU Chip Select Output Line 1** **EBU Chip Select Output Line 2** **EBU Chip Select Output Line 3** Each corresponds to a programmable region. Only one can be active at one time.
CSCOMB	N3	O	PUC	**EBU Chip Select Output for Combination Function (Overlay Memory and Global)**
SDCLKI	J1	I	—	**SDRAM Clock Input (Clock Feedback)**
SDCLKO	H1	O	—	**SDRAM Clock Output** Accesses to SDRAM devices are synchronized to this clock.
RAS	D6	O	PUC	**EBU SDRAM Row Address Strobe Output**
CAS	D5	O	PUC	**EBU SDRAM Column Address Strobe Output**
CKE	L4	O	PUC	**EBU SDRAM Clock Enable Output**

Table 3-2 Block Address Map of Segment 15 (cont'd)

Symbol	Description	Address Range	Size
LFI	LMB to FPI Bus Bridge	F87F FF00$_H$ - F87F FFFF$_H$	256 Bytes
–	Reserved	F880 0000$_H$ - FFFF FFFF$_H$	–

Features:

The FPI Bus is designed with the requirements of high-performance systems in mind. The features are:

- Core independent
- Multimaster capability (up to 16 masters)
- Demultiplexed operation
- Clock synchronous
- Peak transfer rate of up to 800 Mbytes/sec (@ 100 MHz bus clock)
- Address and data bus scalable (address bus up to 32 bits, data bus up to 64 bits)
- 8-/16-/32- and 64-bit data transfers
- Broad range of transfer types from single to multiple data transfers
- Split transaction support for agents with long response time
- Burst transfer capability
- EMI and power consumption minimized

3.4.3 LFI

The LMB-to-FPI Interface (LFI) block provides the circuitry to interface (bridge) the FPI bus and the Local Memory Bus (LMB).

LFI Features:

- Full support for bus transactions found within current TriCore™ 1.3 based systems:
  - Single 8/16/32-bit Write/Read transfers from FPI to LMB
  - Single 8/16/32/64-bit Write/Read transfers from LMB to FPI
  - Read-Modify-Write transfers of 8/16/32-bit in both directions
  - Burst transactions of 2, 4 or 8 data beats from the FPI to the LMB
  - Burst transactions of 2 or 4 data beats from the LMB to the FPI
- Address decoding and translation as required by TriCore™ 1.3 implementation
- FPI master interface supports full pipelining on FPI bus
- LMB master interface supports pipelining on LMB within the scope of the LMB specification
- FPI master interface can act as default master on FPI bus
- Programmable support for split LMB to FPI read transactions
- Retry generation on both FPI and LMB buses
- Full support for abort, retry, error and FPI timeout conditions
- Flexible LMB/FPI clock ratio support including dynamic clock switching support
- LFI core clock may be shut down when no transactions are being issued to LFI from either bus and the LFI has no transactions in progress, thus saving power.

3.6 Direct Memory Access (DMA)

The Direct Memory Access Controller executes DMA transactions from a source address location to a destination address location, without intervention of the CPU. One DMA transaction is controlled by one DMA channel. Each DMA channel has assigned its own channel register set. The total of 8 channels are provided by one DMA sub-block.

The DMA module is connected to 3 bus interfaces in TC1100, the Flexible Peripheral Interconnect Bus (FPI), the DMA Bus and the Micro Link Bus. It can do transfers on each of the buses as well as between the buses.

In addition, it bridges accesses from the Flexible Peripheral Interconnect Bus to the peripherals on the DMA Bus, allowing easy access to these peripherals by CPU. Clock control, address decoding, DMA request wiring, and DMA interrupt service request control are implementation specific and managed outside the DMA controller kernel.

Features:

- 8 independent DMA channels
  - Up to 8 selectable request inputs per DMA channel
  - Programmable priority of DMA channels within a DMA sub-block (2 levels)
  - Software and hardware DMA request generation
  - Hardware requests by selected peripherals and external inputs
- Programmable priority of the DMA sub-block on the bus interfaces
- Buffer capability for move actions on the buses (min. 1 move per bus is buffered)
- Individually programmable operation modes for each DMA channel
  - Single mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated
  - Programmable address modification
- Full 32-bit addressing capability of each DMA channel
  - 4-Gbyte address range
  - Support of circular buffer addressing mode
- Programmable data width of a DMA transaction: 8-bit, 16-bit, or 32-bit
- Micro Link supported
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channels is also implemented in the DMA module)
- All buses/interfaces connected to the DMA module must work at the same frequency.
- Read/write requests of the FPI Bus Side to the Remote Peripherals are bridged to the DMA Bus (only the DMA is master on the DMA bus)

The basic structure and external interconnections of the DMA are shown in **Figure 3-2**.

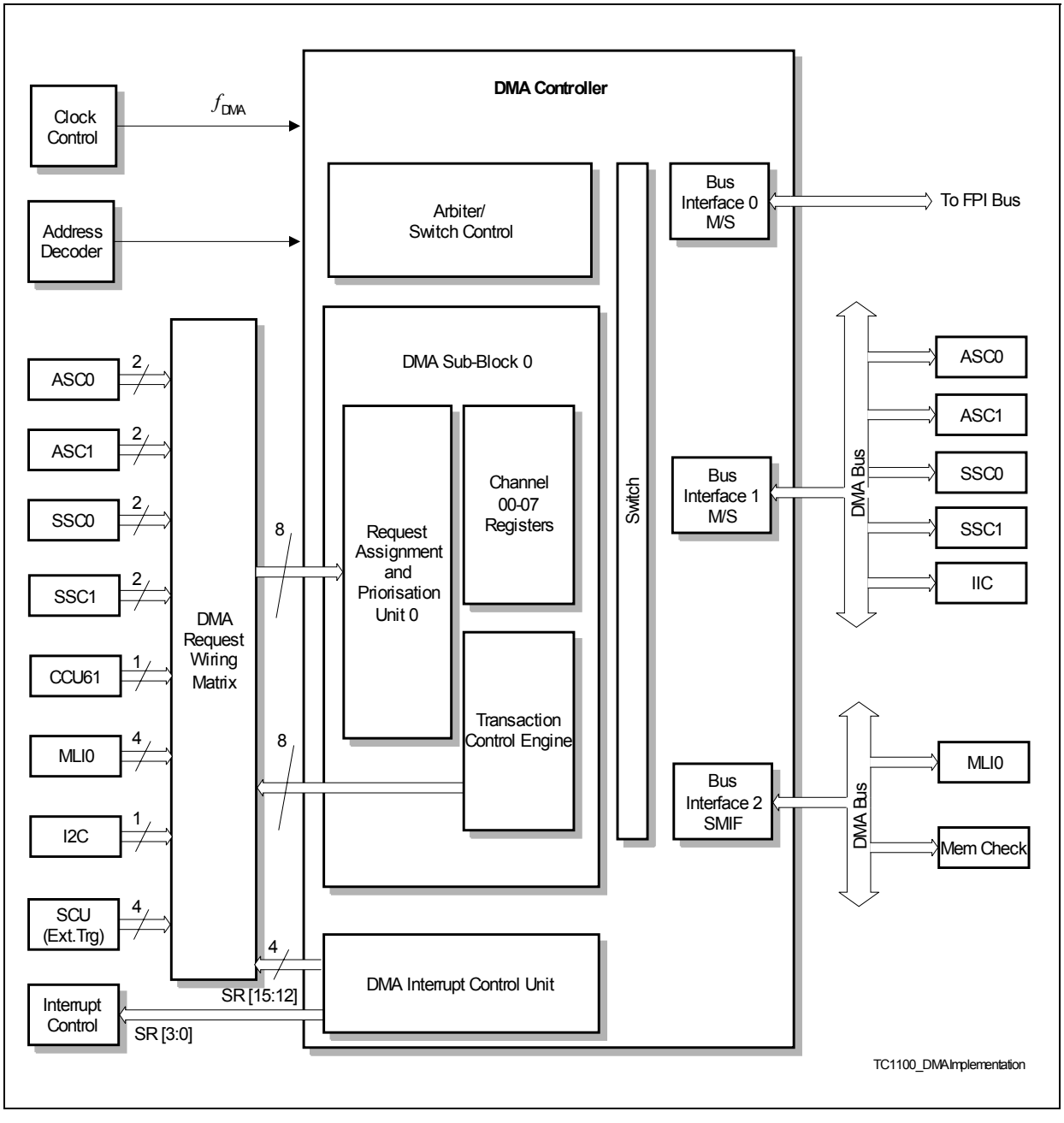

Figure 3-2 DMA Controller Structure and Interconnections

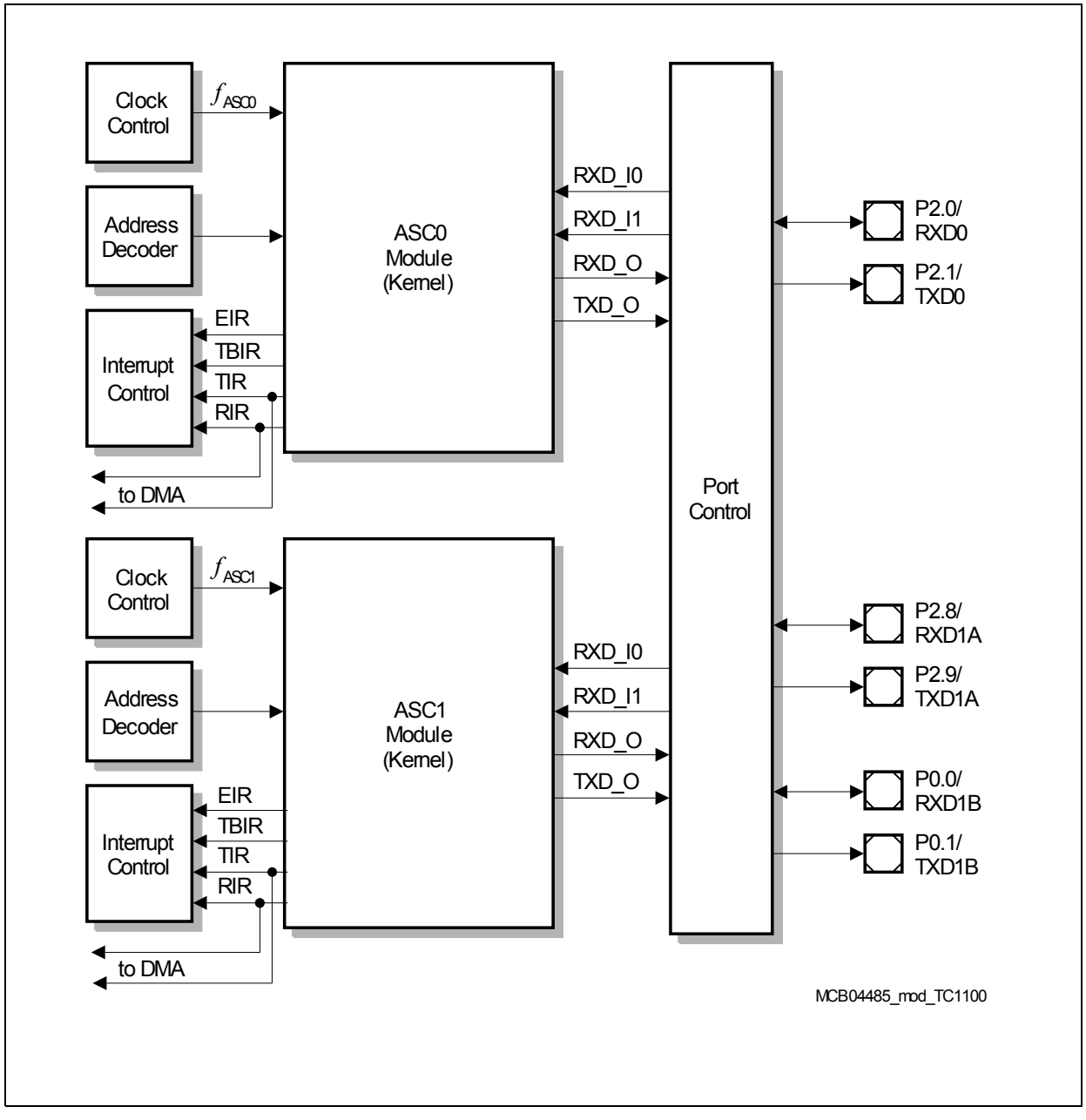

Figure 3-5 General Block Diagram of the ASC Interfaces

Features:

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baud rate from 4.6875 MBaud to 1.1 Baud (@ 75 MHz clock)
- Multiprocessor mode for automatic address/data byte detection

3.13 General Purpose Timer Unit (GPTU)

Figure 3-9 shows a global view of the functional blocks of the General Purpose Timer Unit (GPTU).

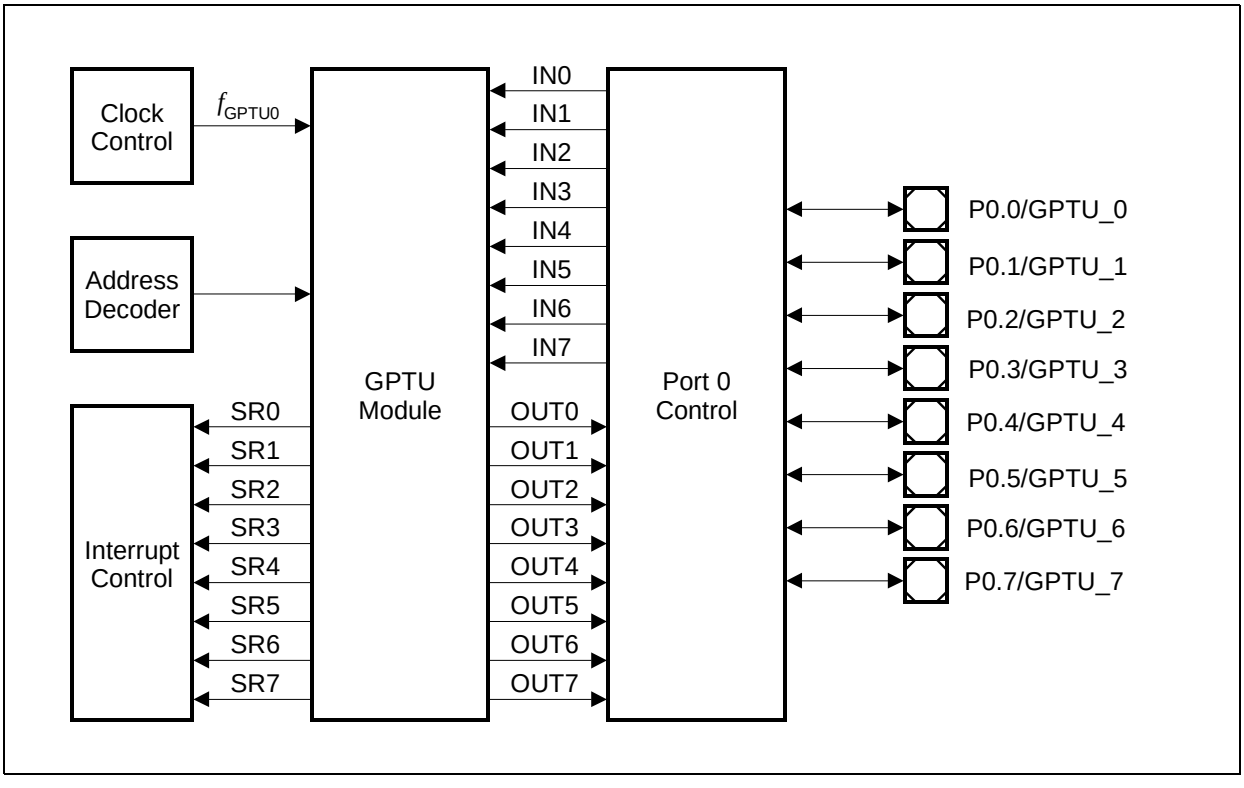

Figure 3-9 General Block Diagram of the GPTU Interface

The GPTU consists of three 32-bit timers designed to solve such application tasks as event timing, event counting, and event recording. The GPTU communicates with the external world via eight I/O lines located at Port 0.

The three timers of GPTU module, T0, T1 and T2, can operate independently of each other or can be combined:

General Features:

- All timers are 32-bit precision timers with a maximum input frequency of f_{GPTU}
- Events generated in T0 or T1 can be used to trigger actions in T2
- Timer overflow or underflow in T2 can be used to clock either T0 or T1
- T0 and T1 can be concatenated to form one 64-bit timer

Features of T0 and T1:

- Each timer has a dedicated 32-bit reload register with automatic reload on overflow
- Timers can be split into individual 8-, 16-, or 24-bit timers with individual reload registers

- Overflow signals can be selected to generate service requests, pin output signals, and T2 trigger events
- Two input pins can define a count option

Features of T2:

- Count up or down is selectable
- Operating modes:
  - Timer
  - Counter
  - Quadrature counter (incremental/phase encoded counter interface)
- Options:
  - External start/stop, one-shot operation, timer clear on external event
  - Count direction control through software or an external event
  - Two 32-bit reload/capture registers
- Reload modes:
  - Reload on overflow or underflow
  - Reload on external event: positive transition, negative transition, or both transitions
- Capture modes:
  - Capture on external event: positive transition, negative transition, or both transitions
  - Capture and clear timer on external event: positive transition, negative transition, or both transitions
- Can be split into two 16-bit counter/timers
- Timer count, reload, capture, and trigger functions can be assigned to input pins. T0 and T1 overflow events can also be assigned to these functions.
- Overflow and underflow signals can be used to trigger T0 and/or T1 and to toggle output pins
- T2 events are freely assignable to the service request nodes

- Important debugging support is provided through the reset prewarning operation by first issuing an NMI to the CPU before finally resetting the device after a certain period of time.

3.20 On-Chip Debug Support

The On-Chip Debug Support of the TC1100 consists of the following building blocks:

- OCDS L1 module of TriCore™
- OCDS L2 interface of TriCore™
- OCDS L1 module in the BCU of the FPI Bus
- OCDS L1 facilities within the DMA
- OCDS L2 interface of DMA
- OCDS System Control Unit (OSCU)
- Multi Core Break Switch (MCBS)
- JTAG based Debug Interface (Cerberus JDI)
- Suspend functionality of peripherals

Features:

- TriCore™ L1 OCDS:
  - Hardware event generation unit
  - Break by DEBUG instruction or break signal
  - Full Single-Step support in hardware, possible also with software break
  - Access to memory, SFRs, etc. on the fly
- DMA L1 OCDS:
  - Output break request on errors
  - Suspension of pre-selected channels
- Level 2 trace port with 16 pins that outputs either TriCore™, or DMA trace
- OCDS System Control Unit (Cerberus OSCU)
  - Minimum number of pins required (no OCDS enable pin)
  - Hardware allows hot attach of a debugger to a running system
  - System is secure (can be locked from internal)
- Multi Core Break Switch (Cerberus MCBS):
  - TriCore™, DMA, break pins, and BCUs as break sources
  - TriCore™ as break targets; other parts can in addition be suspended
  - Synchronous stop and restart of the system
  - Break to Suspend converter

Figure 3-12 shows a basic block diagram of the building blocks.

3.22 Power Supply

The TC1100 provides an ingenious power supply concept in order to improve the EMI behavior as well as to minimize the crosstalk within on-chip modules.

Figure 3-15 shows the TC1100's power supply concept, where certain logic modules are individually supplied with power. This concept improves the EMI behavior by reduction of the noise cross coupling.

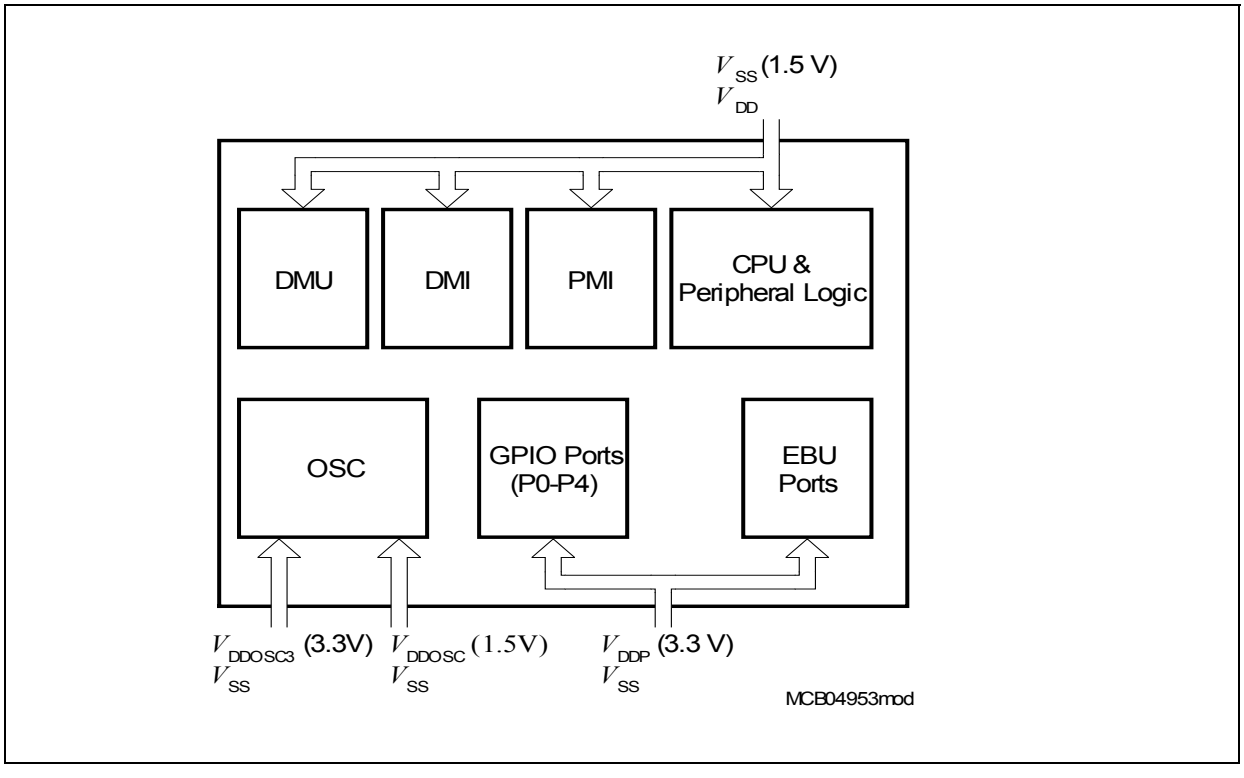

Figure 3-15 TC1100 Power Supply Concept

3.24 Identification Register Values

Table 3-6 TC1100 Identification Registers

Short Name	Address	Value
SCU_ID	F000 0008$_H$	002C C001$_H$
MANID	F000 0070$_H$	0000 1820$_H$
CHIPID	F000 0074$_H$	0000 8C01$_H$
RTID	F000 0078$_H$	0000 0000$_H$
SBCU_ID	F000 0108$_H$	0000 6A0A$_H$
STM_ID	F000 0208$_H$	0000 C005$_H$
CBS_JDPID	F000 0308$_H$	0000 6307$_H$
GPTU_ID	F000 0608$_H$	0001 C002$_H$
CCU61_ID	F000 2108$_H$	0042 C004$_H$
DMA_ID	F000 3C08$_H$	001A C011$_H$
SSC0_ID	F010 0108$_H$	0000 4530$_H$
SSC1_ID	F010 0208$_H$	0000 4530$_H$
ASC0_ID	F010 0308$_H$	0000 44E2$_H$
ASC1_ID	F010 0408$_H$	0000 44E2$_H$
IIC_ID	F010 0608$_H$	0000 4604$_H$
MLI0_ID	F010 C008$_H$	0025 C004$_H$
MCHK_ID	F010 C208$_H$	001B C001$_H$
CPS_ID	F7E0 FF08$_H$	0015 C006$_H$
MMU_ID	F7E1 8008$_H$	0009 C002$_H$
CPU_ID	F7E1 FE18$_H$	000A C005$_H$
EBU_ID	F800 0008$_H$	0014 C004$_H$
DMU_ID	F800 0408$_H$	002D C001$_H$
DMI_ID	F87F FC08$_H$	0008 C004$_H$
PMI_ID	F87F FD08$_H$	000B C004$_H$
LBCU_ID	F87F FE08$_H$	000F C005$_H$
LFI_ID	F87F FF08$_H$	000C C005$_H$

4.2 DC Parameters

4.2.1 Input/Output Characteristics

V_{SS} = 0 V; T_A = -40°C to +125°C

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
GPIO pins, Dedicated pins and EBU pins						
Input low voltage	V_{IL}	SR	-0.3	0.8	V	LvTTL
Input high voltage	V_{IH}	SR	2.0	V_{DDP} + 0.3	V	LvTTL
Output low voltage	V_{OL}	CC	–	0.4	V	I_{OL} = 2mA
Output high voltage	V_{OH}	CC	2.4	–	V	I_{OH} = -2mA
Pull-up current [1]	$\|I_{PUA}\|$	CC	–	149	µA	V_{IN} = 0V
	$\|I_{PUC}\|$	CC	–	7.2	µA	V_{IN} = 0V
Pull-down current [2]	$\|I_{PDA}\|$	CC	–	156	µA	V_{IN} = V_{DDP}
	$\|I_{PDC}\|$	CC	–	15.7	µA	V_{IN} = V_{DDP}
Input leakage current [3]	I_{OZ1}	CC	–	±350	nA	0 < V_{IN} < V_{DDP}
Pin Capacitance [4]	C_{IO}	CC	–	10	pF	f = 1 MHz T_A = 25 °C

1) The current is applicable to the pins, for which a pull-up has been specified. Refer to **Table 2-1**. I_{PUx} refers to the pull-up current for type *x in absolute values*.

2) The current is applicable to the pins, for which a pull-down has been specified. Refer to **Table 2-1**. I_{PDx} refers to the pull-down current for type *x in absolute values*.

3) Excluded following pins: $\overline{\text{NMI}}$, $\overline{\text{TRST}}$, TCK, TDI, TMS, ALE, P2.1,HWCFG0, HWCFG1, HWCFG2, BRKIN, PORST, HDRST.

4) Not subject to production test, verified by design/characterization

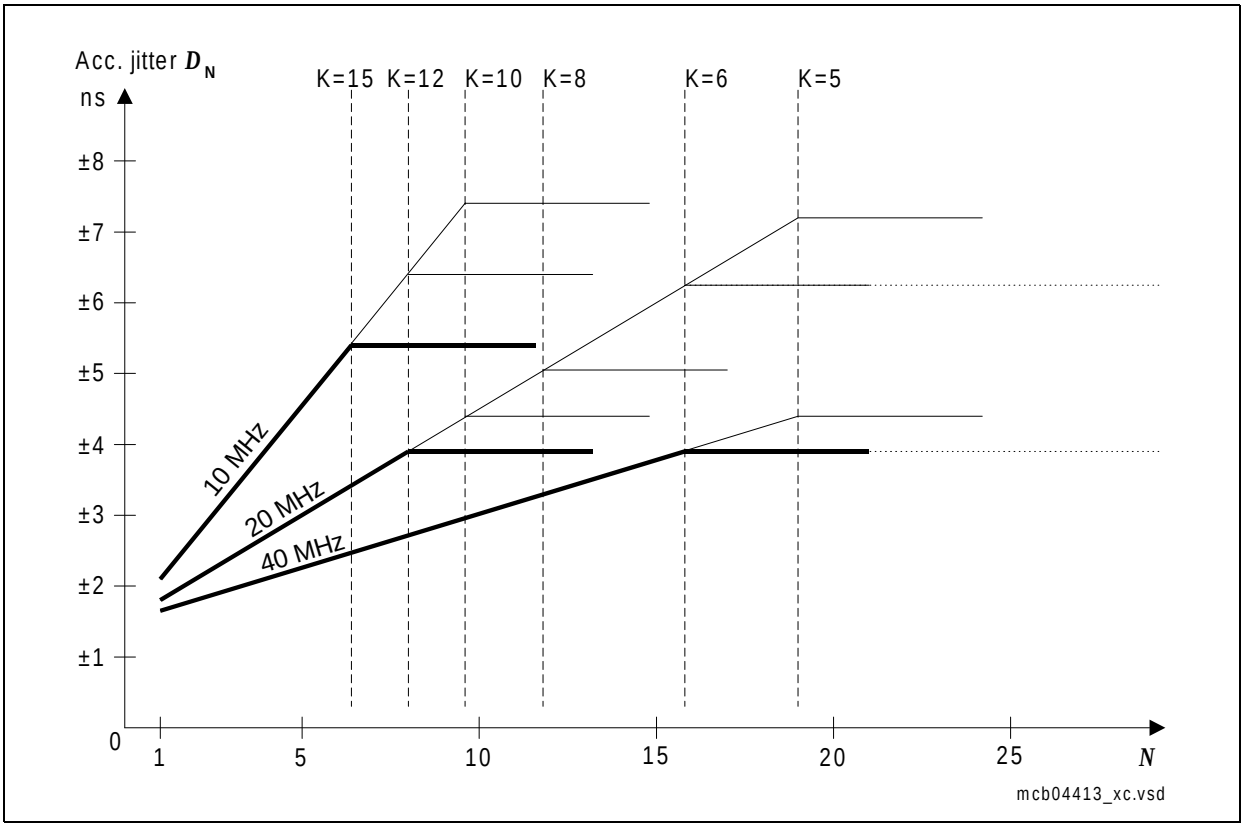

Figure 4-2 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 4-1 VCO Bands for PLL Operation

PLL_CLC.VCOSEL	VCO Frequency Range	Base Frequency Range [1]
00	400 ... 500 MHz	250 ... 320 MHz
01	500 ... 600 MHz	300 ... 400 MHz
10	600 ... 700 MHz	350 ... 480 MHz
11	Reserved [2]	

[1] Base Frequency Range is the free running operation frequency of the PLL, when no input clock is available.

[2] This option cannot be used.

4.3.4 Input Clock Timing

(Operating Conditions apply)

Parameter		Symbol	Limits		Unit
			min	max	
Oscillator clock frequency	with PLL	f_{OSC} SR	4	25	MHz
Input clock frequency driving at XTAL1	with PLL	f_{OSCDD} SR	-	40	MHz
Input Clock Duty Cycle (t_1 /t_2)		SR	45	55	%

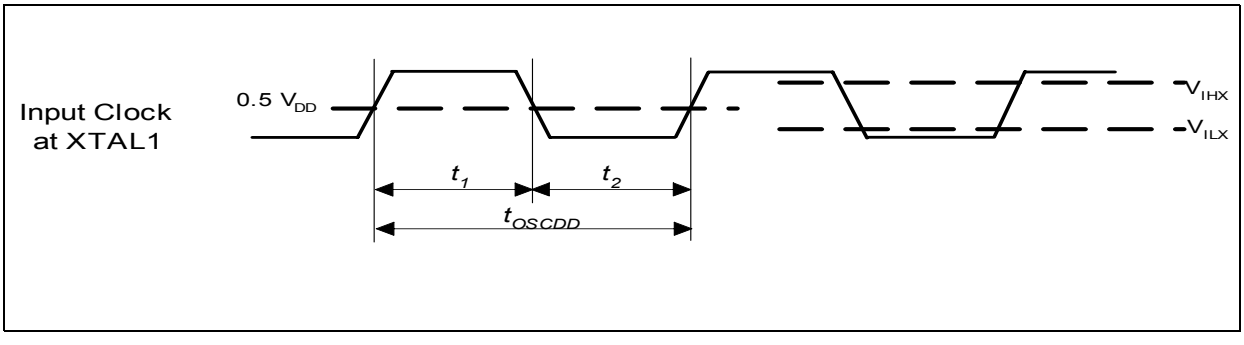

Figure 4-4 Input Clock Timing

4.3.5 Port Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol	Limits		Unit
		min	max	
Port data valid from TRCLK [1] up to 120 MHz[2]	t_1 CC	–	13	ns

[1] Port data is output with respect to the FPI clock. The TRCLK is used as a reference here since the FPI clock is not available as an external pin and TRCLK is same frequency as CPU clock. Port lines maintain their states for at least 2 CPU clocks.

[2] 120 MHz is verified by design/characterization.

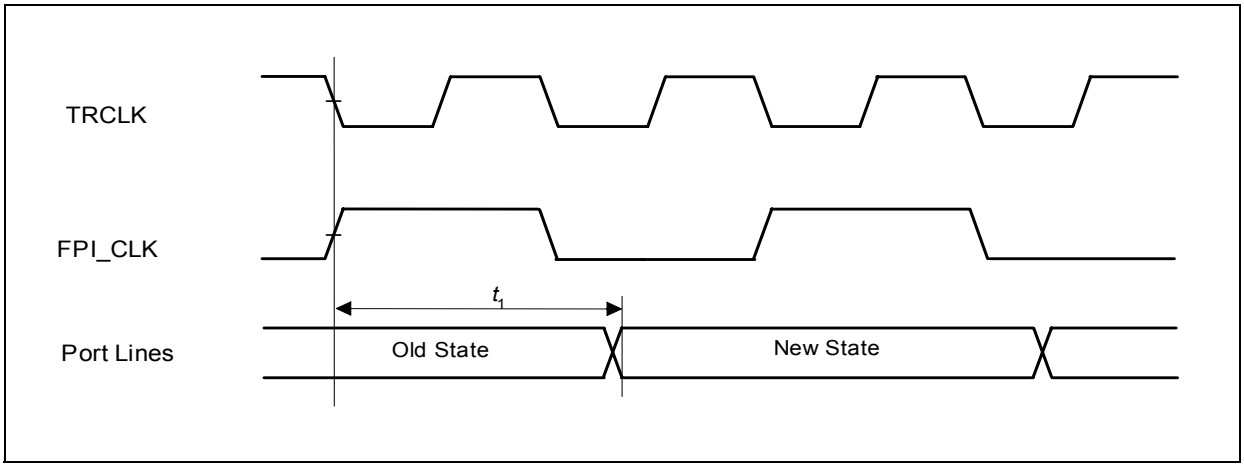

Figure 4-5 Port Timing

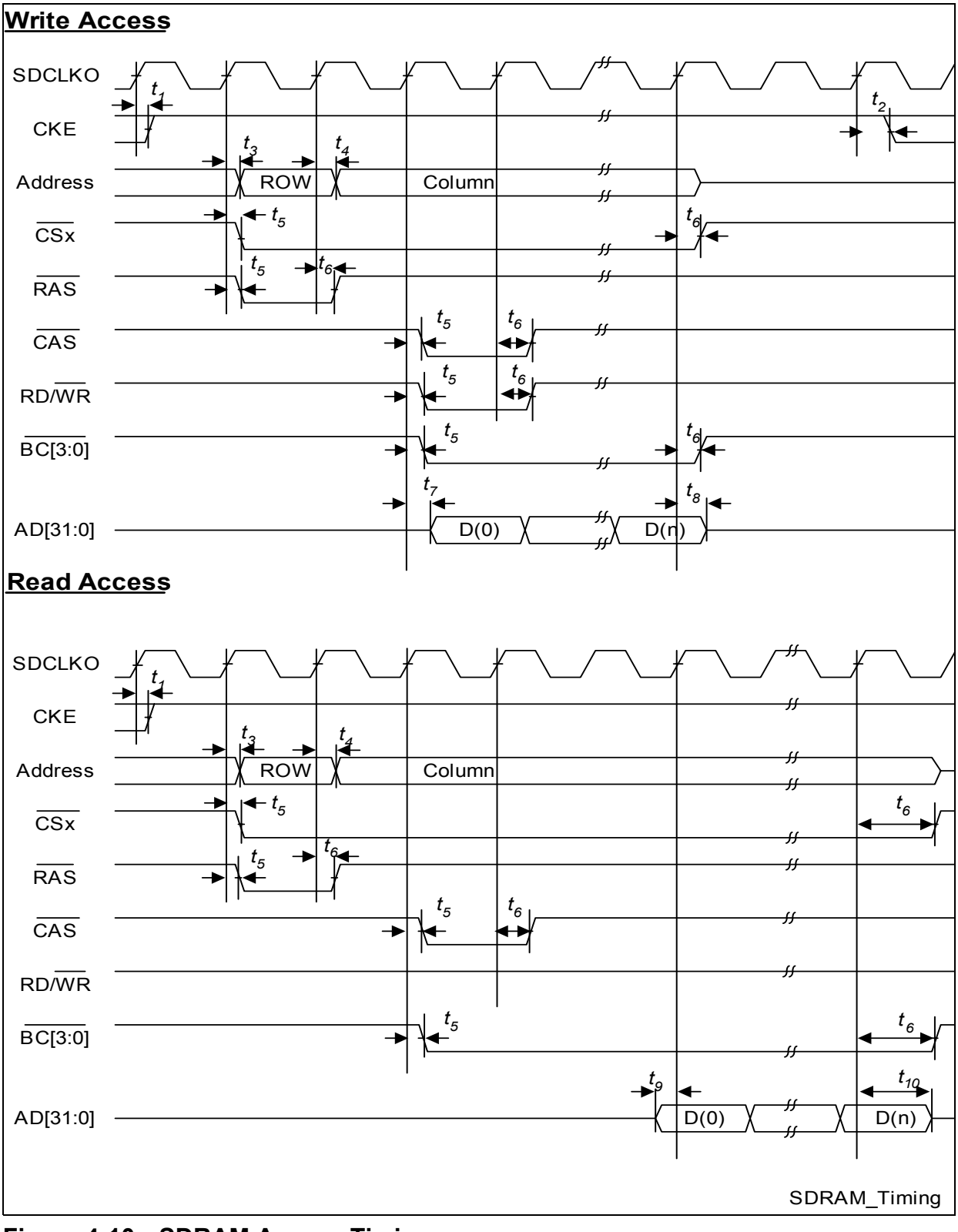

Figure 4-10 SDRAM Access Timing