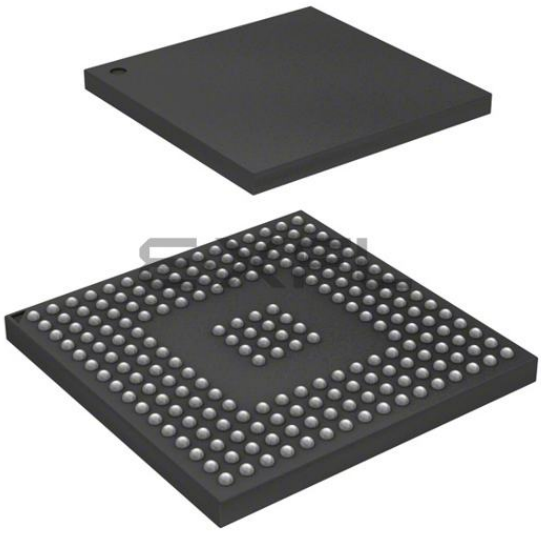

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1100-l150eb-bb

TC1100

32-Bit Single-Chip Microcontroller

Advance Information

Microcontrollers

Never stop thinking.

TC1100 Data Sheet
Advance Information
Revision History: 2005-02 V1.0

Previous Version: none

Page	Subjects (major changes since last revision)

Controller Area Network (CAN): License of Robert Bosch GmbH

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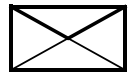

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P1		I/O		**Port 1** Port 1 serves as 16-bit bi-directional general purpose I/O port which can be used for input/output for OCDS L2, SSC0/1, EBU and SCU.	
P1.0	D11	I	PUC	SWCFG0	Software configuration 0
		O		OCDSA_0	OCDS L2 Debug Line A0
P1.1	C12	I	PUC	SWCFG1	Software configuration 1
		O		OCDSA_1	OCDS L2 Debug Line A1
P1.2	D12	I	PUC	SWCFG2	Software configuration 2
		O		OCDSA_2	OCDS L2 Debug Line A2
P1.3	B12	I	PUC	SWCFG3	Software configuration 3
		O		OCDSA_3	OCDS L2 Debug Line A3
P1.4	C11	I	PUC	SWCFG4	Software configuration 4
		O		OCDSA_4	OCDS L2 Debug Line A4
P1.5	C13	I	PUC	SWCFG5	Software configuration 5
		O		OCDSA_5	OCDS L2 Debug Line A5
P1.6	A12	I	PUC	SWCFG6	Software configuration 6
		O		OCDSA_6	OCDS L2 Debug Line A6
P1.7	B13	I	PUC	SWCFG7	Software configuration 7
		O		OCDSA_7	OCDS L2 Debug Line A7
P1.8	A13	I	PUC	SWCFG8	Software configuration 8
		O		OCDSA_8	OCDS L2 Debug Line A8
P1.9	A14	I	PUC	SWCFG9	Software configuration 9
		O		OCDSA_9	OCDS L2 Debug Line A9
P1.10	B14	I	PUC	SWCFG10	Software configuration 10
		O		OCDSA_10	OCDS L2 Debug Line A10
P1.11	C14	I	PUC	SWCFG11	Software configuration 11
		O		OCDSA_11	OCDS L2 Debug Line A1
		O		SLSO0_1	SSC0 Slave Select output 1
P1.12	F13	I	PUC	SWCFG12	Software configuration 12
		O		OCDSA_12	OCDS L2 Debug Line A12
		O		SLSO1_1	SSC1 Slave Select output 1
P1.13	E14	I	PUC	SWCFG13	Software configuration 13
		O		OCDSA_13	OCDS L2 Debug Line A13
		O		SLSO0_2	SSC0 Slave Select output 2
P1.14	D14	O	PUC	SLSO1_2	SSC1 Slave Select output 2
		I		SWCFG14	Software configuration 14
		O		OCDSA_14	OCDS L2 Debug Line A14

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
				EBU Address/Data Bus Input/Output Lines
AD0	C8	I/O	PUC	EBU Address/Data Bus Line 0
AD1	C7	I/O	PUC	EBU Address/Data Bus Line 1
AD2	B6	I/O	PUC	EBU Address/Data Bus Line 2
AD3	C6	I/O	PUC	EBU Address/Data Bus Line 3
AD4	C5	I/O	PUC	EBU Address/Data Bus Line 4
AD5	A3	I/O	PUC	EBU Address/Data Bus Line 5
AD6	A2	I/O	PUC	EBU Address/Data Bus Line 6
AD7	C3	I/O	PUC	EBU Address/Data Bus Line 7
AD8	C2	I/O	PUC	EBU Address/Data Bus Line 8
AD9	D2	I/O	PUC	EBU Address/Data Bus Line 9
AD10	F1	I/O	PUC	EBU Address/Data Bus Line 10
AD11	E3	I/O	PUC	EBU Address/Data Bus Line 11
AD12	F3	I/O	PUC	EBU Address/Data Bus Line 12
AD13	G1	I/O	PUC	EBU Address/Data Bus Line 13
AD14	H2	I/O	PUC	EBU Address/Data Bus Line 14
AD15	G3	I/O	PUC	EBU Address/Data Bus Line 15
AD16	D7	I/O	PUC	EBU Address/Data Bus Line 16
AD17	B5	I/O	PUC	EBU Address/Data Bus Line 17
AD18	A4	I/O	PUC	EBU Address/Data Bus Line 18
AD19	B4	I/O	PUC	EBU Address/Data Bus Line 19
AD20	C4	I/O	PUC	EBU Address/Data Bus Line 20
AD21	B3	I/O	PUC	EBU Address/Data Bus Line 21
AD22	B2	I/O	PUC	EBU Address/Data Bus Line 22
AD23	B1	I/O	PUC	EBU Address/Data Bus Line 23
AD24	C1	I/O	PUC	EBU Address/Data Bus Line 24
AD25	D3	I/O	PUC	EBU Address/Data Bus Line 25
AD26	E2	I/O	PUC	EBU Address/Data Bus Line 26
AD27	F2	I/O	PUC	EBU Address/Data Bus Line 27
AD28	F4	I/O	PUC	EBU Address/Data Bus Line 28
AD29	G4	I/O	PUC	EBU Address/Data Bus Line 29
AD30	H3	I/O	PUC	EBU Address/Data Bus Line 30
AD31	G2	I/O	PUC	EBU Address/Data Bus Line 31
$\overline{\text{BC0}}$	A5	O	PUC	**EBU Byte Control Line 0**
$\overline{\text{BC1}}$	A6	O	PUC	**EBU Byte Control Line 1**
$\overline{\text{BC2}}$	B7	O	PUC	**EBU Byte Control Line 2**
BC3	A7	O	PUC	**EBU Byte Control Line 3**

3.3 Memory Protection System

The TC1100 memory protection system specifies the addressable range and read/write permissions of memory segments available to the currently executing task. The memory protection system controls the position and range of addressable segments in memory. It also controls the kinds of read and write operations allowed within addressable memory segments. Any illegal memory access is detected by the memory protection hardware, which then invokes the appropriate Trap Service Routine (TSR) to handle the error. Thus, the memory protection system protects critical system functions against both software and hardware errors. The memory protection hardware can also generate signals to the Debug Unit to facilitate tracing illegal memory accesses.

In TC1100, TriCore™ supports two address spaces: the virtual address space and the physical address space. Both address space are 4 Gbytes in size and divided into 16 segments with each segment being 256 Mbytes. The upper 4 bits of the 32-bit address are used to identify the segment. Virtual segments are numbered 0 - 15. But a virtual address is always translated into a physical address before accessing memory. The virtual address is translated into a physical address using one of two translation mechanisms: (a) direct translation, and (b) Page Table Entry (PTE) based translation. If the virtual address belongs to the upper half of the virtual address space then the virtual address is directly used as the physical address (direct translation). If the virtual address belongs to the lower half of the address space, then the virtual address is used directly as the physical address if the processor is operating in physical mode (direct translation) or translated using a Page Table Entry if the processor is operating in virtual mode (PTE translation). These are managed by Memory Management Unit (MMU).

Memory protection is enforced using separate mechanisms for the two translation paths.

3.3.1 Protection for Direct translation

Memory protection for addresses that undergo direct translation is enforced using the range based protection that has been used in the previous generation of the TriCore™ architecture. The range based protection mechanism provides support for protecting memory ranges from unauthorized read, write, or instruction fetch accesses. The TriCore™ architecture provides up to four protection register sets with the PSW.PRS field controlling the selection of the protection register set. Because the TC1100 uses a Harvard-style memory architecture, each Memory Protection Register Set is broken down into a Data Protection Register Set and a Code Protection Register Set. Each Data Protection Register Set can specify up to four address ranges to receive particular protection modes. Each Code Protection Register Set can specify up to two address ranges to receive particular protection modes.

Each of the Data Protection Register Sets and Code Protection Register Sets determines the range and protection modes for a separate memory area. Each contains register pairs which determine the address range (the Data Segment Protection Registers and Code Segment Protection Registers) and one register (Data Protection

Features:

The FPI Bus is designed with the requirements of high-performance systems in mind. The features are:

- Core independent
- Multimaster capability (up to 16 masters)
- Demultiplexed operation
- Clock synchronous
- Peak transfer rate of up to 800 Mbytes/sec (@ 100 MHz bus clock)
- Address and data bus scalable (address bus up to 32 bits, data bus up to 64 bits)
- 8-/16-/32- and 64-bit data transfers
- Broad range of transfer types from single to multiple data transfers
- Split transaction support for agents with long response time
- Burst transfer capability
- EMI and power consumption minimized

3.4.3 LFI

The LMB-to-FPI Interface (LFI) block provides the circuitry to interface (bridge) the FPI bus and the Local Memory Bus (LMB).

LFI Features:

- Full support for bus transactions found within current TriCore™ 1.3 based systems:
  - Single 8/16/32-bit Write/Read transfers from FPI to LMB
  - Single 8/16/32/64-bit Write/Read transfers from LMB to FPI
  - Read-Modify-Write transfers of 8/16/32-bit in both directions
  - Burst transactions of 2, 4 or 8 data beats from the FPI to the LMB
  - Burst transactions of 2 or 4 data beats from the LMB to the FPI
- Address decoding and translation as required by TriCore™ 1.3 implementation
- FPI master interface supports full pipelining on FPI bus
- LMB master interface supports pipelining on LMB within the scope of the LMB specification
- FPI master interface can act as default master on FPI bus
- Programmable support for split LMB to FPI read transactions
- Retry generation on both FPI and LMB buses
- Full support for abort, retry, error and FPI timeout conditions
- Flexible LMB/FPI clock ratio support including dynamic clock switching support
- LFI core clock may be shut down when no transactions are being issued to LFI from either bus and the LFI has no transactions in progress, thus saving power.

The EBU is used primarily for any Local Memory Bus (LMB) master accessing external memories. The EBU controls all transactions required for this operation and in particular handles the arbitration between the internal EBU master and the external EBU master.

The types of external devices/bus modes controlled by the EBU are:

- Intel-style peripherals (separate $\overline{RD}$ and $\overline{WR}$ signals)
- ROMs, EPROMs
- Static RAMs
- PC100 and PC133 SDRAMs (Burst Read/Write Capacity/Multi-Bank/Page support)
- Specific types of Burst Mode Flash devices
- Special support for external emulator/debug hardware

Features:

- Supports 64-bit Local Memory Bus (LMB)
- Supports external bus frequency: internal LMB frequency = 1:1 or 1:2
- Provides highly programmable access parameters
- Supports Intel-style peripherals/devices
- Supports PC100 and PC133 (runs in maximum 120 MHz) SDRAM (burst access, multibanking, precharge, refresh)
- Supports 16- and 32-bit SDRAM data bus and 64-,128-, and 256-Mbit devices
- Supports Burst Flash devices
- Supports Multiplexed access (address and data on the same bus) when PC100 and PC133 SDRAM are not presented on the external bus
- Supports data buffering: Code Prefetch Buffer, Read/Write Buffer
- External master arbitration compatible to C166 and other TriCore™ devices
- Provides 4 programmable address regions (1 dedicated for emulator)
- Provides a CSGLB signal, bit programmable to combine one or more $\overline{CS}$ lines for buffer control
- Provides $\overline{RMW}$ signal reflecting read-modify-write action
- Supports Little Endian byte ordering
- Provides signal for controlling data flow of slow-memory buffer

The basic structure and external interconnections of the DMA are shown in **Figure 3-2**.

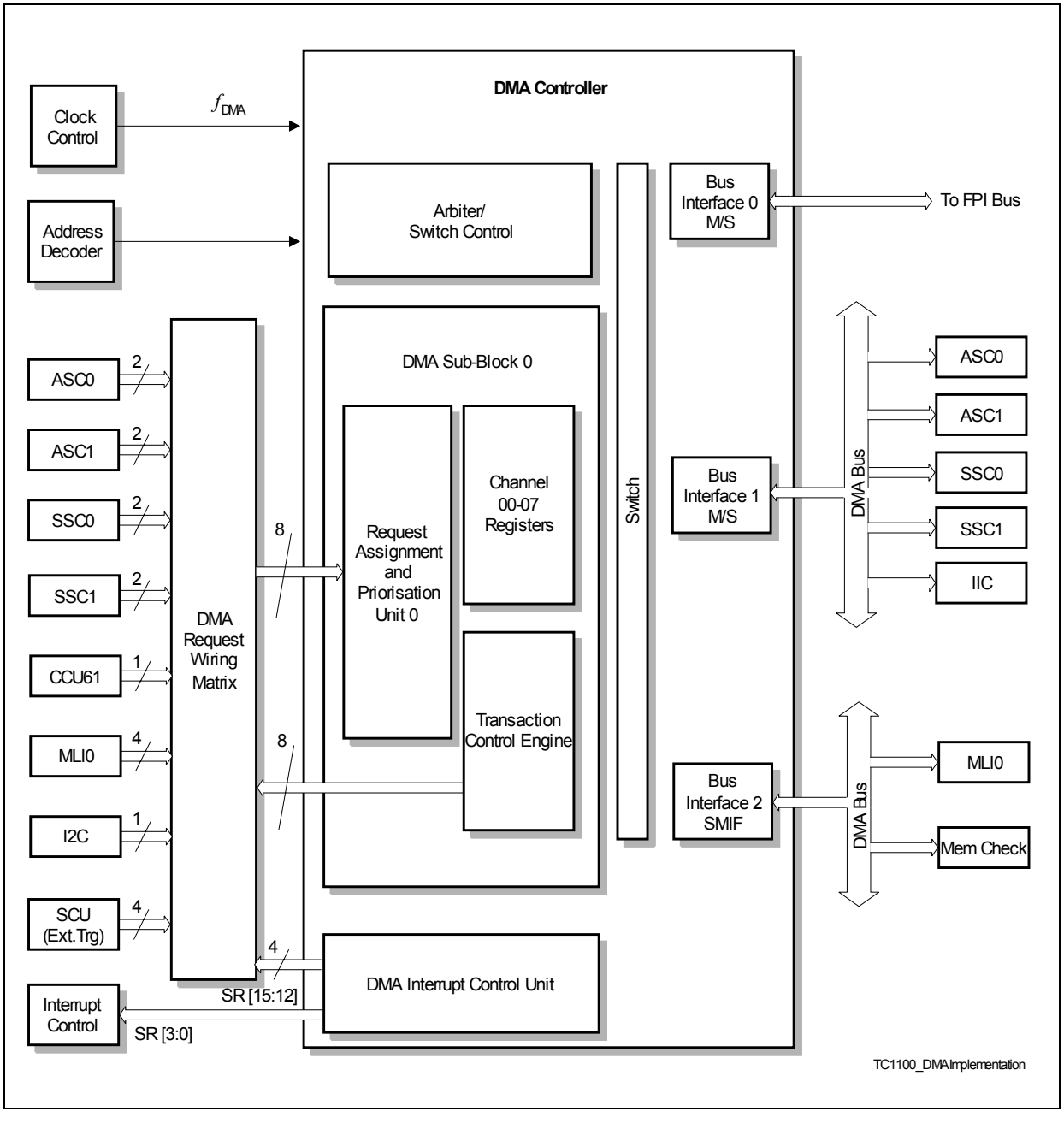

Figure 3-2 DMA Controller Structure and Interconnections

3.9 Asynchronous/Synchronous Serial Interface (ASC)

Figure 3-5 shows a global view of the functional blocks of two Asynchronous/ Synchronous Serial interfaces (ASC0 and ASC1).

Each ASC module (ASC0/ASC1) communicates with the external world via one pair of I/O lines. The RXD line is the receive data input signal (in synchronous mode also output). TXD is the transmit output signal. Clock control, address decoding, and interrupt service request control are managed outside the ASC module kernel.

The Asynchronous/Synchronous Serial interfaces provide serial communication between the TC1100 and other microcontrollers, microprocessors or external peripherals.

Each ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In synchronous mode, data is transmitted or received synchronous to a shift clock which is generated by the ASC internally. In asynchronous mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud-rate generator provides the ASC with a separate serial clock signal that can be accurately adjusted by a prescaler implemented as a fractional divider.

3.10 High-Speed Synchronous Serial Interface (SSC)

Figure 3-6 shows a global view of the functional blocks of two High-Speed Synchronous Serial interfaces (SSC0 and SSC1).

Each SSC supports full-duplex and half-duplex serial synchronous communication up to 37.5 MBaud (@ 75 MHz module clock) with receive and transmit FIFO support. The serial clock signal can be generated by the SSC itself (master mode) or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. Eight slave select inputs are available for slave mode operation. Eight programmable slave select outputs (chip selects) are supported in master mode.

Features:

- Master and slave mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baud rate generation minimum at 572.2 Baud (@ 75 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Four-pin interface
- Flexible SSC pin configuration
- Up to eight slave select inputs in slave mode
- Up to eight programmable slave select outputs SLSO in master mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control
- 4-stage receive FIFO (RXFIFO) and 4-stage transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 2- to 16-bit FIFO data width
  - Programmable receive/transmit interrupt trigger level
  - Receive and transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation

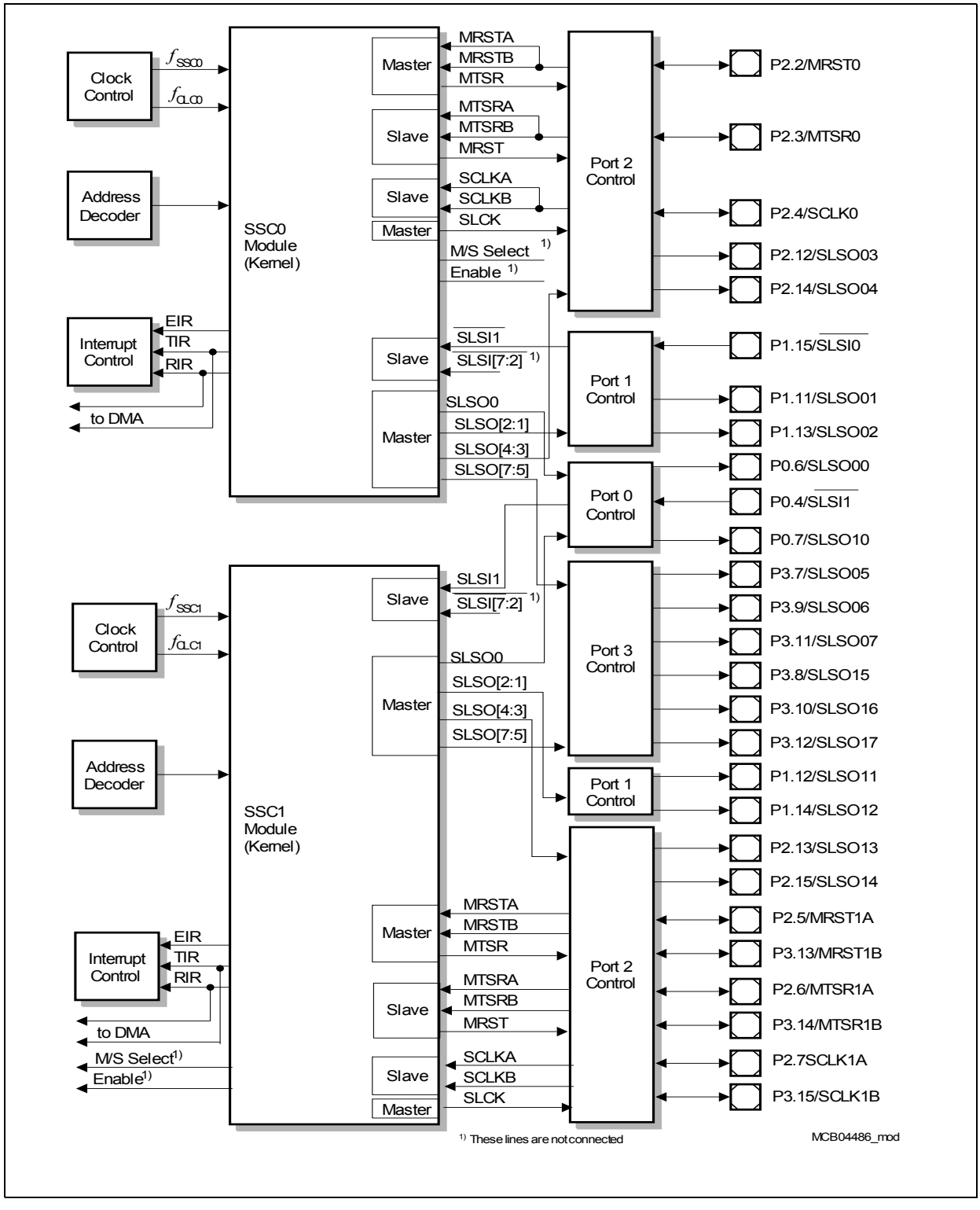

Figure 3-6 General Block Diagram of the SSC Interfaces

3.12 Micro Link Serial Bus Interface (MLI)

Figure 3-8 shows a global view of the functional blocks of the Micro Link Serial Bus Interface (MLI0).

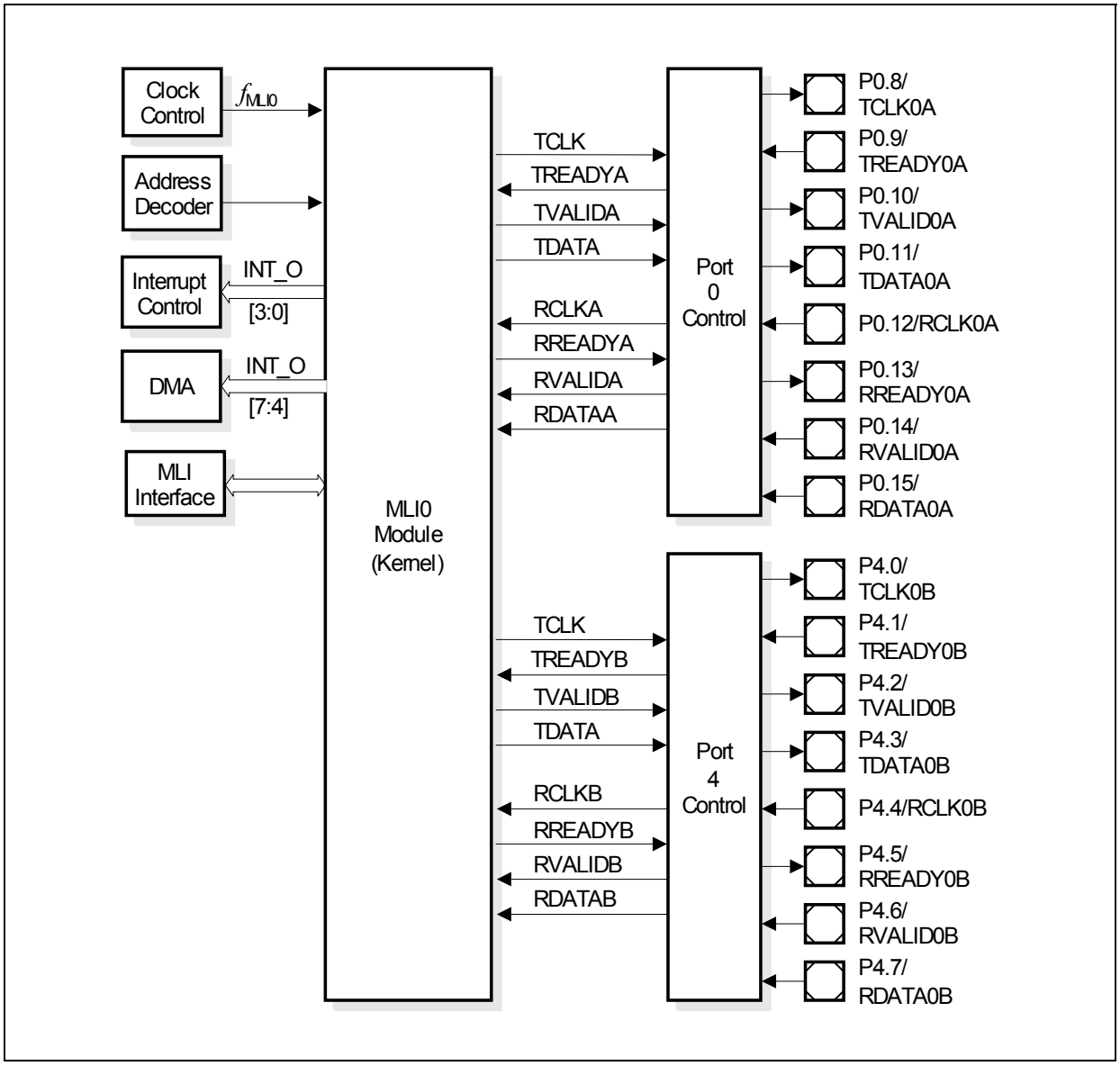

Figure 3-8 General Block Diagram of the MLI0 Interface

The Micro Link Serial Bus Interface is dedicated to the serial communication between the other Infineon 32-bit controllers with MLI. The communication is intended to be fast due to an address translation system, and it is not necessary to have any special program in the second controller.

3.17 System Control Unit

The System Control Unit (SCU) of the TC1100 handles the system control tasks. All of these system functions are tightly coupled; thus, they are conveniently handled by one unit, the SCU. The system tasks of the SCU are:

- Clock Control
  - Clock generation
  - Oscillator and PLL control
- Reset and Boot Control
  - Generation of all internal reset signals
  - Generation of external hardware and software reset signal
- Power Management Control
  - Enabling of several power management modes
- Configuration input sampling
- FPU interrupts
- External Request Unit
- Parity Error Control
- Fault SRAM Fuse Box
- CSCOMB Control
- EBU Pull-Up Control
- NMI Control and Status
- DMA Request Signal Selection

3.19 Power Management System

The TC1100 power management system allows software to configure the various processing units to adjust automatically in order to draw the minimum necessary power for the application.

There are four power management modes:

- Run Mode
- Idle Mode
- Sleep Mode
- Deep Sleep Mode

Table 3-4 describes the features of the power management modes.

Table 3-4 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to run mode. Idle mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the NMI pin, or any enabled interrupt event will return the system to run mode.
Sleep	The system clock continues to be distributed only to those peripherals programmed to operate in sleep mode. The other peripheral modules will be shut down by the suspend signal. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the NMI pin, or a reset event will return the system to run mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.
Deep Sleep	The system clock is shut off; only an external signal will restart the system. Entering this state requires an orderly shut-down controlled by the Power Management State Machine (PMSM).

Besides these explicit software-controlled power-saving modes, special attention has been paid in the TC1100 to automatic power-saving in operating units that are currently not required or idle. In this case, they are shut off automatically until their operation is required again.

3.24 Identification Register Values

Table 3-6 TC1100 Identification Registers

Short Name	Address	Value
SCU_ID	F000 0008$_H$	002C C001$_H$
MANID	F000 0070$_H$	0000 1820$_H$
CHIPID	F000 0074$_H$	0000 8C01$_H$
RTID	F000 0078$_H$	0000 0000$_H$
SBCU_ID	F000 0108$_H$	0000 6A0A$_H$
STM_ID	F000 0208$_H$	0000 C005$_H$
CBS_JDPID	F000 0308$_H$	0000 6307$_H$
GPTU_ID	F000 0608$_H$	0001 C002$_H$
CCU61_ID	F000 2108$_H$	0042 C004$_H$
DMA_ID	F000 3C08$_H$	001A C011$_H$
SSC0_ID	F010 0108$_H$	0000 4530$_H$
SSC1_ID	F010 0208$_H$	0000 4530$_H$
ASC0_ID	F010 0308$_H$	0000 44E2$_H$
ASC1_ID	F010 0408$_H$	0000 44E2$_H$
IIC_ID	F010 0608$_H$	0000 4604$_H$
MLI0_ID	F010 C008$_H$	0025 C004$_H$
MCHK_ID	F010 C208$_H$	001B C001$_H$
CPS_ID	F7E0 FF08$_H$	0015 C006$_H$
MMU_ID	F7E1 8008$_H$	0009 C002$_H$
CPU_ID	F7E1 FE18$_H$	000A C005$_H$
EBU_ID	F800 0008$_H$	0014 C004$_H$
DMU_ID	F800 0408$_H$	002D C001$_H$
DMI_ID	F87F FC08$_H$	0008 C004$_H$
PMI_ID	F87F FD08$_H$	000B C004$_H$
LBCU_ID	F87F FE08$_H$	000F C005$_H$
LFI_ID	F87F FF08$_H$	000C C005$_H$

4.1.2 Absolute Maximum Rating

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	-40	85	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	125	°C	under bias
Voltage at 1.5 V power supply pins with respect to V_{SS} [1]	V_{DD}	-0.5	1.7	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS} [2]	V_{DDP}	-0.5	4.0	V	–
Voltage on any pin with respect to V_{SS} [2]	V_{IN}	-0.5	4.0	V	–
Input current on any pin during overload condition	I_{IN}	-10	10	mA	–
Absolute sum of all input currents during overload condition	ΣI_{IN}	–	|100|	mA	–
CPU & LMB Bus Frequency	f_{SYS}	–	150	MHz	–
FPI Bus Frequency	f_{FPI}	–	100	MHz	–

1) Applicable for V_{DD} and V_{DDOSC}.

2) Applicable for V_{DDP} and V_{DDOSC3}. The maximum voltage difference must not exceed 4.0 V in any case (i.e. Supply Voltage = 4.0 V and Input Voltage = -0.5 V is not allowed).

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

4.3.2 PLL Parameters

When PLL operation is configured (*PLL_CLC.LOCK = 1*), the on-chip phase locked loop is enabled and provides the master clock. The PLL multiplies the input frequency by the factor **F** ($f_{MC} = f_{OSC} \times$ **F**) which results from the input divider, the multiplication factor (N Factor), and the output divider (**F** = *NDIV+1 / (PDIV+1 × KDIV+1)*). The PLL circuit synchronizes the master clock to the input clock. This synchronization is done smoothly, i.e. the master clock frequency does not change abruptly.

Due to this adaptation to the input clock, the frequency of f_{MC} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{MC} which also affects the duration of individual TCMs.

The timing listed in the AC Characteristics refers to TCPs. Because f_{CPU} is derived from f_{MC}, the timing must be calculated using the minimum TCP possible under the respective circumstances.
The actual minimum value for TCP depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency in order to correspond to the applied input frequency (crystal or oscillator), the relative deviation for periods of more than one TCP is lower than for one single TCP (see formula and **Figure 4-2**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baud rates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler (K = *KDIV*+1) to generate the master clock signal f_{MC}. Therefore, the number of VCO cycles can be represented as $K \times N$, where N is the number of consecutive f_{MC} cycles (TCM).

For a period of $N \times$ TCM, the accumulated PLL jitter is defined by the corresponding deviation D_N:

D_N [ns] = $\pm(1.5 + 6.32 \times N / f_{MC})$; f_{MC} in [MHz], N = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: $D_3 = \pm(1.5 + 6.32 \times 3 / 20) = 2.448$ ns.

This formula is applicable for $K \times N < 95$. For longer periods, the $K \times N = 95$ value can be used. This steady value can be approximated by: D_{Nmax} [ns] = $\pm(1.5 + 600 / (K \times f_{MC}))$.

4.3.6 Timing for JTAG Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
TCK clock period	t_{TCK}	SR	50	–	ns
TCK high time	t_1	SR	10	–	ns
TCK low time	t_2	SR	29	–	ns
TCK clock rise time	t_3	SR	–	0.4	ns
TCK clock fall time	t_4	SR	–	0.4	ns

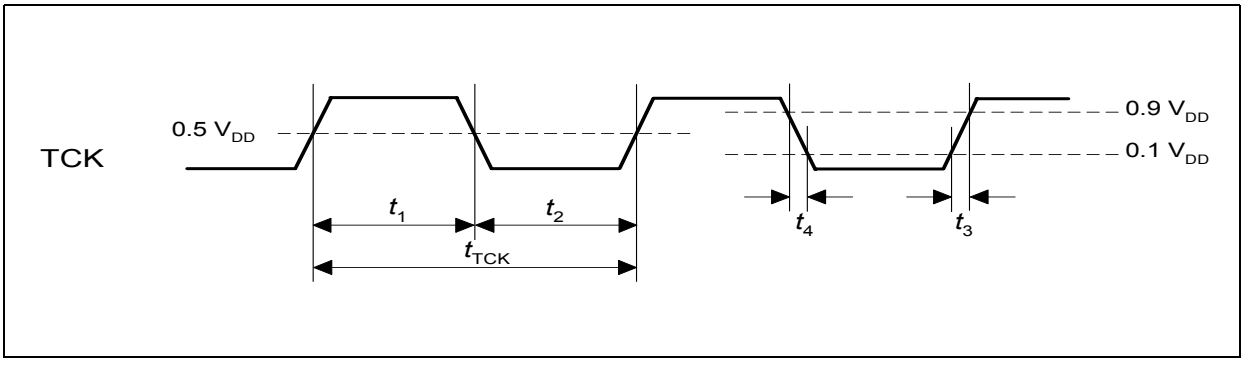

Figure 4-6 TCK Clock Timing

4.3.8 EBU Timings

4.3.8.1 SDCLKO Output Clock Timing

(Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limits[1]		Limits[2]		Unit
			min	max	min	max	
SDCLKO period	t_1	CC	10	–	8.3	–	ns
SDCLKO high time	t_2	CC	3	–	2.5	–	ns
SDCLKO low time	t_3	CC	3	–	2.5	–	ns
SDCLKO rise time	t_4	CC	–	2.5	–	2.5	ns
SDCLKO fall time	t_5	CC	–	2.5	–	2.5	ns

1) The parameters are applicable for PC100 SDRAM access and the maximum SDCLKO is up to 100 MHz.

2) The parameters are applicable for PC133 SDRAM access and the maximum SDCLKO is up to 120 MHz.

4.3.8.2 BFCLKO Output Clock Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit [1]		Limit [2]		Unit
			min	max	min	max	
Clock period	t_1	CC	20	–	16.7	–	ns
BFCLKO high time	t_2	CC	6.6	–	7.5	–	ns
BFCLKO low time	t_3	CC	6.6	–	7.5	–	ns
BFCLKO rise time	t_4	CC	–	3.5	–	3.5	ns
BFCLKO fall time	t_5	CC	–	2.5	–	2.5	ns

1) The CPU runs at 150 MHz and the Burst Flash runs at divided by 3 clock.

2) The CPU runs at 120 MHz and the Burst Flash runs at divided by 2 clock.

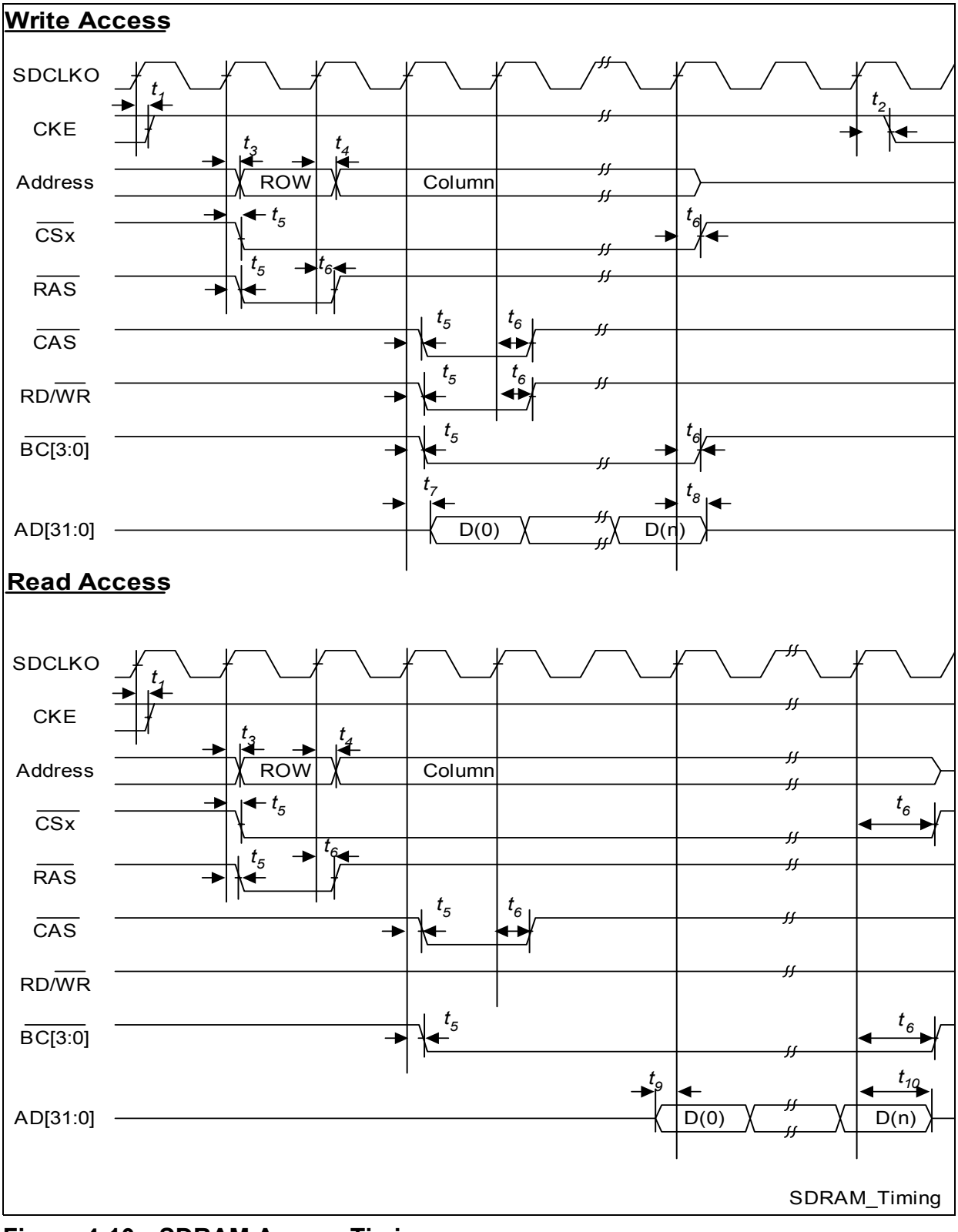

Figure 4-10 SDRAM Access Timing