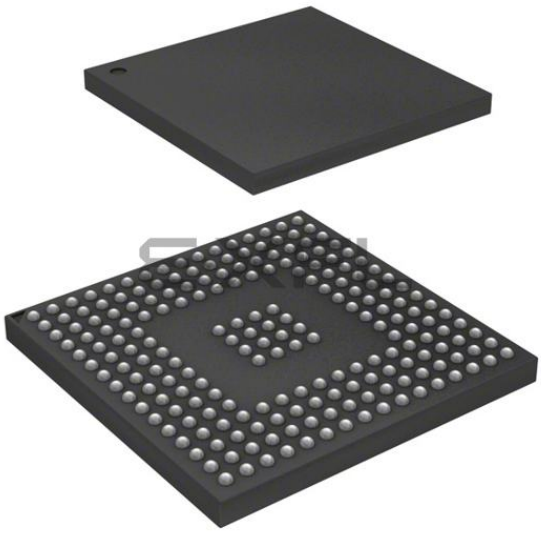
Infineon Technologies - SAF-TC1100-L150EB-G BB Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1100-l150eb-g-bb

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TC1100 Data Sheet
Advance Information
Revision History: 2005-02 V1.0

Previous Version: none

Page	Subjects (major changes since last revision)

Controller Area Network (CAN): License of Robert Bosch GmbH

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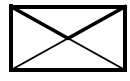

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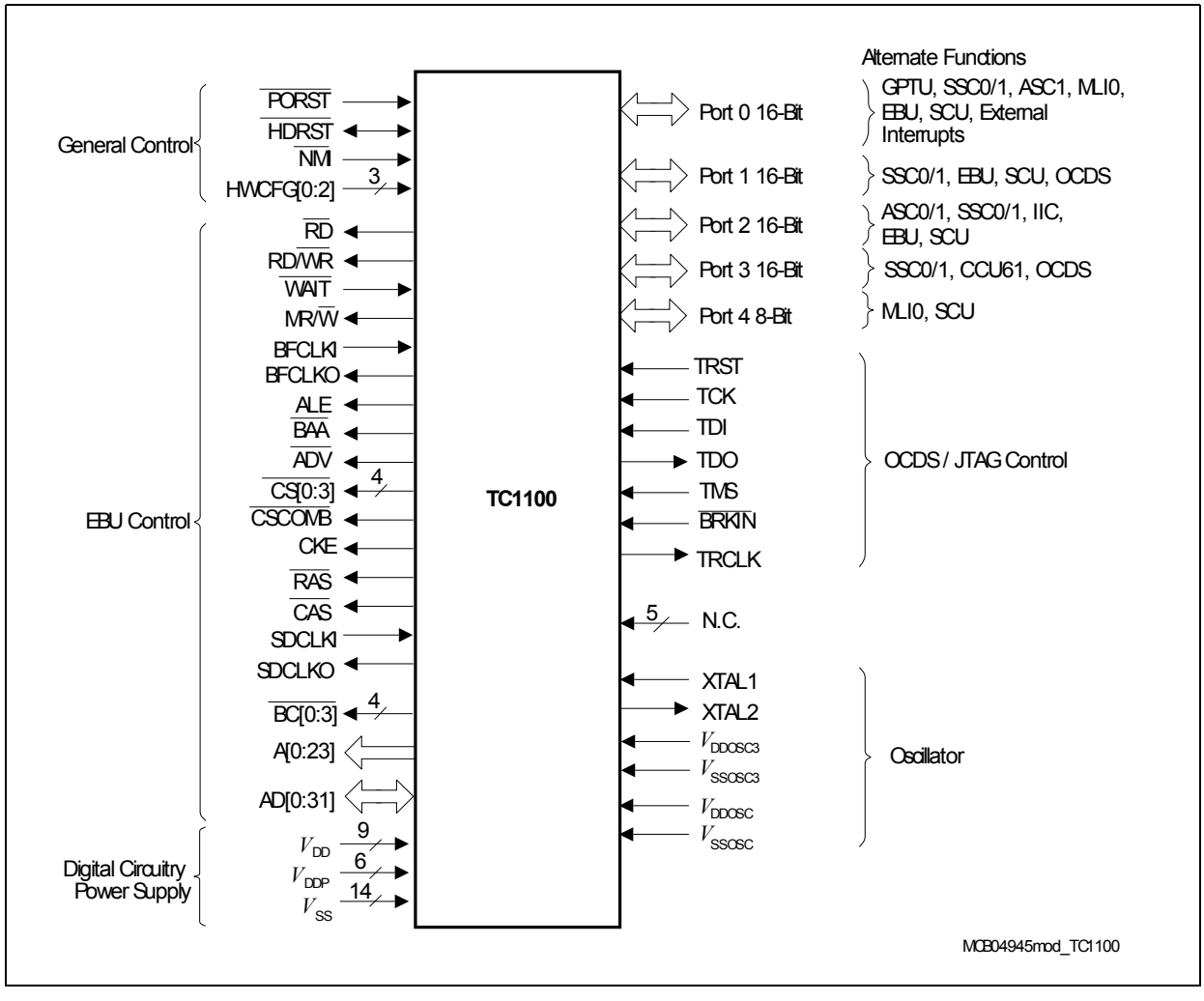

Figure 2-2 TC1100 Logic Symbol

Table 3-1 TC1100 Block Address Map (cont'd)

Seg-ment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
13	D000 0000$_H$ – D000 6FFF$_H$	28 KB	DMI Local Data RAM (LDRAM)	DMI local	via LMB	non-cached
	D000 7000$_H$ – D3FF FFFF$_H$	~ 64 MB	Reserved			
	D400 0000$_H$ – D400 7FFF$_H$	32 KB	PMI Local Code Scratch Pad RAM (SPRAM)	via LMB	PMI local	
	D400 8000$_H$ – D7FF FFFF$_H$	~64 MB	Reserved			
	D800 0000$_H$ – DDFF FFFF$_H$	96 MB	External Memory Space	via LMB	via LMB	
	DE00 0000$_H$ – DEFF FFFF$_H$	16 MB	Emulator Memory Space			
	DF00 0000$_H$ – DFFF BFFF$_H$	~16 MB	Reserved	–	–	
	DFFF C000$_H$ – DFFF FFFF$_H$	16 KB	Boot ROM Space	via FPI	via FPI	
14	E000 0000$_H$ – E7FF FFFF$_H$	128 MB	External Memory Space	via LMB	via LMB	
	E800 0000$_H$ – E83F FFFF$_H$	4 MB	Reserved for mapped space for lower 4 Mbytes of Local Memory in Segment 12 (Transformed by LFI bridge to C000 0000$_H$ – C03F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E840 0000$_H$ – E84F FFFF$_H$	1 MB	Reserved for mapped space for lower 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D000 0000$_H$ – D00F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E850 0000$_H$ – E85F FFFF$_H$	1 MB	Reserved for mapped space for 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D400 0000$_H$ – D40F FFFF$_H$)			

3.6 Direct Memory Access (DMA)

The Direct Memory Access Controller executes DMA transactions from a source address location to a destination address location, without intervention of the CPU. One DMA transaction is controlled by one DMA channel. Each DMA channel has assigned its own channel register set. The total of 8 channels are provided by one DMA sub-block.

The DMA module is connected to 3 bus interfaces in TC1100, the Flexible Peripheral Interconnect Bus (FPI), the DMA Bus and the Micro Link Bus. It can do transfers on each of the buses as well as between the buses.

In addition, it bridges accesses from the Flexible Peripheral Interconnect Bus to the peripherals on the DMA Bus, allowing easy access to these peripherals by CPU. Clock control, address decoding, DMA request wiring, and DMA interrupt service request control are implementation specific and managed outside the DMA controller kernel.

Features:

- 8 independent DMA channels
  - Up to 8 selectable request inputs per DMA channel
  - Programmable priority of DMA channels within a DMA sub-block (2 levels)
  - Software and hardware DMA request generation
  - Hardware requests by selected peripherals and external inputs
- Programmable priority of the DMA sub-block on the bus interfaces
- Buffer capability for move actions on the buses (min. 1 move per bus is buffered)
- Individually programmable operation modes for each DMA channel
  - Single mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated
  - Programmable address modification
- Full 32-bit addressing capability of each DMA channel
  - 4-Gbyte address range
  - Support of circular buffer addressing mode
- Programmable data width of a DMA transaction: 8-bit, 16-bit, or 32-bit
- Micro Link supported
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channels is also implemented in the DMA module)
- All buses/interfaces connected to the DMA module must work at the same frequency.
- Read/write requests of the FPI Bus Side to the Remote Peripherals are bridged to the DMA Bus (only the DMA is master on the DMA bus)

3.9 Asynchronous/Synchronous Serial Interface (ASC)

Figure 3-5 shows a global view of the functional blocks of two Asynchronous/ Synchronous Serial interfaces (ASC0 and ASC1).

Each ASC module (ASC0/ASC1) communicates with the external world via one pair of I/O lines. The RXD line is the receive data input signal (in synchronous mode also output). TXD is the transmit output signal. Clock control, address decoding, and interrupt service request control are managed outside the ASC module kernel.

The Asynchronous/Synchronous Serial interfaces provide serial communication between the TC1100 and other microcontrollers, microprocessors or external peripherals.

Each ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In synchronous mode, data is transmitted or received synchronous to a shift clock which is generated by the ASC internally. In asynchronous mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud-rate generator provides the ASC with a separate serial clock signal that can be accurately adjusted by a prescaler implemented as a fractional divider.

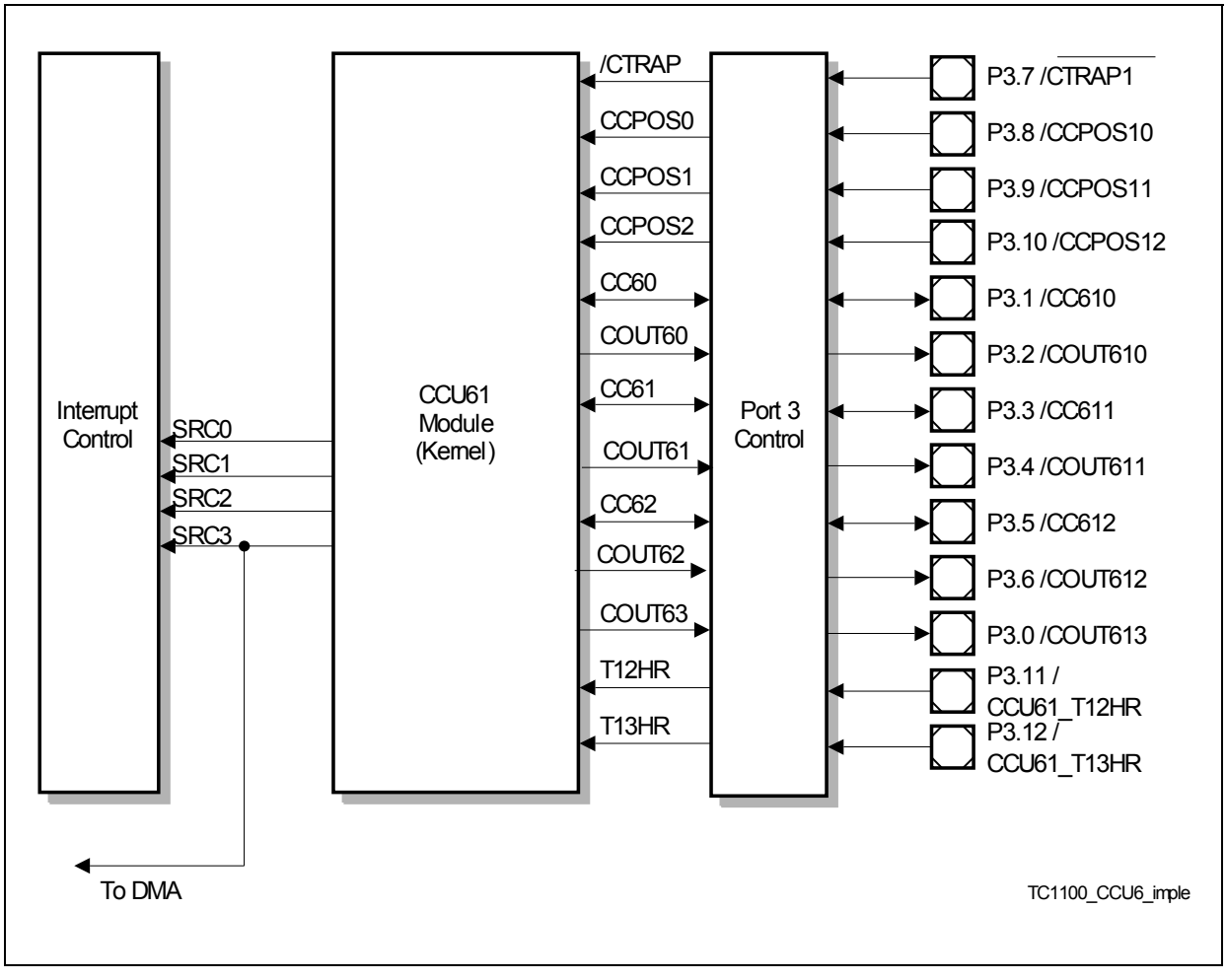

Figure 3-10 General Block Diagram of the CCU6 Interface

3.16 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC1100 in a user-specified time period. When enabled, the WDT will cause the TC1100 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1100 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard “Watchdog” function, the WDT incorporates the ENDINIT feature and monitors its modifications. A system-wide line is connected to the ENDINIT bit implemented in a WDT control register, serving as an additional write-protection for critical registers (besides supervisor mode protection). Registers protected via this line can be modified only when supervisor mode is active and bit ENDINIT = 0.

A further enhancement in the TC1100’s Watchdog Timer is its reset prewarning operation. Instead of immediately resetting the device upon detection of an error, the WDT first issues a Non-Maskable Interrupt (NMI) to the CPU before finally resetting the device at a specified time period later. This gives the CPU a chance to save system state to memory for later examination of the cause of the malfunction, thus providing an important aid in debugging.

Features:

- 16-bit Watchdog counter
- Selectable input frequency: $f_{SYS}/256$ or $f_{SYS}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for time-out and prewarning modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated password access mechanism with fixed and user-definable password fields
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled
- Double Reset Detection: If a Watchdog induced reset occurs twice without a proper access to its control register in between, a severe system malfunction is assumed and the TC1100 is held in reset until a power-on reset. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed.

- Important debugging support is provided through the reset prewarning operation by first issuing an NMI to the CPU before finally resetting the device after a certain period of time.

3.17 System Control Unit

The System Control Unit (SCU) of the TC1100 handles the system control tasks. All of these system functions are tightly coupled; thus, they are conveniently handled by one unit, the SCU. The system tasks of the SCU are:

- Clock Control
  - Clock generation
  - Oscillator and PLL control
- Reset and Boot Control
  - Generation of all internal reset signals
  - Generation of external hardware and software reset signal
- Power Management Control
  - Enabling of several power management modes
- Configuration input sampling
- FPU interrupts
- External Request Unit
- Parity Error Control
- Fault SRAM Fuse Box
- CSCOMB Control
- EBU Pull-Up Control
- NMI Control and Status
- DMA Request Signal Selection

4.1.2 Absolute Maximum Rating

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	-40	85	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	125	°C	under bias
Voltage at 1.5 V power supply pins with respect to V_{SS} [1]	V_{DD}	-0.5	1.7	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS} [2]	V_{DDP}	-0.5	4.0	V	–
Voltage on any pin with respect to V_{SS} [2]	V_{IN}	-0.5	4.0	V	–
Input current on any pin during overload condition	I_{IN}	-10	10	mA	–
Absolute sum of all input currents during overload condition	ΣI_{IN}	–	|100|	mA	–
CPU & LMB Bus Frequency	f_{SYS}	–	150	MHz	–
FPI Bus Frequency	f_{FPI}	–	100	MHz	–

1) Applicable for V_{DD} and V_{DDOSC}.

2) Applicable for V_{DDP} and V_{DDOSC3}. The maximum voltage difference must not exceed 4.0 V in any case (i.e. Supply Voltage = 4.0 V and Input Voltage = -0.5 V is not allowed).

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

4.1.3 Operating Condition

The following operating conditions must be complied with in order to ensure correct operation of the TC1100. All parameters specified in the following table refer to these operating conditions, unless otherwise indicated.

Parameter	Symbol	Limit Values		Unit	Notes Conditions
		min.	max.		
Digital supply voltage	V_{DD}	1.43	1.58	V	–
	V_{DDP}	3.14	3.47	V	–
Digital ground voltage	V_{SS}	0		V	–
Digital core supply current	I_{DD}	–	525	mA	–
Ambient temperature under bias	T_A	-40	+85	°C	–
CPU clock	f_{SYS}	–[1]	150	MHz	–
Overload current	I_{OV}	-1	1	mA	[2][3]
		-3	3		duty cycle ≤ 25%
Short circuit current	I_{SC}	-1	1	mA	[4]
		-3	3		duty cycle ≤ 25%
Absolute sum of overload + short circuit currents	$\Sigma\|I_{OV}\| + \|I_{SC}\|$	–	|50|	mA	[3]
			|100|		duty cycle ≤ 25%
Inactive device pin current (V_{DD} = V_{DDP} = 0)	I_{ID}	-1	1	mA	–
External load capacitance	C_L	–	50	pF	–
ESD strength	–	2000	–	V	Human Body Model (HBM)

[1] The TC1100 uses a static design, so the minimum operation frequency is 0 MHz. However, due to test time restriction no lower frequency boundary is tested.

[2] Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DDP}$ + 0.5 V or $V_{OV} < V_{SS}$ - 0.5 V). The absolute sum of input overload currents on all digital I/O pins may not exceed **50 mA**. The supply voltage must remain within the specified limits.

[3] Not subject to production test, verified by design/characterization.

[4] Applicable for digital inputs.

4.2.2 Oscillator Characteristics

V_{SS} = 0 V; T_A = -40°C to +125°C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Oscillator Pins					
Input low voltage at XTAL1	V_{ILX} SR	-0.3	–	V	1)
Input high voltage at XTAL1	V_{IHX} SR	–	3	V	1)
Quartz oscillation peak-peak amplitude at oscillator Input	V_{PPOSC} SR	0.6	–	V	1)
Input low voltage at XTAL1	V_{ILX} SR	-0.3	0.1	V	2)
Input high voltage at XTAL1	V_{IHX} SR	1.4	V_{DDC} + 0.3V	V	2)
Oscillator input current	I_{OSCIN}	–	25	µA	

1) Quartz mode: using a quartz crystal

2) Bypass mode: using an external clock

4.3.4 Input Clock Timing

(Operating Conditions apply)

Parameter		Symbol	Limits		Unit
			min	max	
Oscillator clock frequency	with PLL	f_{OSC} SR	4	25	MHz
Input clock frequency driving at XTAL1	with PLL	f_{OSCDD} SR	-	40	MHz
Input Clock Duty Cycle (t_1 /t_2)		SR	45	55	%

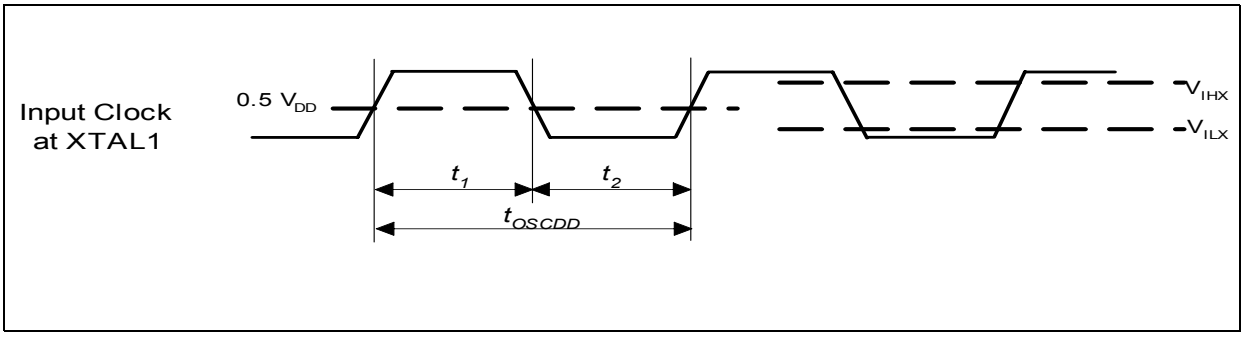

Figure 4-4 Input Clock Timing

4.3.8 EBU Timings

4.3.8.1 SDCLKO Output Clock Timing

(Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limits[1]		Limits[2]		Unit
			min	max	min	max	
SDCLKO period	t_1	CC	10	–	8.3	–	ns
SDCLKO high time	t_2	CC	3	–	2.5	–	ns
SDCLKO low time	t_3	CC	3	–	2.5	–	ns
SDCLKO rise time	t_4	CC	–	2.5	–	2.5	ns
SDCLKO fall time	t_5	CC	–	2.5	–	2.5	ns

1) The parameters are applicable for PC100 SDRAM access and the maximum SDCLKO is up to 100 MHz.

2) The parameters are applicable for PC133 SDRAM access and the maximum SDCLKO is up to 120 MHz.

4.3.8.2 BFCLKO Output Clock Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit [1]		Limit [2]		Unit
			min	max	min	max	
Clock period	t_1	CC	20	–	16.7	–	ns
BFCLKO high time	t_2	CC	6.6	–	7.5	–	ns
BFCLKO low time	t_3	CC	6.6	–	7.5	–	ns
BFCLKO rise time	t_4	CC	–	3.5	–	3.5	ns
BFCLKO fall time	t_5	CC	–	2.5	–	2.5	ns

1) The CPU runs at 150 MHz and the Burst Flash runs at divided by 3 clock.

2) The CPU runs at 120 MHz and the Burst Flash runs at divided by 2 clock.

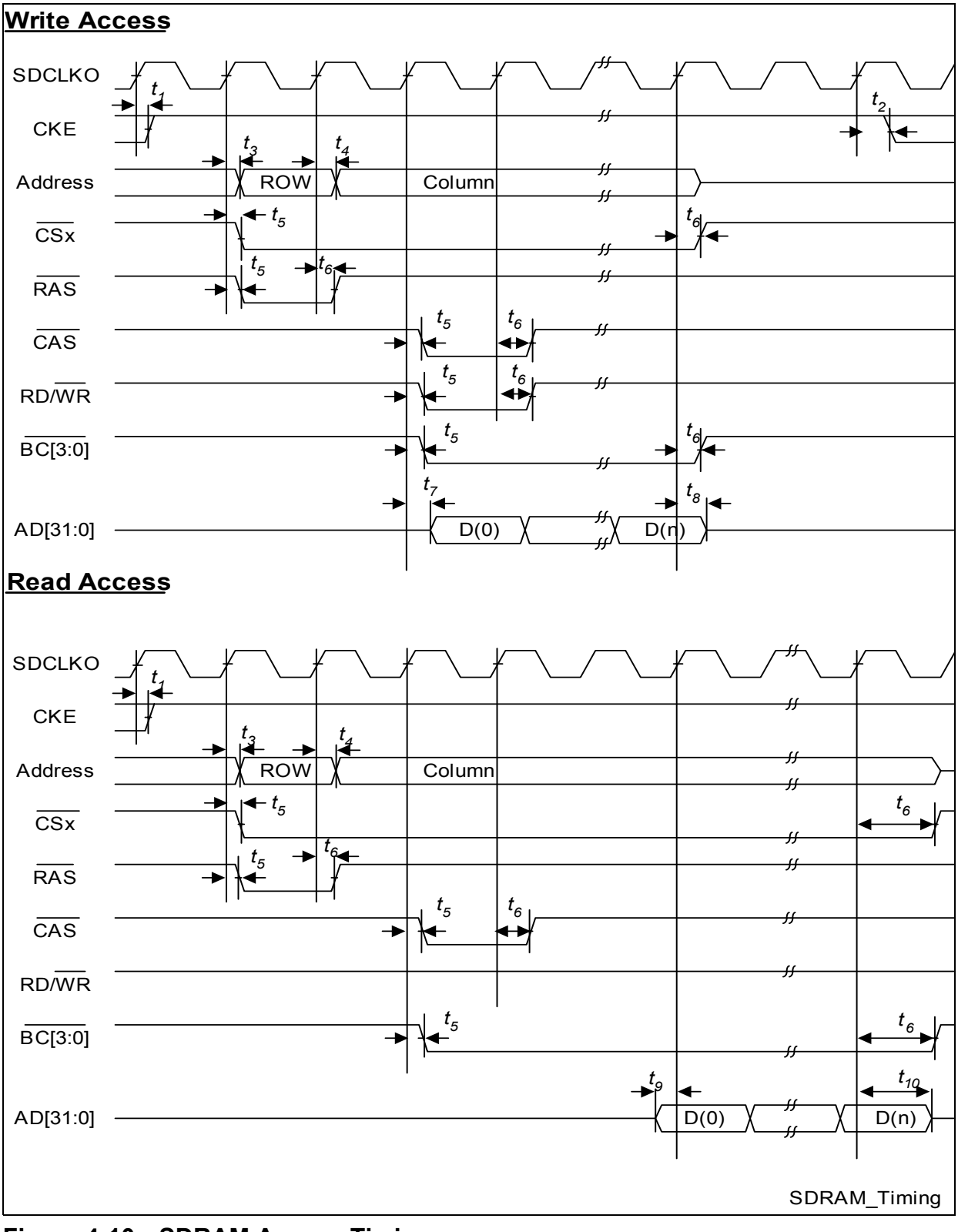

Figure 4-10 SDRAM Access Timing

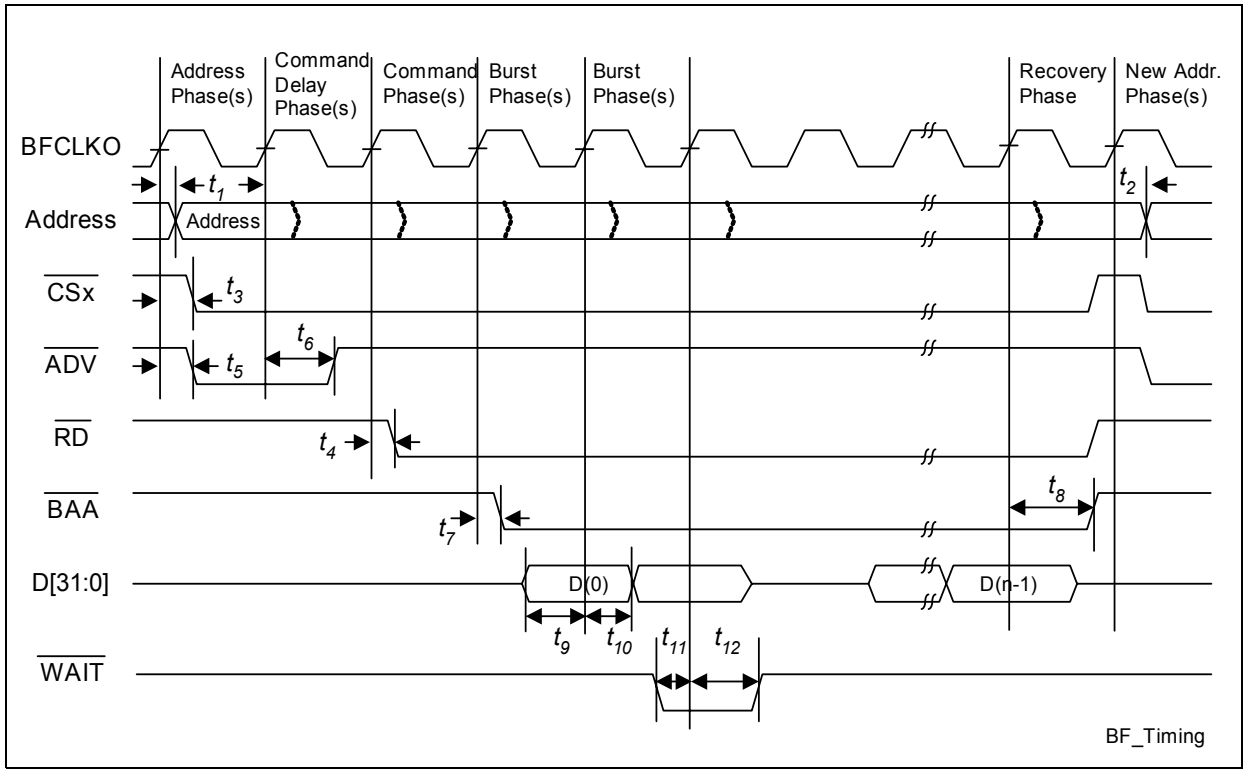

Figure 4-11 Burst Flash Access Timing

Note: Output delays are always referenced to BFCLKO. The reference clock for input characteristics depends on bit BFCON.FDBKEN.
BFCON.FDBKEN = 0: BFCLKO is the input reference clock.
BFCON.FDBKEN = 1: BFCLKI is the input reference clock (EBULMB clock feedback enabled).

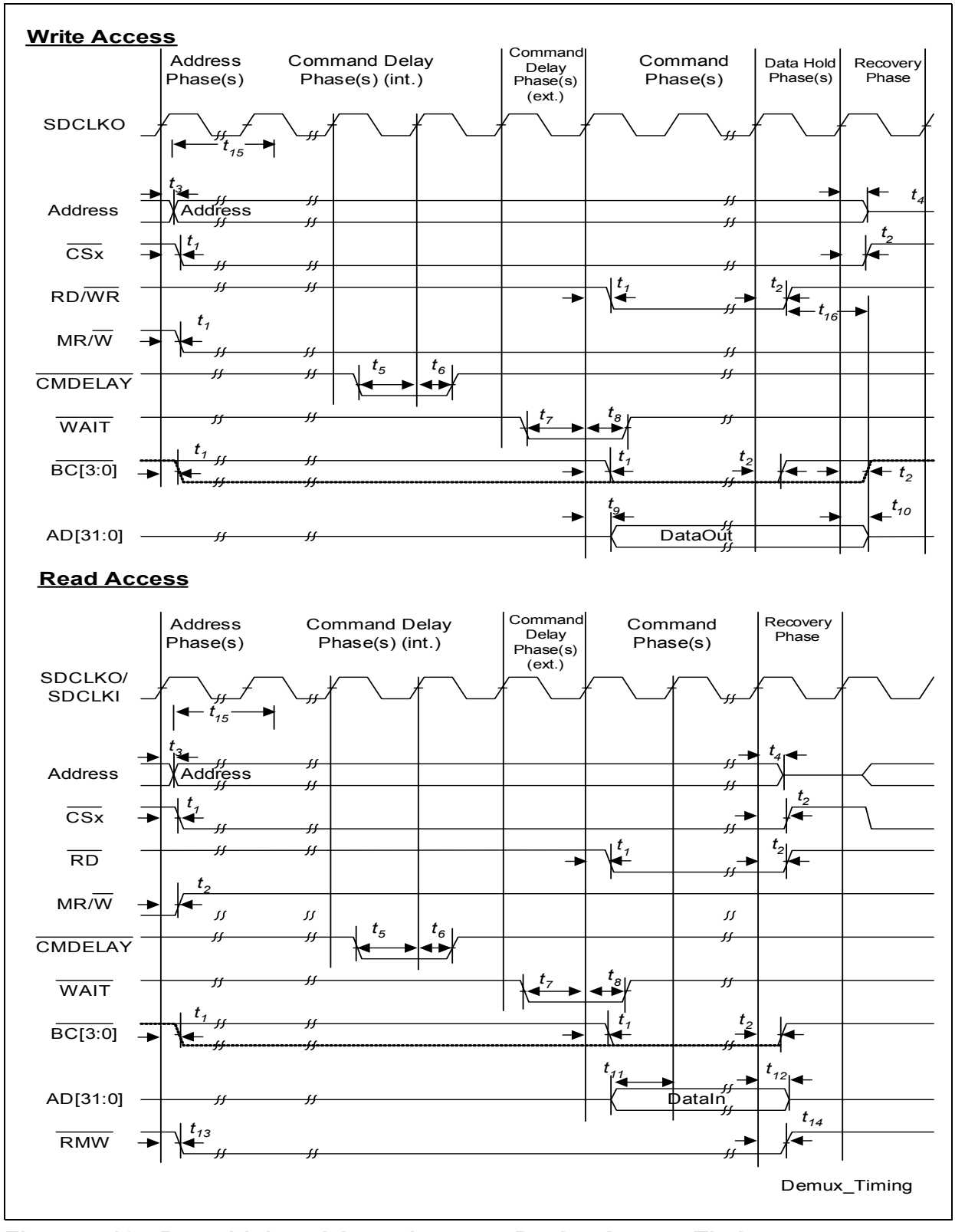

Figure 4-12 Demultiplexed Asynchronous Device Access Timing