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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	-
Interface	-
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	-
Voltage - Core	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8155vfge

Document Revision History

Version History	Description of Change
Rev 0.0	Initial release
Rev 1.0	Fixed typos in Section 1.1.3; Replace any reference to Flash Interface Unit with Flash Memory Module; added note to Vcap pin in **Table 2-2**; corrected **Table 4-4**, removed unneccessary notes in **Table 10-12**; corrected temperature range in **Table 10-14**; added ADC calibration information to **Table 10-23** and new graphs in **Figure 10-22**
Rev 2.0	Corrected 2.2μF to 0.1 μF low ESR capacitor in **Table 2-2**. Replaced **Table 10-16** with correct parameters for the 128 package pinout. Corrected (fout/2) with (fout) in **Table 10-14**. Corrected pinout labels in **Figure 11-1**.
Rev 3.0	Adding/clarifing notes to **Table 4-4** to help clarify independent program flash blocks and other Program Flash modes, clarification to **Table 10-22**, corrected Digital Input Current Low (pullup enabled) numbers in **Table 10-5**. Removed text and Table 10-2; replaced with note to **Table 10-1**.
Rev 4.0	Correcting **Table 4-6** Address locations.
Rev 5.0	Added 56F8155 information; edited to indicate differences in 56F8355 and 56F8155. Reformatted for Freescale look and feel. Updated Temperature Sensor and ADC tables, then updated balance of electrical tables for consistency throughout the family. Clarified I/O power description in **Table 2-2**, added note to **Table 10-7** and clarified **Section 12.3**.
Rev 6.0	Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed P_D in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**.
Rev 7.0	Updated **Table 10-23** to reflect new value for maximum Uncalibrated Gain Error
Rev 8.0	Deleted RSTO from Pin Group 2 (listed after **Table 10-1**). Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) in **Table 10-4**. Added RoHS-compliance and "pb-free" language to back cover.
Rev 9.0	Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.
Rev 10.0	Replaced "Tri-stated" with an explanation in State During Reset column in **Table 2-2**.
Rev 11.0	Corrected bootflash memory map layout in **Table 4-4** to 16KB.
Rev. 12	• Added the following note to the description of the TMS signal in **Table 2-2**: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor. • Added the following note to the description of the $\overline{TRST}$ signal in **Table 2-2**: **Note:** For normal operation, connect $\overline{TRST}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{TRST}$ may be tied to V_{SS} through a 1K resistor.

Please see http://www.freescale.com for the most current data sheet revision.

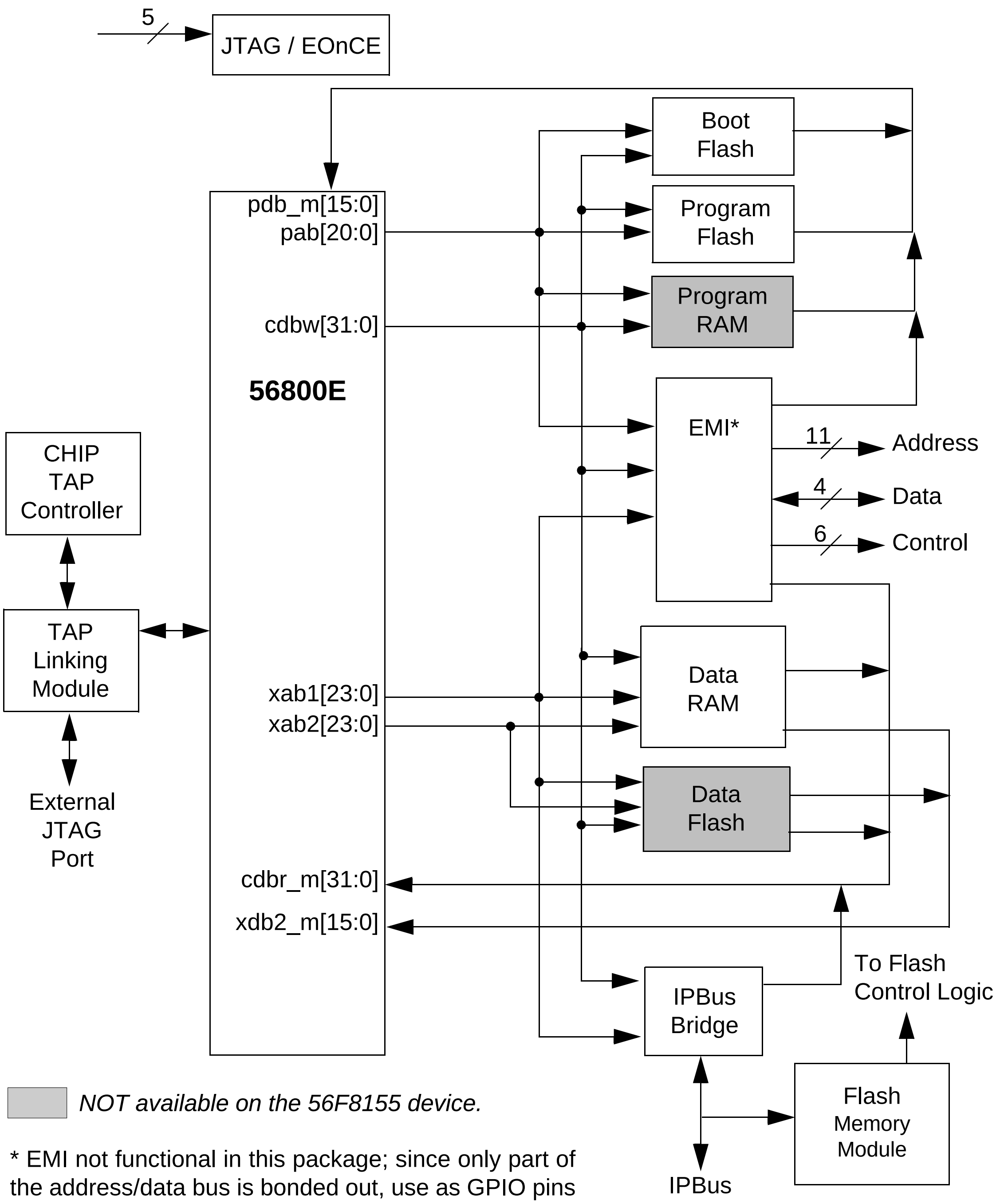

Figure 1-1 System Bus Interfaces

Note: Flash memories are encapsulated within the Flash Memory (FM) Module. Flash control is accomplished by the I/O to the FM over the peripheral bus, while reads and writes are completed between the core and the Flash memories.

Note: The primary data RAM port is 32 bits wide. Other data ports are 16 bits.

Table 2-2 Signal and Package Information for the 128-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
ANB0	96	Input	Analog Input	**ANB0 - 3** — Analog inputs to ADC B, channel 0
ANB1	97			
ANB2	98			
ANB3	99			
ANB4	100	Input	Analog Input	**ANB4 - 7** — Analog inputs to ADC B, channel 1
ANB5	101			
ANB6	102			
ANB7	103			
TEMP_SENSE	88	Output	Analog Output	**Temperature Sense Diode** — This signal connects to an on-chip diode that can be connected to one of the ADC inputs and used to monitor the temperature of the die. Must be bypassed with a 0.01μF capacitor.
CAN_RX	121	Schmitt Input	Input, pullup enabled	**FlexCAN Receive Data** — This is the CAN input. This pin has an internal pullup resistor. To deactivate the internal pullup resistor, set the CAN bit in the SIM_PUDR register.
CAN_TX	120	Open Drain Output	Open Drain Output	**FlexCAN Transmit Data** — This is the CAN output.
TC0 **(GPIOE8)**	111	Schmitt Input/ Output Schmitt Input/ Output	Input, pullup enabled	**TC0 - 1** — Timer C, Channels 0 and 1 **Port E GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to Timer functionality. To deactivate the internal pullup resistor, clear the appropriate bit of the GPIOE_PUR register. See **Part 6.5.6** for details.
TC1 (GPIOE9)	113			

Table 4-21 Analog-to-Digital Converter Registers Address Map (Continued)
(ADCB_BASE = $00 F240)

Register Acronym	Address Offset	Register Description
ADCB_RSLT 2	$B	Result Register 2
ADCB_RSLT 3	$C	Result Register 3
ADCB_RSLT 4	$D	Result Register 4
ADCB_RSLT 5	$E	Result Register 5
ADCB_RSLT 6	$F	Result Register 6
ADCB_RSLT 7	$10	Result Register 7
ADCB_LLMT 0	$11	Low Limit Register 0
ADCB_LLMT 1	$12	Low Limit Register 1
ADCB_LLMT 2	$13	Low Limit Register 2
ADCB_LLMT 3	$14	Low Limit Register 3
ADCB_LLMT 4	$15	Low Limit Register 4
ADCB_LLMT 5	$16	Low Limit Register 5
ADCB_LLMT 6	$17	Low Limit Register 6
ADCB_LLMT 7	$18	Low Limit Register 7
ADCB_HLMT 0	$19	High Limit Register 0
ADCB_HLMT 1	$1A	High Limit Register 1
ADCB_HLMT 2	$1B	High Limit Register 2
ADCB_HLMT 3	$1C	High Limit Register 3
ADCB_HLMT 4	$1D	High Limit Register 4
ADCB_HLMT 5	$1E	High Limit Register 5
ADCB_HLMT 6	$1F	High Limit Register 6
ADCB_HLMT 7	$20	High Limit Register 7
ADCB_OFS 0	$21	Offset Register 0
ADCB_OFS 1	$22	Offset Register 1
ADCB_OFS 2	$23	Offset Register 2
ADCB_OFS 3	$24	Offset Register 3
ADCB_OFS 4	$25	Offset Register 4
ADCB_OFS 5	$26	Offset Register 5
ADCB_OFS 6	$27	Offset Register 6
ADCB_OFS 7	$28	Offset Register 7
ADCB_POWER	$29	Power Control Register
ADCB_CAL	$2A	ADC Calibration Register

Table 4-22 Temperature Sensor Register Address Map (TSENSOR_BASE = $00 F270)
Temperature Sensor is NOT available in the 56F8155 device

Register Acronym	Address Offset	Register Description
TSENSOR_CNTL	$0	Control Register

Table 4-23 Serial Communication Interface 0 Registers Address Map (SCI0_BASE = $00 F280)

Register Acronym	Address Offset	Register Description
SCI0_SCIBR	$0	Baud Rate Register
SCI0_SCICR	$1	Control Register
		Reserved
SCI0_SCISR	$3	Status Register
SCI0_SCIDR	$4	Data Register

Table 4-24 Serial Communication Interface 1 Registers Address Map (SCI1_BASE = $00 F290)

Register Acronym	Address Offset	Register Description
SCI1_SCIBR	$0	Baud Rate Register
SCI1_SCICR	$1	Control Register
		Reserved
SCI1_SCISR	$3	Status Register
SCI1_SCIDR	$4	Data Register

Table 4-25 Serial Peripheral Interface 0 Registers Address Map (SPI0_BASE = $00 F2A0)

Register Acronym	Address Offset	Register Description
SPI0_SPSCR	$0	Status and Control Register
SPI0_SPDSR	$1	Data Size Register
SPI0_SPDRR	$2	Data Receive Register
SPI0_SPDTR	$3	Data Transmitter Register

5.2 Features

The ITCN module design includes these distinctive features:

- Programmable priority levels for each IRQ
- Two programmable Fast Interrupts
- Notification to SIM module to restart clocks out of Wait and Stop modes
- Drives initial address on the address bus after reset

For further information, see **Table 4-5**, Interrupt Vector Table Contents.

5.3 Functional Description

The Interrupt Controller is a slave on the IPBus. It contains registers allowing each of the 82 interrupt sources to be set to one of four priority levels, excluding certain interrupts of fixed priority. Next, all of the interrupt requests of a given level are priority encoded to determine the lowest numerical value of the active interrupt requests for that level. Within a given priority level, 0 is the highest priority, while number 81 is the lowest.

5.3.1 Normal Interrupt Handling

Once the ITCN has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the VBA and the vector number to determine the vector address. In this way, an offset is generated into the vector table for each interrupt.

5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The following tables define the nesting requirements for each priority level.

Table 5-1 Interrupt Mask Bit Definition

SR[9][1]	SR[8][1]	Permitted Exceptions	Masked Exceptions
0	0	Priorities 0, 1, 2, 3	None
0	1	Priorities 1, 2, 3	Priority 0
1	0	Priorities 2, 3	Priorities 0, 1
1	1	Priority 3	Priorities 0, 1, 2

1. Core status register bits indicating current interrupt mask within the core.

Table 5-2 Interrupt Priority Encoding

IPIC_LEVEL[1:0][1]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No Interrupt or SWILP	Priorities 0, 1, 2, 3

Table 5-2 Interrupt Priority Encoding

IPIC_LEVEL[1:0][1]	Current Interrupt Priority Level	Required Nested Exception Priority
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3
11	Priorities 2 or 3	Priority 3

1. See IPIC field definition in **Part 5.6.30.2**

5.3.3 Fast Interrupt Handling

Fast interrupts are described in the DSP56800E Reference Manual. The interrupt controller recognizes fast interrupts before the core does.

A fast interrupt is defined (to the ITCN) by:

1. Setting the priority of the interrupt as level 2, with the appropriate field in the IPR registers
2. Setting the FIMn register to the appropriate vector number
3. Setting the FIVALn and FIVAHn registers with the address of the code for the fast interrupt

When an interrupt occurs, its vector number is compared with the FIM0 and FIM1 register values. If a match occurs, and it is a level 2 interrupt, the ITCN handles it as a fast interrupt. The ITCN takes the vector address from the appropriate FIVALn and FIVAHn registers, instead of generating an address that is an offset from the VBA.

The core then fetches the instruction from the indicated vector adddress and if it is not a JSR, the core starts its fast interrupt handling.

5.4 Block Diagram

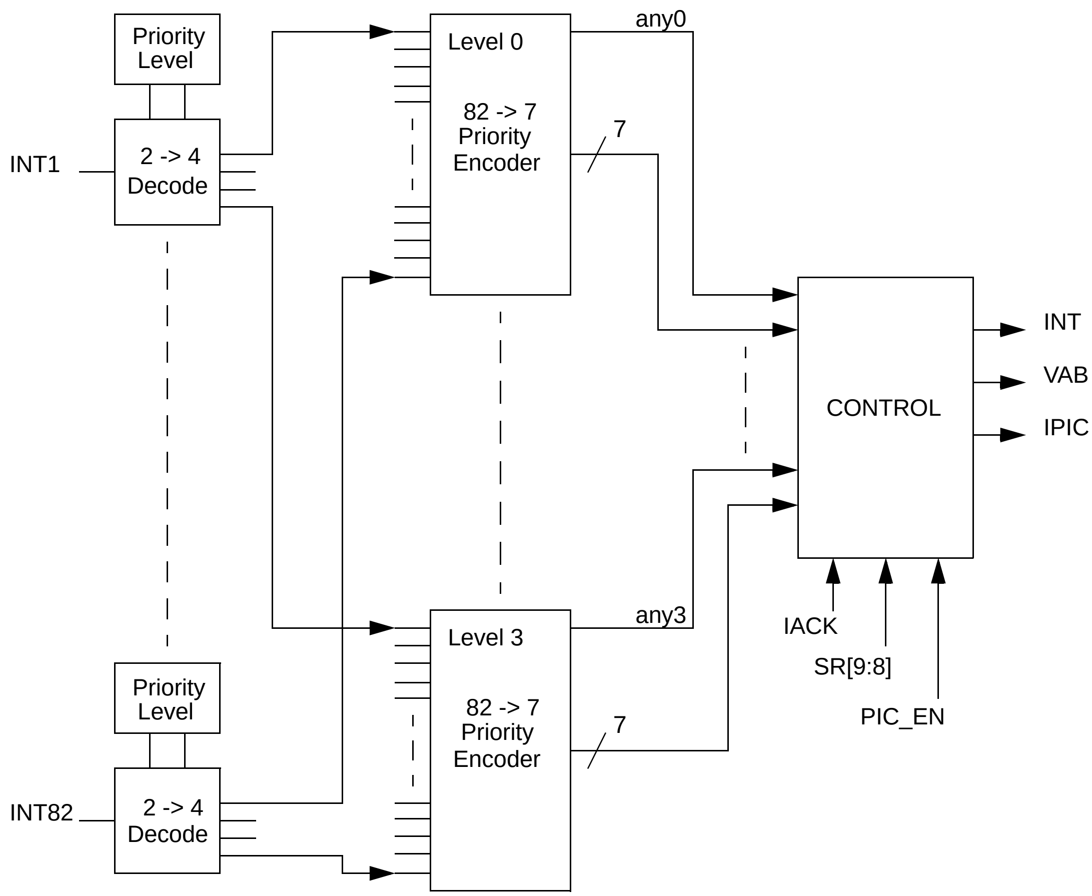

Figure 5-1 Interrupt Controller Block Diagram

5.5 Operating Modes

The ITCN module design contains two major modes of operation:

- **Functional Mode**
  The ITCN is in this mode by default.
- **Wait and Stop Modes**
  During Wait and Stop modes, the system clocks and the 56800E core are turned off. The ITCN will signal a pending IRQ to the System Integration Module (SIM) to restart the clocks and service the IRQ. An IRQ can only wake up the core if the IRQ is enabled prior to entering the Wait or Stop mode. Also, the IRQA and IRQB signals automatically become low-level sensitive in these modes even if the control register bits are set to make them falling-edge sensitive. This is because there is no clock available to detect the falling edge.

  A peripheral which requires a clock to generate interrupts will not be able to generate interrupts during Stop mode. The FlexCAN module can wake the device from Stop mode, and a reset will do just that, or IRQA and IRQB can wake it up.

5.6.5.4 Reserved—Bits 9–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.5.5 GPIOA Interrupt Priority Level (GPIOA IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.6 GPIOB Interrupt Priority Level (GPIOB IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.7 GPIOC Interrupt Priority Level (GPIOC IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6 Interrupt Priority Register 5 (IPR5)

Base + $5	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	DEC1_XIRQ IPL		DEC1_HIRQ IPL		SCI1_RCV IPL		SCI1_RERR IPL		0	0	SCI1_TIDL IPL		SCI1_XMIT IPL		SPI0_XMIT IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-8 Interrupt Priority Register 5 (IPR5)

5.6.6.1 Quadrature Decoder 1 INDEX Pulse Interrupt Priority Level (DEC1_XIRQ IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.2 Quadrature Decoder 1 HOME Signal Transition or Watchdog Timer Interrupt Priority Level (DEC1_HIRQ IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.3 SCI1 Receiver Full Interrupt Priority Level (SCI1_RCV IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.4 SCI1 Receiver Error Interrupt Priority Level (SCI1_RERR IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.1 Timer C, Channel 0 Interrupt Priority Level (TMRC0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.2 Timer D, Channel 3 Interrupt Priority Level (TMRD3 IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.3 Timer D, Channel 2 Interrupt Priority Level (TMRD2 IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.4 Timer D, Channel 1 Interrupt Priority Level (TMRD1 IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FIELD															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-5 SIM Software Control Register 0 (SIM_SCR0)

6.5.3.1 Software Control Data 1 (FIELD)—Bits 15–0

This register is reset only by the Power-On Reset (POR). It has no part-specific functionality and is intended for use by a software developer to contain data that will be unaffected by the other reset sources ($\overline{\text{RESET}}$ pin, software reset, and COP reset).

6.5.4 Most Significant Half of JTAG ID (SIM_MSH_ID)

This read-only register displays the most significant half of the JTAG ID for the chip. This register reads $01F4.

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
Write																
RESET	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

Figure 6-6 Most Significant Half of JTAG ID (SIM_MSH_ID)

6.5.5 Least Significant Half of JTAG ID (SIM_LSH_ID)

This read-only register displays the least significant half of the JTAG ID for the chip. This register reads $601D.

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1
Write																
RESET	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-7 Least Significant Half of JTAG ID (SIM_LSH_ID)

6.5.6 SIM Pullup Disable Register (SIM_PUDR)

Most of the pins on the chip have on-chip pullup resistors. Pins which can operate as GPIO can have these resistors disabled via the GPIO function. Non-GPIO pins can have their pullups disabled by setting the appropriate bit in this register. Disabling pullups is done on a peripheral-by-peripheral basis (for pins not muxed with GPIO). Each bit in the register (see **Figure 6-8**) corresponds to a functional group of pins. See

6.5.6.10 Reserved—Bit 6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.11 CTRL—Bit 5

This bit controls the pullup resistors on the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pins.

6.5.6.12 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.13 JTAG—Bit 3

This bit controls the pullup resistors on the $\overline{\text{TRST}}$, TMS and TDI pins.

6.5.6.14 Reserved—Bit 2–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7 CLKO Select Register (SIM_CLKOSR)

The CLKO select register can be used to multiplex out any one of the clocks generated inside the clock generation and SIM modules. The default value is SYS_CLK. This path has been optimized in order to minimize any delay and clock duty cycle distortion. All other clocks primarily muxed out are for test purposes only, and are subject to significant phase shift at high frequencies.

The upper four bits of the GPIOB register can function as GPIO, A[23:20], or as additional clock output signals. GPIO has priority and is enabled/disabled via the GPIOB_PER. If GPIOB[7:4] are programmed to operate as peripheral outputs, then the choice between A[23:20] and additional clock outputs is done here in the CLKOSR. The default state is for the peripheral function of GPIOB[7:4] to be programmed as A[23:20]. This can be changed by altering A[23:20], as shown in **Figure 6-9**.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	A23	A22	A21	A20	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-9 CLKO Select Register (SIM_CLKOSR)

6.5.7.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7.2 Alternate GPIOB Peripheral Function for A23 (A23)—Bit 9

- 0 = Peripheral output function of GPIOB7 is defined to be A23

6.5.8 GPIO Peripheral Select Register (SIM_GPS)

The GPIO Peripheral Select register can be used to multiplex out any one of the three alternate peripherals for GPIOC. The default peripheral is *Quad Decoder 1* and *Quad Decoder 1*, (NOT available in the 56F8155 device); these peripherals work together.

The four I/O pins associated with GPIOC can function as GPIO, *Quad Decoder 1/Quad Decoder 1*, or as SPI 1 signals. GPIO is not the default and is enabled/disabled via the GPIOC_PER, as shown in **Figure 6-10** and **Table 6-2**. When GPIOC[3:0] are programmed to operate as peripheral I/O, then the choice between decoder/timer and SPI inputs/outputs is made in the SIM_GPS register and in conjunction with the Quad Timer Status and Control Registers (SCR). The default state is for the peripheral function of GPIOC[3:0] to be programmed as decoder functions. This can be changed by altering the appropriate controls in the indicated registers.

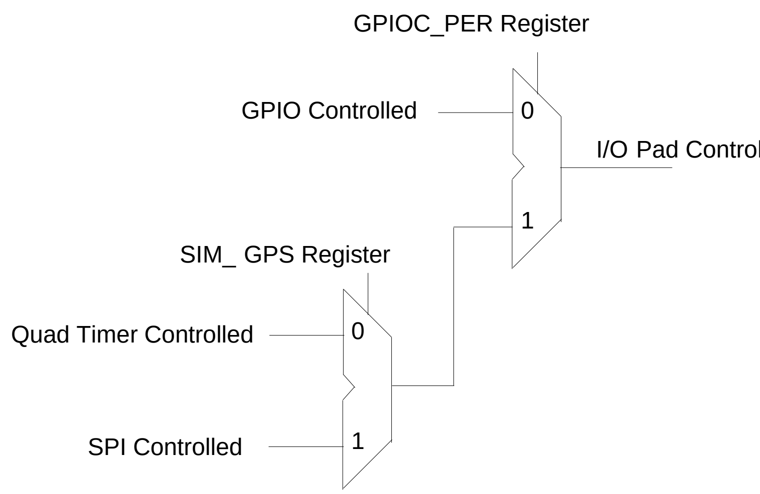

Figure 6-10 Overall Control of Pads Using SIM_GPS Control

Table 6-2 Control of Pads Using SIM_GPS Control [1]

Pin Function	Control Registers				Comments
	GPIOC_PER	GPIOC_DTR	SIM_GPS	Quad Timer SCR Register OEN bits	
GPIO Input	0	0	—	—	
GPIO Output	0	1	—	—	
Quad Timer Input / Quad Decoder Input [2]	1	—	0	0	See the “Switch Matrix for Inputs to the Timer” table in the **56F8300 Peripheral User Manual** for the definition of timer inputs based on the Quad Decoder mode configuration.
Quad Timer Output / Quad Decoder Input [3]	1	—	0	1	

Table 8-1 56F8355 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8355	Peripheral Function	Reset Function
D	13	11	2 pins - EMI CSn 4 pins - EMI CSn - Can only be used as GPIO 2 pins - SCI1 2 pins - EMI CSn - Not available in this package 3 pins - PWMB current sense	EMI Chip Selects EMI Chip Selects SCI1 N/A PWMB current sense
E	14	12	2 pins - SCI0 2 pins - EMI Address pins - Not available in this package 4 pins - SPI0 2 pins - TMRC 4 pins - TMRD	SCI0 N/A SPI0 TMRC TMRD
F	16	4	4 pins - EMI Data - Can only be used as GPIO 12 pins - EMI Data - Not available in this package	EMI Data N/A

Table 8-2 56F8155 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8155	Peripheral Function	Reset Function
A	14	6	6 pins - EMI Address pins - Can only be used as GPIO 8 pins - EMI Address pins - Not available in this package	EMI Address N/A
B	8	5	5 pins - EMI Address pins - Can only be used as GPIO 3 pins - EMI Address pins - Not available in this package	GPIO N/A
C	11	11	4 pins - SPI1 4 pins - DEC0 / TMRA 3 pins - Dedicated GPIO	DEC1 / TMRB DEC0 / TMRA GPIO
D	13	11	6 pins - EMI CSn - Can only be used as GPIO 2 pins - SCI1 2 pins - EMI CSn - Not available in this package 3 pins - PWMB current sense	EMI Chip Selects SCI1 N/A PWMB current sense
E	14	12	2 pins - SCI0 2 pins - EMI Address pins - Not available in this package 4 pins - SPI0 2 pins - TMRC 4 pins - Dedicated GPIO	SCI0 N/A SPI0 TMRC GPIO
F	16	4	4 pins - EMI Data - Can only be used as GPIO 12 pins - EMI Data - Not available in this package	EMI Data N/A

1. Not useful in reset configuration in this package - reconfigure as GPIO
2. See **Part 6.5.8** to determine how to select peripherals from this set; DEC1 is the selected peripheral at reset

Part 9 Joint Test Action Group (JTAG)

9.1 56F8355 Information

Please contact your Freescale marketing representative or authorized distributor for device/package-specific BSDL information.

Part 10 Specifications

10.1 General Characteristics

The 56F8355/56F8155 are fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term “5V-tolerant” refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such sytems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Note: All specifications meet both Automotive and Industrial requirements unless individual specifications are listed.

Note: *The 56F8155 device is guaranteed to 40MHz and specified to meet Industrial requirements only.*

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Note: *The 56F8155 device is specified to meet Industrial requirements only; CAN is NOT available on the 56F8155 device.*

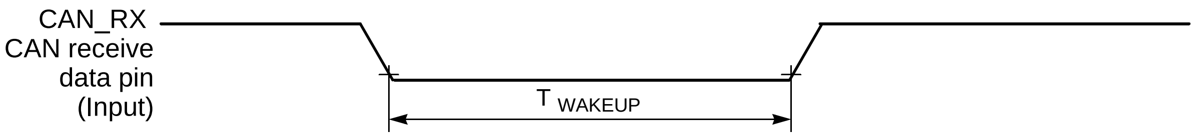

Figure 10-18 Bus Wake Up Detection

10.14 JTAG Timing

Table 10-22 JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation using EOnCE[1]	f_{OP}	DC	SYS_CLK/8	MHz	10-19
TCK frequency of operation not using EOnCE[1]	f_{OP}	DC	SYS_CLK/4	MHz	10-19
TCK clock pulse width	t_{PW}	50	—	ns	10-19
TMS, TDI data set-up time	t_{DS}	5	—	ns	10-20
TMS, TDI data hold time	t_{DH}	5	—	ns	10-20
TCK low to TDO data valid	t_{DV}	—	30	ns	10-20
TCK low to TDO tri-state	t_{TS}	—	30	ns	10-20
$\overline{\text{TRST}}$ assertion time	t_{TRST}	2T[2]	—	ns	10-21

1. TCK frequency of operation must be less than 1/8 the processor rate.
2. T = processor clock period (nominally 1/60MHz)

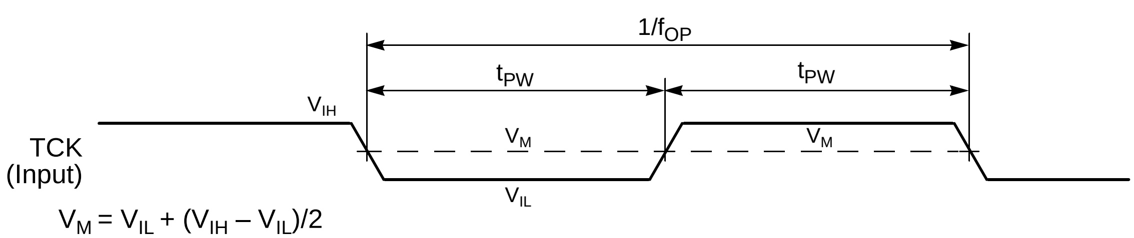

Figure 10-19 Test Clock Input Timing Diagram

PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.

C, the internal [dynamic component], is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic component], reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the IO cell types used on the device reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 10-24 IO Loading Coefficients at 10MHz

	Intercept	Slope
PDU08DGZ_ME	1.3	0.11mW / pF
PDU04DGZ_ME	1.15mW	0.11mW / pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. **Table 10-24** provides coefficients for calculating power dissipated in the IO cells as a function of capacitive load. In these cases:

$TotalPower = \Sigma((\text{Intercept} + \text{Slope}*\text{Cload})*\text{frequency}/10\text{MHz})$

where:

- Summation is performed over all output pins with capacitive loads
- TotalPower is expressed in mW
- Cload is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10mA into LEDs, then P = 8*.5*.01 = 40mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

Table 11-1 56F8355 128-Pin LQFP Package Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
29	GPIOB2	61	PWMA2	93	V_{REFH}	125	MISO0
30	GPIOB3	62	V_{DD_IO}	94	V_{DDA_ADC}	126	MOSI0
31	GPIOB4	63	PWMA3	95	V_{SSA_ADC}	127	PHASEA0
32	PWMB0	64	PWMA4	96	ANB0	128	PHASEB0

1. Primary function is not available in this package configuration; GPIO function must be used instead.

11.2 56F8155 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8155. This device comes in a 128-pin low-profile quad flat pack (LQFP). **Figure 11-1** shows the package outline for the 128-pin LQFP case, **Figure 11-3** shows the mechanical parameters for the 128-pin LQFP case, and **Table 11-1** lists the pin-out for the 128-pin LQFP.