Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	49
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8355vfge

Document Revision History

Version History	Description of Change
Rev 0.0	Initial release
Rev 1.0	Fixed typos in Section 1.1.3; Replace any reference to Flash Interface Unit with Flash Memory Module; added note to Vcap pin in **Table 2-2**; corrected **Table 4-4**, removed unneccessary notes in **Table 10-12**; corrected temperature range in **Table 10-14**; added ADC calibration information to **Table 10-23** and new graphs in **Figure 10-22**
Rev 2.0	Corrected 2.2µF to 0.1 µF low ESR capacitor in **Table 2-2**. Replaced **Table 10-16** with correct parameters for the 128 package pinout. Corrected (fout/2) with (fout) in **Table 10-14**. Corrected pinout labels in **Figure 11-1**.
Rev 3.0	Adding/clarifing notes to **Table 4-4** to help clarify independent program flash blocks and other Program Flash modes, clarification to **Table 10-22**, corrected Digital Input Current Low (pullup enabled) numbers in **Table 10-5**. Removed text and Table 10-2; replaced with note to **Table 10-1**.
Rev 4.0	Correcting **Table 4-6** Address locations.
Rev 5.0	Added 56F8155 information; edited to indicate differences in 56F8355 and 56F8155. Reformatted for Freescale look and feel. Updated Temperature Sensor and ADC tables, then updated balance of electrical tables for consistency throughout the family. Clarified I/O power description in **Table 2-2**, added note to **Table 10-7** and clarified **Section 12.3**.
Rev 6.0	Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed P_D in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**.
Rev 7.0	Updated **Table 10-23** to reflect new value for maximum Uncalibrated Gain Error
Rev 8.0	Deleted RSTO from Pin Group 2 (listed after **Table 10-1**). Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) in **Table 10-4**. Added RoHS-compliance and “pb-free” language to back cover.
Rev 9.0	Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.
Rev 10.0	Replaced “Tri-stated” with an explanation in State During Reset column in **Table 2-2**.
Rev 11.0	Corrected bootflash memory map layout in **Table 4-4** to 16KB.
Rev. 12	• Added the following note to the description of the TMS signal in **Table 2-2**: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor. • Added the following note to the description of the $\overline{TRST}$ signal in **Table 2-2**: **Note:** For normal operation, connect $\overline{TRST}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{TRST}$ may be tied to V_{SS} through a 1K resistor.

Please see http://www.freescale.com for the most current data sheet revision.

Table 2-2 Signal and Package Information for the 128-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
V_{SSA_ADC}	95	Supply		**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
OCR_DIS	71	Input	Input	**On-Chip Regulator Disable** — Tie this pin to V_{SS} to enable the on-chip regulator. Tie this pin to V_{DD} to disable the on-chip regulator. **This pin is intended to be a static DC signal from power-up to shut down. Do no try to toggle this pin for power savings during operation.**
$V_{CAP}1$	49	Supply	Supply	**$V_{CAP}1$ - 4** — When OCR_DIS is tied to V_{SS} (regulator enabled), connect each pin to a 2.2μF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation. When OCR_DIS is tied to V_{DD} (regulator disabled), these pins become V_{DD_CORE} and should be connected to a regulated 2.5V power supply. **Note: This bypass is required even if the chip is powered with an external supply.**
$V_{CAP}2$	122			
$V_{CAP}3$	75			
$V_{CAP}4$	13			
$V_{PP}1$	119	Input	Input	**$V_{PP}1$ - $V_{PP}2$** — These pins should be left unconnected as an open circuit for normal functionality.
$V_{PP}2$	5			
CLKMODE	79	Input	Input	**Clock Input Mode Selection** — This input determines the function of the XTAL and EXTAL pins. 1 = External clock input on XTAL is used to directly drive the input clock of the chip. The EXTAL pin should be grounded. 0 = A crystal or ceramic resonator should be connected between XTAL and EXTAL.
EXTAL	74	Input	Input	**External Crystal Oscillator Input** — This input can be connected to an 8MHz external crystal. Tie this pin low if XTAL is driven by an external clock source.
XTAL	73	Input/ Output	Chip-driven	**Crystal Oscillator Output** — This output connects the internal crystal oscillator output to an external crystal. If an external clock is used, XTAL must be used as the input and EXTAL connected to GND. The input clock can be selected to provide the clock directly to the core. This input clock can also be selected as the input clock for the on-chip PLL.

Table 2-2 Signal and Package Information for the 128-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
MOSI0 **(GPIOE5)**	126	Input/ Output Input/ Output	In reset, output is disabled, pullup is enabled	**SPI 0 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MOSI0. To deactivate the internal pullup resistor, clear bit 5 in the GPIOE_PUR register.
MISO0 **(GPIOE6)**	125	Input/ Output Input/ Output	Input, pullup enabled	**SPI 0 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MISO0. To deactivate the internal pullup resistor, clear bit 6 in the GPIOE_PUR register.
$\overline{\text{SS0}}$ **(GPIOE7)**	123	Input Input/ Output	Input, pullup enabled	**SPI 0 Slave Select** — $\overline{\text{SS0}}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received. **Port E GPIO** — This GPIO pin can be individually programmed as input or output pin. After reset, the default state is $\overline{\text{SS0}}$. To deactivate the internal pullup resistor, clear bit 7 in the GPIOE_PUR register.

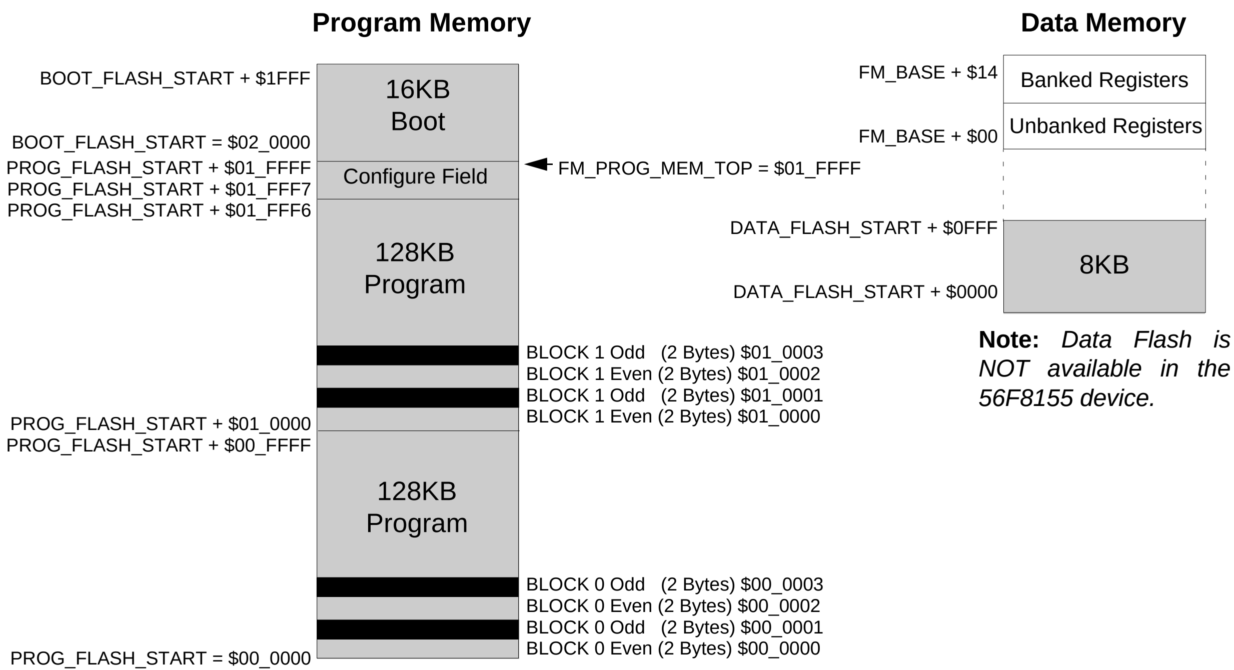


Figure 4-1 Flash Array Memory Maps

Table 4-7 shows the page and sector sizes used within each Flash memory block on the chip.

Note: *Data Flash is NOT available on the 56F8155 device.*

Table 4-7 Flash Memory Partitions

	Flash Size	Sectors	Sector Size	Page Size
Program Flash	256KB	16	8K x 16 bits	512 x 16 bits
Data Flash	8KB	16	256 x 16 bits	256 x 16 bits
Boot Flash	16KB	4	2K x 16 bits	256 x 16 bits

Please see **56F8300 Peripheral User Manual** for additional Flash information.

4.6 EOnCE Memory Map

Table 4-8 EOnCE Memory Map

Address	Register Acronym	Register Name
		Reserved

Table 4-13 Quad Timer C Registers Address Map (Continued) (TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRC2_CMP1	$20	Compare Register 1
TMRC2_CMP2	$21	Compare Register 2
TMRC2_CAP	$22	Capture Register
TMRC2_LOAD	$23	Load Register
TMRC2_HOLD	$24	Hold Register
TMRC2_CNTR	$25	Counter Register
TMRC2_CTRL	$26	Control Register
TMRC2_SCR	$27	Status and Control Register
TMRC2_CMPLD1	$28	Comparator Load Register 1
TMRC2_CMPLD2	$29	Comparator Load Register 2
TMRC2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRC3_CMP1	$30	Compare Register 1
TMRC3_CMP2	$31	Compare Register 2
TMRC3_CAP	$32	Capture Register
TMRC3_LOAD	$33	Load Register
TMRC3_HOLD	$34	Hold Register
TMRC3_CNTR	$35	Counter Register
TMRC3_CTRL	$36	Control Register
TMRC3_SCR	$37	Status and Control Register
TMRC3_CMPLD1	$38	Comparator Load Register 1
TMRC3_CMPLD2	$39	Comparator Load Register 2
TMRC3_COMSCR	$3A	Comparator Status and Control Register

Table 4-14 Quad Timer D Registers Address Map (TMRD_BASE = $00 F100)
Quad Timer D is NOT available in the 56F8155 device

Register Acronym	Address Offset	Register Description
TMRD0_CMP1	$0	Compare Register 1
TMRD0_CMP2	$1	Compare Register 2
TMRD0_CAP	$2	Capture Register

Table 4-15 Pulse Width Modulator A Registers Address Map (Continued) (PWMA_BASE = $00 F140)
PWMA is NOT available in the 56F8155 device

Register Acronym	Address Offset	Register Description
PWMA_PMDEADTM	$C	Dead Time Register
PWMA_PMDISMAP1	$D	Disable Mapping Register 1
PWMA_PMDISMAP2	$E	Disable Mapping Register 2
PWMA_PMCFG	$F	Configure Register
PWMA_PMCCR	$10	Channel Control Register
PWMA_PMPORT	$11	Port Register
PWMA_PMICCR	$12	PWM Internal Correction Control Register

Table 4-16 Pulse Width Modulator B Registers Address Map (PWMB_BASE = $00 F160)

Register Acronym	Address Offset	Register Description
PWMB_PMCTL	$0	Control Register
PWMB_PMFCTL	$1	Fault Control Register
PWMB_PMFSA	$2	Fault Status Acknowledge Register
PWMB_PMOUT	$3	Output Control Register
PWMB_PMCNT	$4	Counter Register
PWMB_PWMCM	$5	Counter Modulo Register
PWMB_PWMVAL0	$6	Value Register 0
PWMB_PWMVAL1	$7	Value Register 1
PWMB_PWMVAL2	$8	Value Register 2
PWMB_PWMVAL3	$9	Value Register 3
PWMB_PWMVAL4	$A	Value Register 4
PWMB_PWMVAL5	$B	Value Register 5
PWMB_PMDEADTM	$C	Dead Time Register
PWMB_PMDISMAP1	$D	Disable Mapping Register 1
PWMB_PMDISMAP2	$E	Disable Mapping Register 2
PWMB_PMCFG	$F	Configure Register
PWMB_PMCCR	$10	Channel Control Register
PWMB_PMPORT	$11	Port Register
PWMB_PMICCR	$12	PWM Internal Correction Control Register

Table 4-31 GPIOC Registers Address Map (GPIOC_BASE = $00 F310)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOC_PUR	$0	Pullup Enable Register	0 x 07FF
GPIOC_DR	$1	Data Register	0 x 0000
GPIOC_DDR	$2	Data Direction Register	0 x 0000
GPIOC_PER	$3	Peripheral Enable Register	0 x 07FF
GPIOC_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOC_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOC_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOC_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOC_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOC_PPMODE	$9	Push-Pull Mode Register	0 x 07FF
GPIOC_RAWDATA	$A	Raw Data Input Register	—

Table 4-32 GPIOD Registers Address Map (GPIOD_BASE = $00 F320)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOD_PUR	$0	Pullup Enable Register	0 x 1FFF
GPIOD_DR	$1	Data Register	0 x 0000
GPIOD_DDR	$2	Data Direction Register	0 x 0000
GPIOD_PER	$3	Peripheral Enable Register	0 x 1FC0
GPIOD_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOD_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOD_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOD_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOD_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOD_PPMODE	$9	Push-Pull Mode Register	0 x 1FFF
GPIOD_RAWDATA	$A	Raw Data Input Register	—

Table 4-37 Flash Module Registers Address Map (Continued) (FM_BASE = $00 F400)

Register Acronym	Address Offset	Register Description
		Reserved
		Reserved
FMPROT	$10	Protection Register (Banked)
FMPROTB	$11	Protection Boot Register (Banked)
		Reserved
FMUSTAT	$13	User Status Register (Banked)
FMCMD	$14	Command Register (Banked)
		Reserved
		Reserved
FMOPT 0	$1A	16-Bit Information Option Register 0 Hot temperature ADC reading of Temperature Sensor; value set during factory test
FMOPT 1	$1B	16-Bit Information Option Register 1 Not used
FMOPT 2	$1C	16-Bit Information Option Register 2 Room temperature ADC reading of Temperature Sensor; value set during factory test

Table 4-38 FlexCAN Registers Address Map (FC_BASE = $00 F800) *FlexCAN is NOT available in the 56F8155 device*

Register Acronym	Address Offset	Register Description
FCMCR	$0	Module Configuration Register
		Reserved
FCCTL0	$3	Control Register 0 Register
FCCTL1	$4	Control Register 1 Register
FCTMR	$5	Free-Running Timer Register
FCMAXMB	$6	Maximum Message Buffer Configuration Register
		Reserved
FCRXGMASK_H	$8	Receive Global Mask High Register
FCRXGMASK_L	$9	Receive Global Mask Low Register
FCRX14MASK_H	$A	Receive Buffer 14 Mask High Register
FCRX14MASK_L	$B	Receive Buffer 14 Mask Low Register
FCRX15MASK_H	$C	Receive Buffer 15 Mask High Register

Table 5-3 ITCN Register Summary (ITCN_BASE = $00F1A0) (Continued)

Register Acronym	Base Address +	Register Name	Section Location

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	0	0	BKPT_U0 IPL		STPCNT IPL		0	0	0	0	0	0	0	0	0	0
		W																
$1	IPR1	R	0	0	0	0	0	0	0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL	
		W																
$2	IPR2	R	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	IRQB IPL		IRQA IPL	
		W																
$3	IPR3	R	GPIOD IPL		GPIOE IPL		GPIOF IPL		FCMSGBUF IPL		FCWKUP IPL		FCERR IPL		FCBOFF IPL		0	0
		W																
$4	IPR4	R	SPI0_RCV IPL		SPI1_XMIT IPL		SPI1_RCV IPL		0	0	0	0	GPIOA IPL		GPIOB IPL		GPIOC IPL	
		W																
$5	IPR5	R	DEC1_XIRQ IPL		DEC1_HIRQ IPL		SCI1_RCV IPL		SCI1_RERR IPL		0	0	SCI1_TIDL IPL		SCI1_XMIT IPL		SPI0_XMIT IPL	
		W																
$6	IPR6	R	TMRC0 IPL		TMRD3 IPL		TMRD2 IPL		TMRD1 IPL		TMRD0 IPL		0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
		W																
$7	IPR7	R	TMRA0 IPL		TMRB3 IPL		TMRB2 IPL		TMRB1 IPL		TMRB0 IPL		TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
		W																
$8	IPR8	R	SCI0_RCV IPL		SCI0_RERR IPL		0	0	SCI0_TIDL IPL		SCI0_XMIT IPL		TMRA3 IPL		TMRA2 IPL		TMRA1 IPL	
		W																
$9	IPR9	R	PWMA_F IPL		PWMB_F IPL		PWMA_RL IPL		PWMB_RL IPL		ADCA_ZC IPL		ABCB_ZC IPL		ADCA_CC IPL		ADCB_CC IPL	
		W																
$A	VBA	R	0	0	0	VECTOR BASE ADDRESS												
		W																
$B	VBA0	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
		W																
$C	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$D	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$E	FIM1	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
		W	0	0	0	0	0	0	0	0	0							
$F	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$10	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W	0	0	0	0	0	0	0	0	0	0	0					
$11	IRQP0	R	PENDING [16:2]															1
		W																
$12	IRQP1	R	PENDING [32:17]															
		W																
$13	IRQP2	R	PENDING [48:33]															
		W																

Figure 5-2 ITCN Register Map Summary

5.6.21 IRQ Pending 3 Register (IRQP3)

Base + $14	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [64:49]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-23 IRQ Pending 3 Register (IRQP3)

5.6.21.1 IRQ Pending (PENDING)—Bits 64–49

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.22 IRQ Pending 4 Register (IRQP4)

Base + $15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [80:65]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-24 IRQ Pending 4 Register (IRQP4)

5.6.22.1 IRQ Pending (PENDING)—Bits 80–65

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.23 IRQ Pending 5 Register (IRQP5)

Base + $16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	PEND-ING [81]
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-25 IRQ Pending Register 5 (IRQP5)

5.6.23.1 Reserved—Bits 96–82

This bit field is reserved or not implemented. The bits are read as 1 and cannot be modified by writing.

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	O	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0					0	0

Figure 6-4 SIM Reset Status Register (SIM_RSTSTS)

6.5.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.2.2 Software Reset (SWR)—Bit 5

When 1, this bit indicates that the previous reset occurred as a result of a software reset (write to SW RST bit in the SIM_CONTROL register). This bit will be cleared by any hardware reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.3 COP Reset (COPR)—Bit 4

When 1, the COPR bit indicates the Computer Operating Properly (COP) timer-generated reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.4 External Reset (EXTR)—Bit 3

If 1, the EXTR bit indicates an external system reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit position will clear it. Basically, when the EXTR bit is 1, the previous system reset was caused by the external $\overline{\text{RESET}}$ pin being asserted low.

6.5.2.5 Power-On Reset (POR)—Bit 2

When 1, the POR bit indicates a Power-On Reset occurred some time in the past. This bit can be cleared only by software or by another type of reset. Writing a 0 to this bit will set the bit, while writing a 1 to the bit position will clear the bit. In summary, if the bit is 1, the previous system reset was due to a Power-On Reset.

6.5.2.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.3 SIM Software Control Registers (SIM_SCR0, SIM_SCR1, SIM_SCR2, and SIM_SCR3)

Only SIM_SCR0 is shown below. SIM_SCR1, SIM_SCR2, and SIM_SCR3 are identical in functionality.

6.5.8.5 GPIOC0 (C0)—Bit 0

This bit selects the alternate function for GPIOC0.

- 0 = PHASEA1/TB0 (default)
- 1 = SCLK1

6.5.9 Peripheral Clock Enable Register (SIM_PCE)

The Peripheral Clock Enable register is used enable or disable clocks to the peripherals as a power savings feature. The clocks can be individually controlled for each peripheral on the chip.

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read / Write	EMI	ADCB	ADCA	CAN	DEC1	DEC0	TMRD	TMRC	TMRB	TMRA	SCI 1	SCI 0	SPI 1	SPI 0	PWMB	PWMA
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-12 Peripheral Clock Enable Register (SIM_PCE)

6.5.9.1 External Memory Interface Enable (EMI)—Bit 15

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.2 Analog-to-Digital Converter B Enable (ADCB)—Bit 14

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.3 Analog-to-Digital Converter A Enable (ADCA)—Bit 13

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.4 FlexCAN Enable (CAN)—Bit 12

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.5 Decoder 1 Enable (DEC1)—Bit 11

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled

- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.6 Decoder 0 Enable (DEC0)—Bit 10

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.7 Quad Timer D Enable (TMRD)—Bit 9

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.8 Quad Timer C Enable (TMRC)—Bit 8

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.9 Quad Timer B Enable (TMRB)—Bit 7

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.10 Quad Timer A Enable (TMRA)—Bit 6

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.11 Serial Communications Interface 1 Enable (SCI1)—Bit 5

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.12 Serial Communications Interface 0 Enable (SCI0)—Bit 4

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	ISAL[21:6]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-15 I/O Short Address Location Low Register (SIM_ISALL)

6.5.10.2 Input/Output Short Address Low (ISAL[21:6])—Bit 15–0

This field represents the lower 16 address bits of the "hard coded" I/O short address.

6.6 Clock Generation Overview

The SIM uses an internal master clock from the OCCS (CLKGEN) module to produce the peripheral and system (core and memory) clocks. The maximum master clock frequency is 120MHz. Peripheral and system clocks are generated at half the master clock frequency and therefore at a maximum 60MHz. The SIM provides power modes (Stop, Wait) and clock enables (SIM_PCE register, CLK_DIS, ONCE_EBL) to control which clocks are in operation. The OCCS, power modes, and clock enables provide a flexible means to manage power consumption.

Power utilization can be minimized in several ways. In the OCCS, crystal oscillator, and PLL may be shut down when not in use. When the PLL is in use, its prescaler and postscaler can be used to limit PLL and master clock frequency. Power modes permit system and/or peripheral clocks to be disabled when unused. Clock enables provide the means to disable individual clocks. Some peripherals provide further controls to disable unused subfunctions. Refer to **Part 3 On-Chip Clock Synthesis (OCCS)**, and the **56F8300 Peripheral User Manual** for further details.

6.7 Power Down Modes Overview

The 56F8355/56F8155 operate in one of three power-down modes, as shown in **Table 6-3**.

Table 6-3 Clock Operation in Power-Down Modes

Mode	Core Clocks	Peripheral Clocks	Description
Run	Active	Active	Device is fully functional
Wait	Core and memory clocks disabled	Active	Peripherals are active and can produce interrupts if they have not been masked off. Interrupts will cause the core to come out of its suspended state and resume normal operation. Typically used for power-conscious applications.

The value of the JTAG FM_CLKDIV[6:0] will replace the value of the FM register FMCLKD that divides down the system clock for timed events, as illustrated in **Figure 7-1**. FM_CLKDIV[6] will map to the PRDIV8 bit, and FM_CLKDIV[5:0] will map to the DIV[5:0] bits. The combination of PRDIV8 and DIV must divide the FM input clock down to a frequency of 150kHz-200kHz. The **"Writing the FMCLKD Register"** section in the Flash Memory chapter of the **56F8300 Peripheral User Manual** gives specific equations for calculating the correct values.

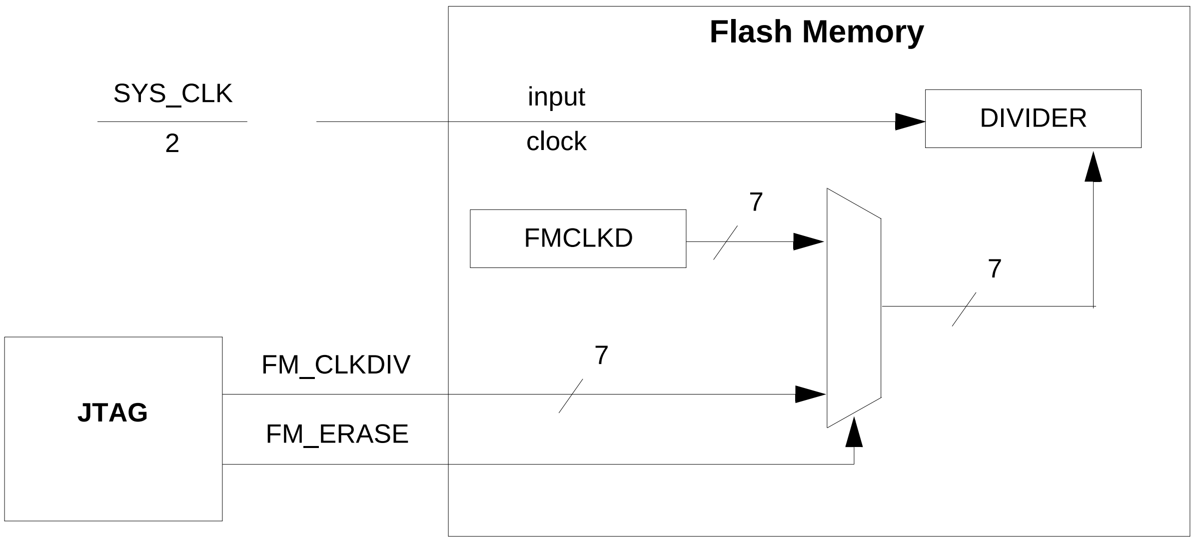


Figure 7-1 JTAG to FM Connection for Lockout Recovery

Two examples of FM_CLKDIV calculations follow.

EXAMPLE 1: If the system clock is the 8MHz crystal frequency because the PLL has not been set up, the input clock will be below 12.8MHz, so PRDIV8 = FM_CLKDIV[6] = 0. Using the following equation yields a DIV value of 19 for a clock of 200kHz, and a DIV value of 20 for a clock of 190kHz. This translates into an FM_CLKDIV[6:0] value of $13 or $14, respectively.

$$150[kHz] < \frac{\left(\frac{SYS\_CLK}{(2)}\right)}{(DIV + 1)} < 200[kHz]$$

EXAMPLE 2: In this example, the system clock has been set up with a value of 32MHz, making the FM

Table 10-2 56F8355/56F8155 ElectroStatic Discharge (ESD) Protection

Characteristic	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	500	—	—	V

Table 10-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			128-pin LQFP		
Junction to ambient Natural convection		$R_{\theta JA}$	50.8	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	46.5	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	43.9	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	41.7	°C/W	1,2
Junction to case		$R_{\theta JC}$	13.9	°C/W	3
Junction to center of case		Ψ_{JT}	1.2	°C/W	4, 5
I/O pin power dissipation		$P_{I/O}$	User-determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Maximum allowed P_D		P_{DMAX}	(TJ - TA) / RθJA[7]	W	

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$) was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p where "s" is the number of signal layers and "p" is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the "case" temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the "resistance" from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See **Part 12.1** for more details on thermal design considerations.
7. TJ = Junction temperature

Table 10-7 Current Consumption per Power Supply Pin (Typical)
On-Chip Regulator Enabled (OCR_DIS = Low)

Mode	I_{DD_IO}[1]	I_{DD_ADC}	$I_{DD\_OSC\_PLL}$	Test Conditions
Stop1	6mA	0uA	155uA	• 8MHz Device Clock • All peripheral clocks are off • ADC powered off • PLL powered off
Stop2	5.1mA	0uA	145uA	• External Clock is off • All peripheral clocks are off • ADC powered off • PLL powered off

1. No Output Switching
2. Includes Processor Core current supplied by internal voltage regulator

Table 10-8 Current Consumption per Power Supply Pin (Typical)
On-Chip Regulator Disabled (OCR_DIS = High)

Mode	I_{DD_Core}	I_{DD_IO}[1]	I_{DD_ADC}	$I_{DD\_OSC\_PLL}$	Test Conditions
RUN1_MAC	150 mA	13μA	50mA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • All peripherals running • Continuous MAC instructions with fetches from Data RAM • ADC powered on and clocked
Wait3	86mA	13μA	70μA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • ADC powered off
Stop1	900μA	13μA	0μA	155μA	• 8MHz Device Clock • All peripheral clocks are off • ADC powered off • PLL powered off
Stop2	100μA	13μA	0μA	145μA	• External Clock is off • All peripheral clocks are off • ADC powered off • PLL powered off

1. No Output Switching

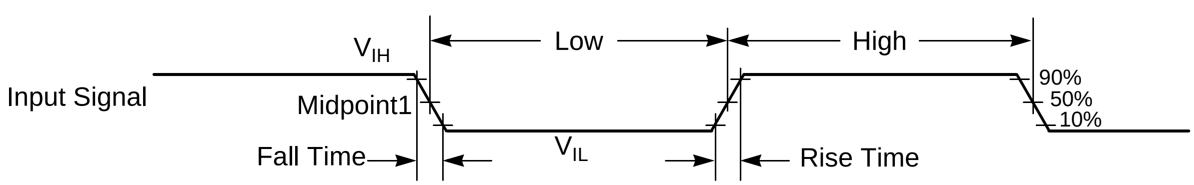
Table 10-11 Temperature Sense Parametrics

Characteristics	Symbol	Min	Typical	Max	Unit
Room Trim Temp. [1, 2]	T_{RT}	24	26	28	°C
Hot Trim Temp. (Industrial)[1,2]	T_{HT}	122	125	128	°C
Hot Trim Temp. (Automotive)[1,2]	T_{HT}	147	150	153	°C
Output Voltage @ V_{DDA_ADC} = 3.3V, T_J =0°C[1]	V_{TS0}	—	1.370	—	V
Supply Voltage	V_{DDA_ADC}	3.0	3.3	3.6	V
Supply Current - OFF	I_{DD-OFF}	—	—	10	µA
Supply Current - ON	I_{DD-ON}	—	—	250	µA
Accuracy[3,1] from -40°C to 150°C Using $V_{TS} = mT + V_{TS0}$	T_{ACC}	-6.7	0	6.7	°C
Resolution[4, 5,1]	R_{ES}	—	0.104	—	°C / bit

1. Includes the ADC conversion of the analog Temperature Sense voltage.
2. The ADC is not calibrated for the conversion of the Temperature Sensor trim value stored in the Flash Memory at FMOPT0 and FMOPT1.
3. See Application Note, AN1980, for methods to increase accuracy.
4. Assuming a 12-bit range from 0V to 3.3V.
5. Typical resolution calculated using equation,

10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in **Table 10-5**. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in **Figure 10-2**.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 10-2 Input Signal Measurement References

Figure 10-3 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state

10.12 Serial Communication Interface (SCI) Timing

Table 10-20 SCI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate[2]	BR	—	$(f_{MAX}/16)$	Mbps	—
RXD[3] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns	10-16
TXD[4] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns	10-17

1. Parameters listed are guaranteed by design.
2. f_{MAX} is the frequency of operation of the system clock, ZCLK, in MHz, which is 60MHz for the 56F8355 device and 40MHz for the 56F8155 device.
3. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
4. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.

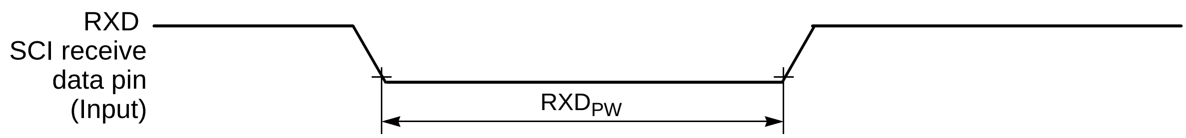


Figure 10-16 RXD Pulse Width

Figure 10-17 TXD Pulse Width

10.13 Controller Area Network (CAN) Timing

Note: *CAN is NOT available in the 56F8155 device.*

Table 10-21 CAN Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate	BR_{CAN}	—	1	Mbps	—
Bus Wake Up detection	T_{WAKEUP}	5	—	µs	10-18

1. Parameters listed are guaranteed by design

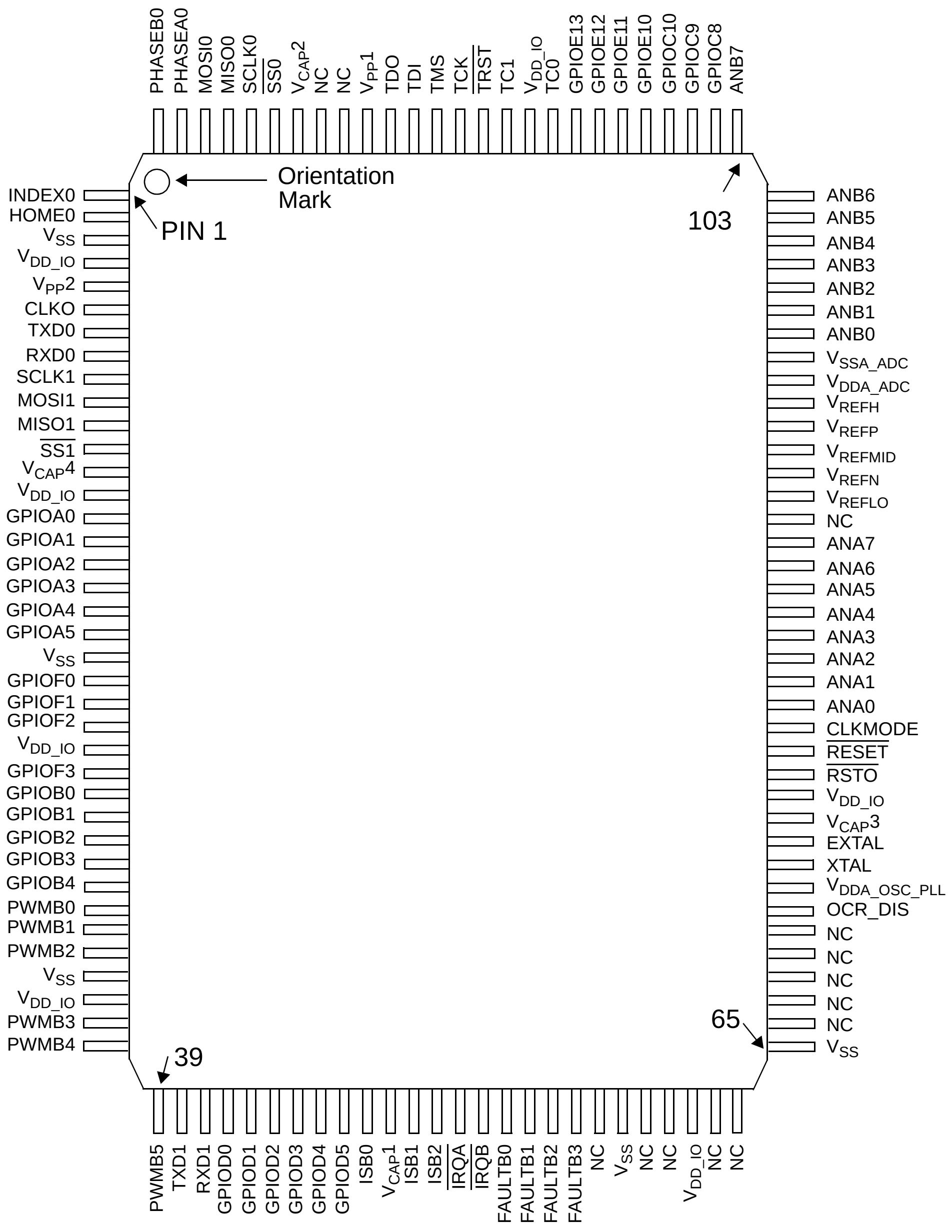


Figure 11-2 Top View, 56F8155 128-Pin LQFP Package

Table 11-2 56F8155 128-Pin LQFP Package Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	INDEX0	33	PWMB1	65	V_{SS}	97	ANB1
2	HOME0	34	PWMB2	66	NC	98	ANB2