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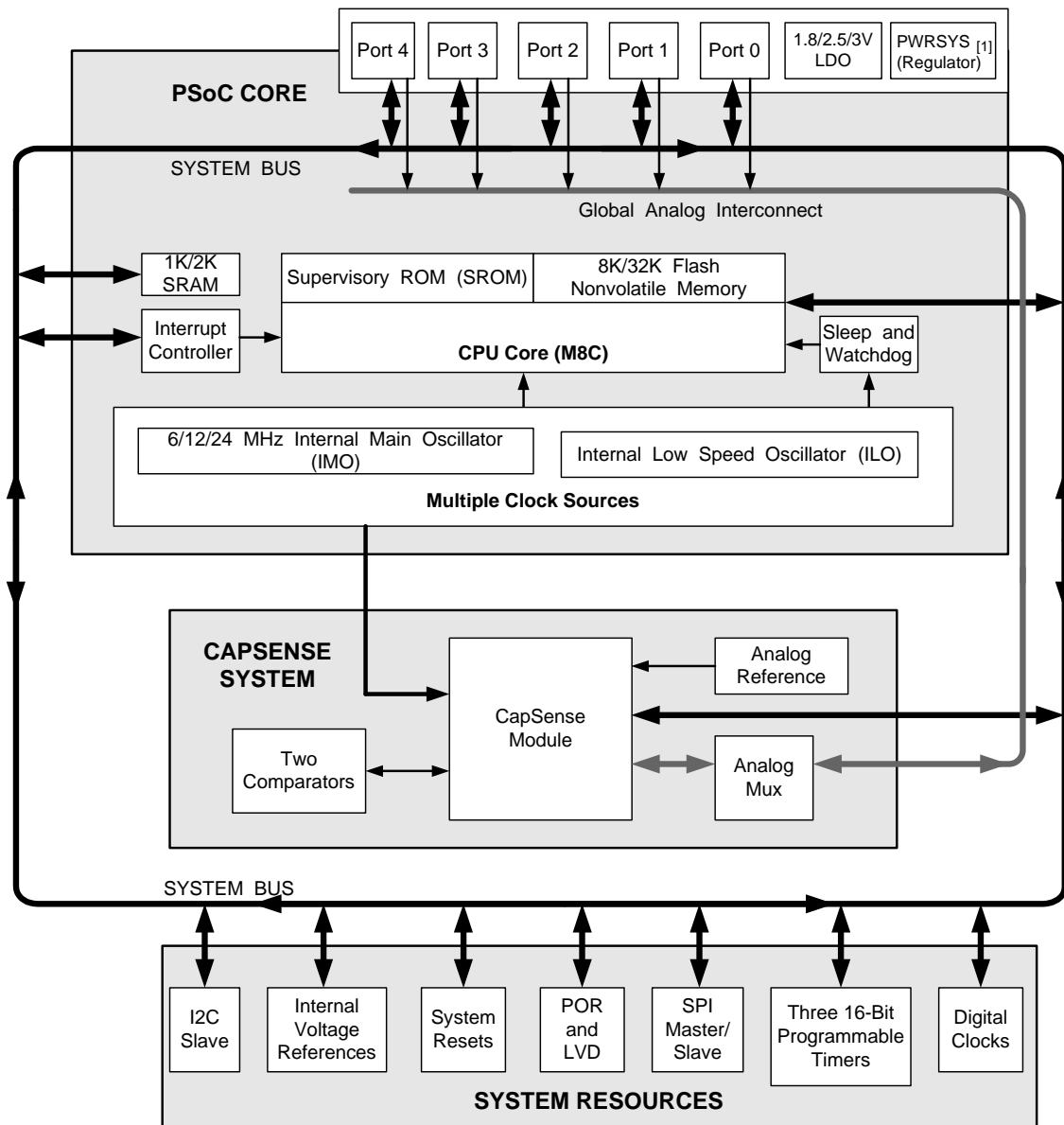
What Are [Embedded - Microcontrollers - Application Specific](#)?

Application specific microcontrollers are engineered to

Details

Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (8kB)
Controller Series	CY8C20xx6A
RAM Size	1K x 8
Interface	I ² C, SPI
Number of I/O	13
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20236a-24lkxa

Logic Block Diagram



Note

1. Internal voltage regulator for internal circuitry

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Additional System Resources

System resources provide additional capability, such as I²C slave, SPI master, or SPI slave interfaces, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I²C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I²C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I²C enhanced slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For usage details, refer to the application note [I2C Enhanced Slave Operation - AN56007](#).
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the [Technical Reference Manual](#) for the CY8C20x36A/66A PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located at www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. Refer to [Development Kits on page 24](#).

Training

Free PSoC and CapSense technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, create a technical support case or call technical support at 1-800-541-4736.

Pinouts

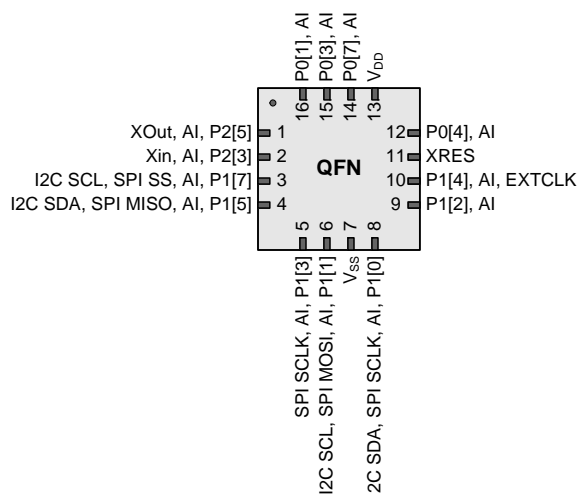
The CY8C20x36A/66A PSoC device is available in a variety of packages, which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of Digital I/O and connection to the common analog bus. However, V_{SS} , V_{DD} , and XRES are not capable of Digital I/O.

16-Pin QFN (No E-Pad)

Table 1. Pin Definitions – CY8C20236A PSoC Device

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	ECO output (XOut)
2	I/O	I	P2[3]	ECO input (XIn)
3	I/OHR	I	P1[7]	I ² C SCL, SPI SS
4	I/OHR	I	P1[5]	I ² C SDA, SPI MISO
5	I/OHR	I	P1[3]	SPI SCLK
6	I/OHR	I	P1[1]	ISSP CLK ^[3] , I ² C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection
8	I/OHR	I	P1[0]	ISSP DATA ^[3] , I ² C SDA, SPI CLK ^[4]
9	I/OHR	I	P1[2]	
10	I/OHR	I	P1[4]	Optional external clock input (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	I/OH	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	I/OH	I	P0[7]	
15	I/OH	I	P0[3]	Integrating input
16	I/OH	I	P0[1]	Integrating input

Figure 2. CY8C20236A PSoC Device



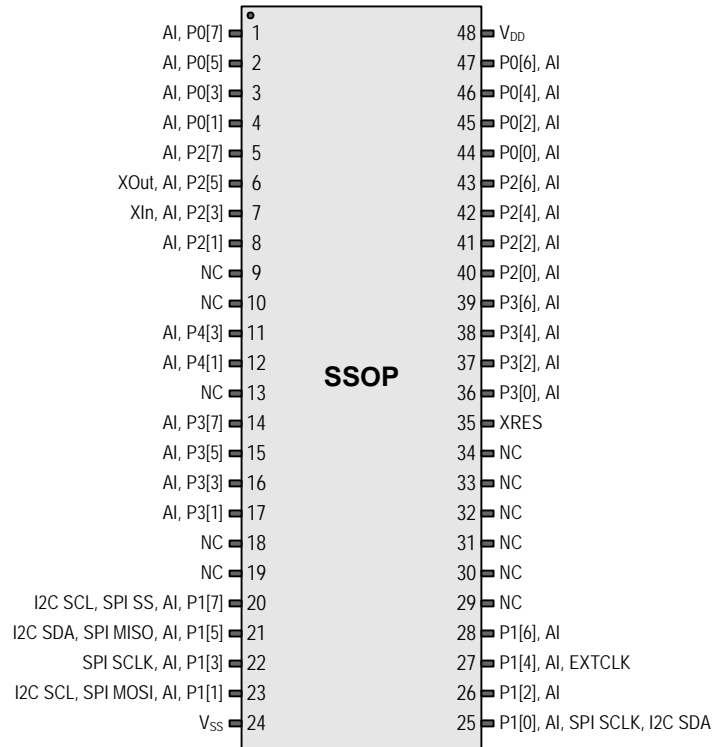
LEGEND A = Analog, I = Input, O = Output, H = 5 mA High Output Drive, R = Regulated Output.

Notes

- On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- Alternate SPI clock.

48-Pin SSOP
Table 2. Pin Definitions – CY8C20566A PSoC Device^[5]

Pin No.	Type		Name	Description
	Digi-tal	Ana-log		
1	I/OH	I	P0[7]	
2	I/OH	I	P0[5]	
3	I/OH	I	P0[3]	Integrating input
4	I/OH	I	P0[1]	Integrating input
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	ECO output (XOut)
7	I/O	I	P2[3]	ECO input (XIn)
8	I/O	I	P2[1]	
9			NC	No connection
10			NC	No connection
11	I/O	I	P4[3]	
12	I/O	I	P4[1]	
13			NC	No connection
14	I/O	I	P3[7]	
15	I/O	I	P3[5]	
16	I/O	I	P3[3]	
17	I/O	I	P3[1]	
18			NC	No connection
19			NC	No connection
20	I/OHR	I	P1[7]	I ² C SCL, SPI SS
21	I/OHR	I	P1[5]	I ² C SDA, SPI MISO
22	I/OHR	I	P1[3]	SPI CLK
23	I/OHR	I	P1[1]	ISSP CLK ^[5] , I ² C SCL, SPI MOSI
24	Power		V _{SS}	Ground connection
25	I/OHR	I	P1[0]	ISSP DATA ^[5] , I ² C SDA, SPI CLK ^[5]
26	I/OHR	I	P1[2]	
27	I/OHR	I	P1[4]	Optional external clock input (EXT CLK)
28	I/OHR	I	P1[6]	
29			NC	No connection
30			NC	No connection
31			NC	No connection
32			NC	No connection
33			NC	No connection
34			NC	No connection
35	Input		XRES	Active high external reset with internal pull-down
36	I/O	I	P3[0]	
37	I/O	I	P3[2]	
38	I/O	I	P3[4]	
39	I/O	I	P3[6]	
40	I/O	I	P2[0]	

Figure 3. CY8C20566A PSoC Device


Pin No.	Type		Name	Description
	Dig-ital	Ana-log		
41	I/O	I	P2[2]	
42	I/O	I	P2[4]	
43	I/O	I	P2[6]	
44	I/OH	I	P0[0]	
45	I/OH	I	P0[2]	
46	I/OH	I	P0[4]	
47	I/OH	I	P0[6]	
48	Power		V _{DD}	Supply voltage

LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.

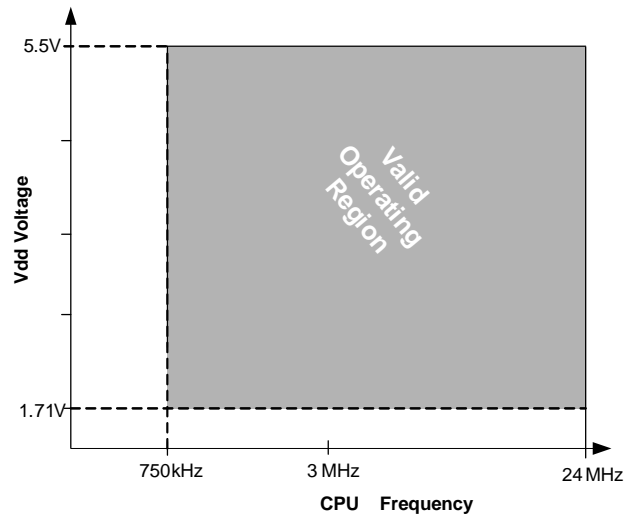
Notes

- On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- Alternate SPI clock.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x36A/66A PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at <http://www.cypress.com/psoc>.

Figure 4. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 3. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is $+25^{\circ}\text{C} \pm 25^{\circ}\text{C}$. Extended duration storage temperatures above 85°C degrades reliability.	-55	+25	+125	$^{\circ}\text{C}$
V_{DD}	Supply voltage relative to V_{SS}	—	-0.5	—	+6.0	V
V_{IO}	DC input voltage	—	$V_{SS} - 0.5$	—	$V_{DD} + 0.5$	V
V_{IOZ}	DC voltage applied to tristate	—	$V_{SS} - 0.5$	—	$V_{DD} + 0.5$	V
I_{MIO}	Maximum current into any port pin	—	-25	—	+50	mA
ESD	Electro static discharge voltage	Human body model ESD	2000	—	—	V
LU	Latch-up current	In accordance with JESD78 standard	—	—	200	mA

Operating Temperature

Table 4. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature	—	-40	—	+85	$^{\circ}\text{C}$
T_J	Operational die temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 23 . The user must limit the power consumption to comply with this requirement.	-40	—	+100	$^{\circ}\text{C}$

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 2.4 V to 3.0 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 1.71 V to 2.4 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3 V at 25 C and are for design guidance only.

Table 6. 3.0-V to 5.5-V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	k Ω
V_{OH1}	High output voltage Port 2 or 3 pins	$IOH \leq 10\ \mu\text{A}$, maximum of 10 mA source current in all I/Os	$V_{DD} - 0.20$	–	–	V
V_{OH2}	High output voltage Port 2 or 3 Pins	$IOH = 1\ \text{mA}$, maximum of 20 mA source current in all I/Os	$V_{DD} - 0.90$	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	$IOH < 10\ \mu\text{A}$, maximum of 10 mA source current in all I/Os	$V_{DD} - 0.20$	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	$IOH = 5\ \text{mA}$, maximum of 20 mA source current in all I/Os	$V_{DD} - 0.90$	–	–	V
V_{OH5}	High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out	$IOH < 10\ \mu\text{A}$, $V_{DD} > 3.1\ \text{V}$, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	$IOH = 5\ \text{mA}$, $V_{DD} > 3.1\ \text{V}$, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	$IOH < 10\ \mu\text{A}$, $V_{DD} > 2.7\ \text{V}$, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	$IOH = 2\ \text{mA}$, $V_{DD} > 2.7\ \text{V}$, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	$IOH < 10\ \mu\text{A}$, $V_{DD} > 2.7\ \text{V}$, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	$IOH = 1\ \text{mA}$, $V_{DD} > 2.7\ \text{V}$, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	$IOL = 25\ \text{mA}$, $V_{DD} > 3.3\ \text{V}$, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.80	V
V_{IH}	Input high voltage	–	2.00	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (Absolute Value)	–	–	0.001	1	μA
C_{PIN}	Pin capacitance	Package and pin dependent Temp = 25 $^{\circ}\text{C}$	0.50	1.70	7	pF

Table 8. 1.71-V to 2.4-V DC GPIO Specifications (continued)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_H	Input hysteresis voltage	—	—	80	—	mV
I_{IL}	Input leakage (absolute value)	—	—	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 9. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch resistance to common analog bus	—	—	—	800	Ω
R_{GND}	Resistance of initialization switch to V_{SS}	—	—	—	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 10. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to V_{DD}	0.0	—	1.8	V
I_{LPC}	LPC supply current	—	—	10	40	μA
V_{OSLPC}	LPC voltage offset	—	—	2.5	30	mV

Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $1.71\text{V} \leq V_{DD} \leq 5.5\text{V}$.

Table 11. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{COMP}	Comparator response time	50 mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to $V_{DD} - 0.2\text{ V}$	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	μA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range		–	0		1.5	V

ADC Electrical Specifications

Table 12. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	V_{REFADC}	V
C_{IIN}	Input capacitance	–	–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	$1/(500\text{fF} \times \text{data clock})$	$1/(400\text{fF} \times \text{data clock})$	$1/(300\text{fF} \times \text{data clock})$	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = $0.001/(2^{\text{Resolution}}/\text{Data Clock})$	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = $0.001/(2^{\text{resolution}}/\text{data clock})$	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR ($V_{DD} > 3.0\text{ V}$)	–	24	–	dB
		PSRR ($V_{DD} < 3.0\text{ V}$)	–	30	–	dB

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{POR0}	1.66 V selected in PSoC Designer	V _{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V _{POR1}	2.36 V selected in PSoC Designer		–	2.36	2.41	
V _{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	
V _{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	
V _{LVD0}	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V _{LVD1}	2.71 V selected in PSoC Designer		2.64 ^[11]	2.71	2.78	
V _{LVD2}	2.92 V selected in PSoC Designer		2.85 ^[12]	2.92	2.99	
V _{LVD3}	3.02 V selected in PSoC Designer		2.95 ^[13]	3.02	3.09	
V _{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V _{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	
V _{LVD6}	1.80 V selected in PSoC Designer		1.75 ^[14]	1.80	1.84	
V _{LVD7}	4.73 V selected in PSoC Designer		4.62	4.73	4.83	

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{DDIWRITE}	Supply voltage for flash write operations	–	1.71	–	5.25	V
I _{DDP}	Supply current during programming or verify	–	–	5	25	mA
V _{ILP}	Input low voltage during programming or verify	See the appropriate DC GPIO Specifications on page 11	–	–	V _{IL}	V
V _{IHP}	Input high voltage during programming or verify	See appropriate DC GPIO Specifications on page 11 table on pages 15 or 16	V _{IH}	–	–	V
I _{ILP}	Input current when Applying V _{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I _{IHP}	Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V _{OLP}	Output low voltage during programming or verify		–	–	V _{SS} + 0.75	V
V _{OHP}	Output high voltage during programming or verify	See appropriate DC GPIO Specifications on page 11 table on page 16. For V _{DD} > 3V use V _{OH4} in Table 4 on page 9 .	V _{OH}	–	V _{DD}	V
Flash _{ENPB}	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
Flash _{DR}	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

Notes

11. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
12. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
13. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
14. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{IMO24}	Internal main oscillator frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F _{IMO12}	Internal main oscillator frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F _{IMO6}	Internal main oscillator frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F _{CPU}	CPU frequency	–	0.75	–	25.20	MHz
F _{32K1}	Internal low speed oscillator frequency	–	19	32	50	kHz
F _{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency)	–	13	32	82	kHz
DC _{IMO}	Duty cycle of IMO	–	40	50	60	%
DC _{ILO}	Internal low speed oscillator duty cycle	–	40	50	60	%
SR _{POWER_UP}	Power supply slew rate	V _{DD} slew rate during power-up	–	–	250	V/ms
t _{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t _{XRST2}	External reset pulse width after power-up ^[15]	Applies after part has booted	10	–	–	μs

Note

15. The minimum required XRES pulse length is longer when programming the device (see [Table 19 on page 18](#)).

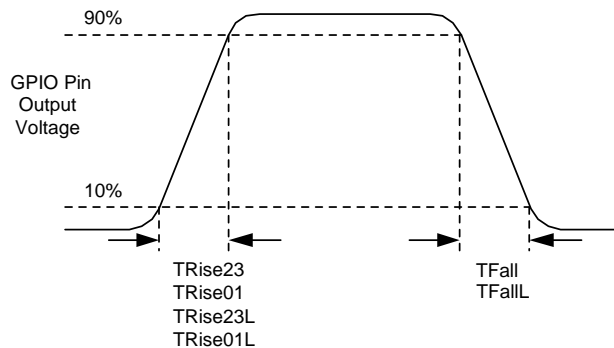
AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode Port 0, 1	0	–	6 MHz for $1.71\text{ V} < V_{DD} < 2.40\text{ V}$	MHz
			0	–	12 MHz for $2.40\text{ V} < V_{DD} < 5.50\text{ V}$	MHz
t_{RISE23}	Rise time, strong mode, Cload = 50 pF Ports 2 or 3	$V_{DD} = 3.0\text{ to }3.6\text{ V}$, 10% to 90%	15	–	80	ns
$t_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, Ports 2 or 3	$V_{DD} = 1.71\text{ to }3.0\text{ V}$, 10% to 90%	15	–	80	ns
t_{RISE01}	Rise time, strong mode, Cload = 50 pF Ports 0 or 1	$V_{DD} = 3.0\text{ to }3.6\text{ V}$, 10% to 90% LDO enabled or disabled	10	–	50	ns
$t_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1	$V_{DD} = 1.71\text{ to }3.0\text{ V}$, 10% to 90% LDO enabled or disabled	10	–	80	ns
t_{FALL}	Fall time, strong mode, Cload = 50 pF all ports	$V_{DD} = 3.0\text{ to }3.6\text{ V}$, 10% to 90%	10	–	50	ns
t_{FALLL}	Fall time, strong mode low supply, Cload = 50 pF, all ports	$V_{DD} = 1.71\text{ to }3.0\text{ V}$, 10% to 90%	10	–	70	ns

Figure 5. GPIO Timing Diagram



AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{LPC}	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency (external oscillator frequency)	–	0.75	–	25.20	MHz
	High period	–	20.60	–	5300	ns
	Low period	–	20.60	–	–	ns
	Power-up IMO to switch	–	150	–	–	μs

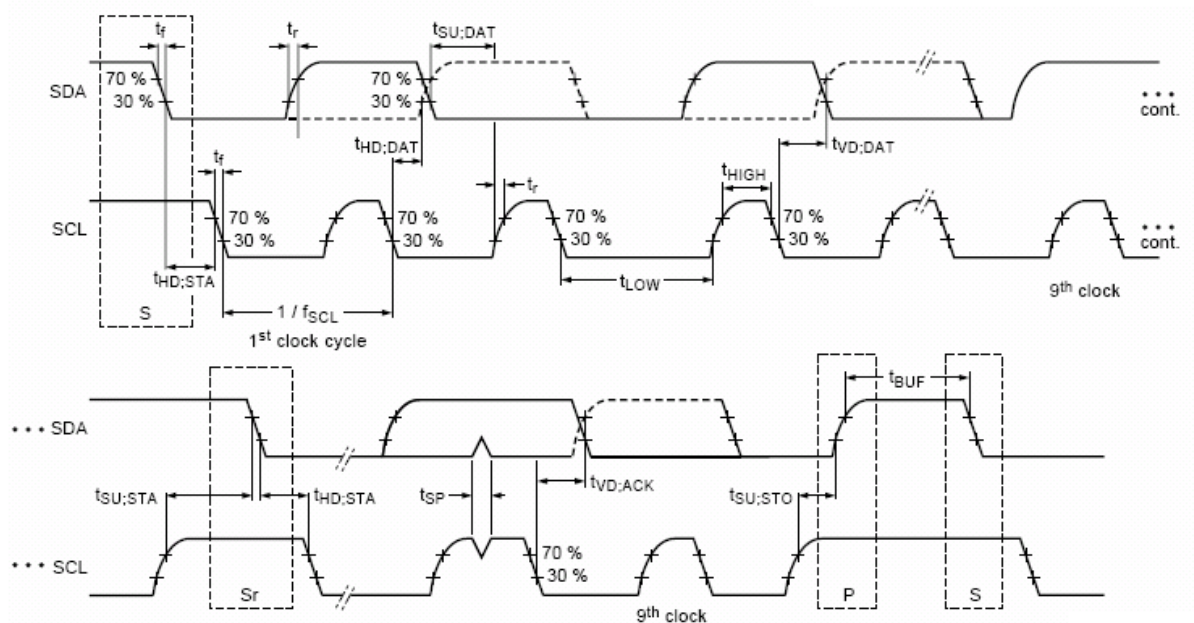
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	—	0.6	—	μ s
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	μ s
t_{HIGH}	HIGH Period of the SCL clock	4.0	—	0.6	—	μ s
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	—	0.6	—	μ s
$t_{HD;DAT}$	Data hold time	0	3.45	0	0.90	μ s
$t_{SU;DAT}$	Data setup time	250	—	100 ^[16]	—	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	—	0.6	—	μ s
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	μ s
t_{SP}	Pulse width of spikes are suppressed by the input filter	—	—	0	50	ns

Figure 7. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

16. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Table 21. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4 \text{ V}$ $V_{DD} < 2.4 \text{ V}$	— —	— —	6 3	MHz MHz
DC	SCLK duty cycle	—	—	50	—	%
t_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 2.4 \text{ V}$ $V_{DD} < 2.4 \text{ V}$	60 100	— —	— —	ns ns
t_{HOLD}	SCLK to MISO hold time	—	40	—	—	ns
t_{OUT_VAL}	SCLK to MOSI valid time	—	—	—	40	ns
t_{OUT_HIGH}	MOSI high time	—	40	—	—	ns

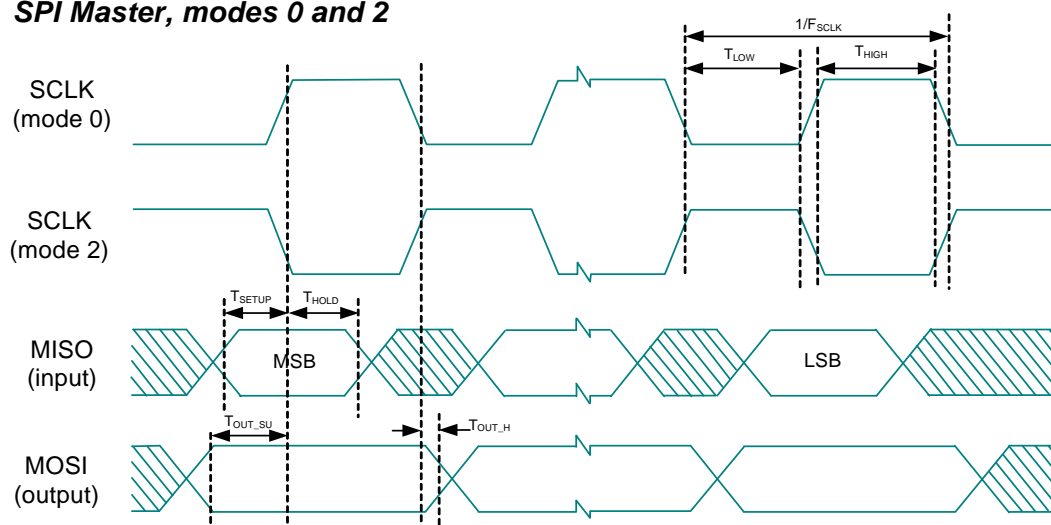
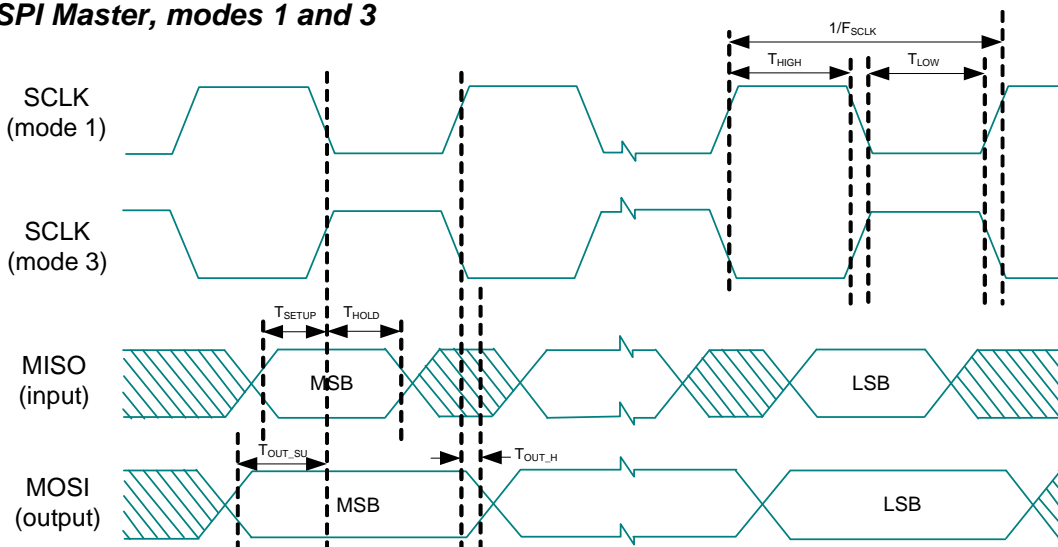
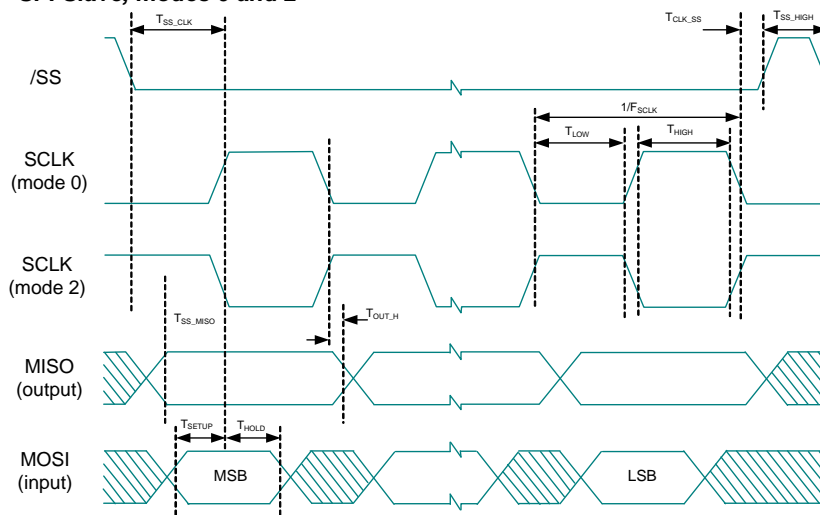
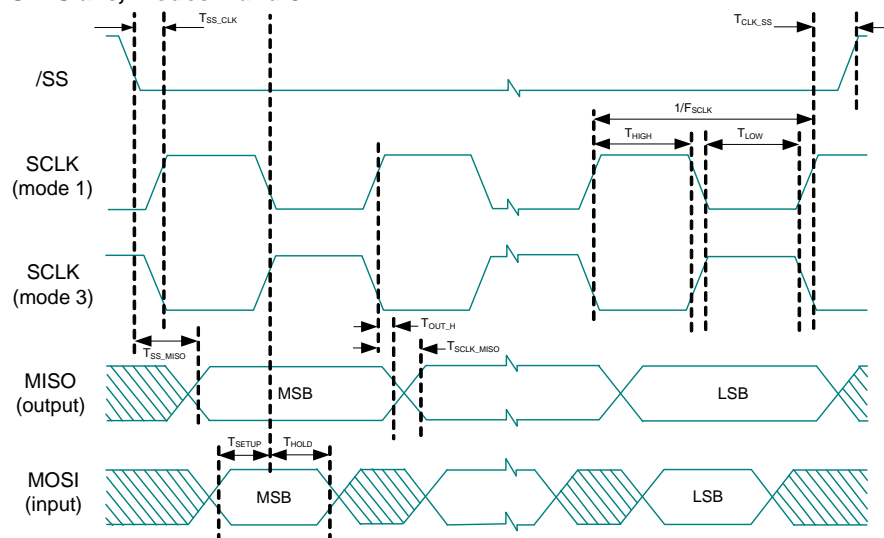
Figure 8. SPI Master Mode 0 and 2
SPI Master, modes 0 and 2

Figure 9. SPI Master Mode 1 and 3
SPI Master, modes 1 and 3


Table 22. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4 \text{ V}$ $V_{DD} < 2.4 \text{ V}$	— —	— —	12 6	MHz MHz
t_{LOW}	SCLK low time	—	42	—	—	ns
t_{HIGH}	SCLK high time	—	42	—	—	ns
t_{SETUP}	MOSI to SCLK setup time	—	30	—	—	ns
t_{HOLD}	SCLK to MOSI hold time	—	50	—	—	ns
t_{SS_MISO}	SS high to MISO valid	—	—	—	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	—	—	—	125	ns
t_{SS_HIGH}	SS high time	—	50	—	—	ns
t_{SS_CLK}	Time from SS low to first SCLK	—	$2/SCLK$	—	—	ns
t_{CLK_SS}	Time from last SCLK to SS high	—	$2/SCLK$	—	—	ns

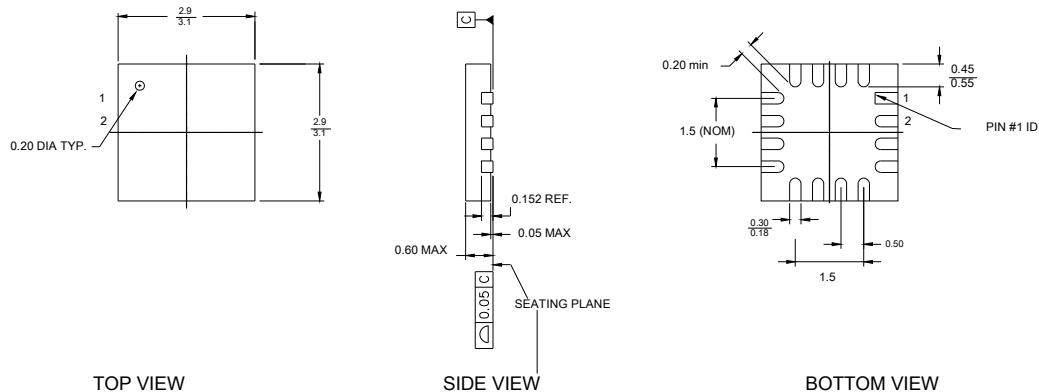
Figure 10. SPI Slave Mode 0 and 2
SPI Slave, modes 0 and 2

Figure 11. SPI Slave Mode 1 and 3
SPI Slave, modes 1 and 3


Packaging Information

This section illustrates the packaging specifications for the CY8C20x36A/66A PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at <http://www.cypress.com>.

Figure 12. 16-pin QFN No E-pad 3x3x0.6 mm Package Outline (Sawn)



PART NO.	DESCRIPTION
LG16A	LEAD-FREE
LD16A	STANDARD

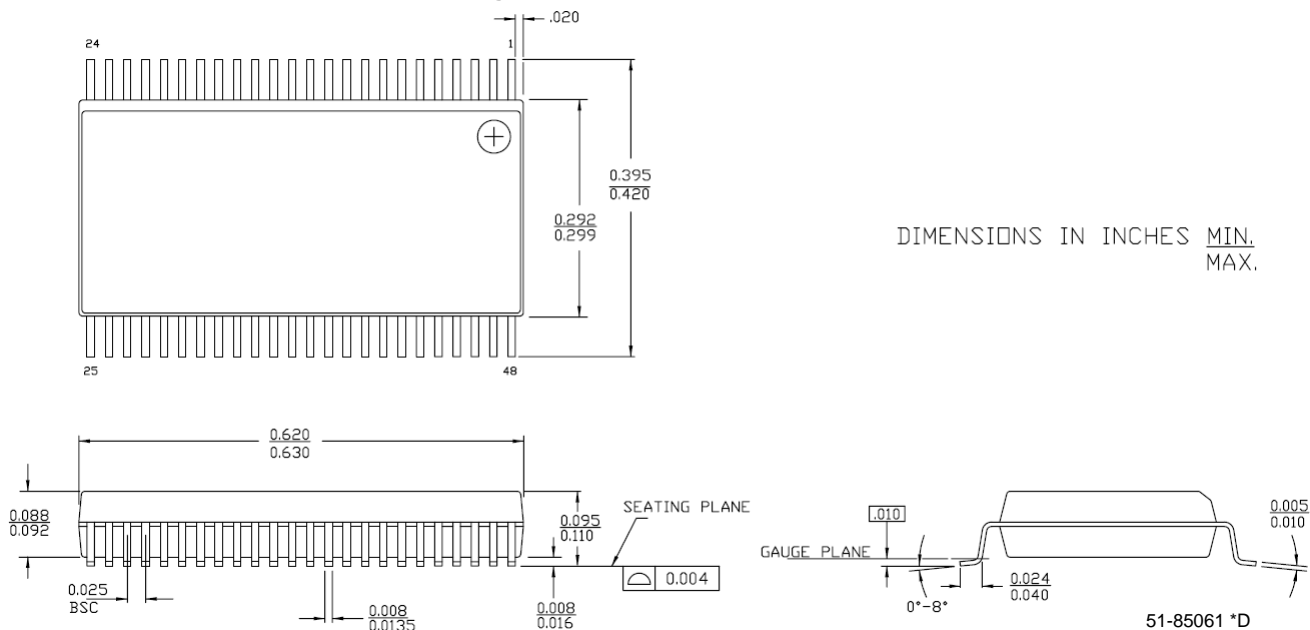
NOTES:

1. JEDEC # MO-220
2. Package Weight 0.014g
3. DIMENSIONS IN MM, MIN

MAX

001-09116 *E

Figure 13. 48-Pin (300-Mil) SSOP



Important Note For information on the preferred dimensions for mounting QFN packages, refer to Application Note, Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages available at <http://www.amkor.com>.

Thermal Impedances

Table 23. Thermal Impedances per Package

Package	Typical θ_{JA} ^[17]
16-pin QFN	33 °C/W
48-pin SSOP	69 °C/W

Solder Reflow Specifications

Table 24 shows the solder reflow temperature limits that must not be exceeded.

Table 24. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above $T_C - 5$ °C
16-pin QFN	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds

Note

17. $T_J = T_A + \text{Power} \times \theta_{JA}$.

Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at <http://www.cypress.com>. PSoC Designer comes with a free C compiler.

PSoC Designer Software Subsystems

You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. Code Generation Tools PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the

capability to program single devices. The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24MHz) operation.

Standard Cypress PSoC IDE tools are available for debugging the CY8C20x36A/66A family of parts. However, the additional trace length and a minimal ground plane in the Flex-Pod can create noise problems that make it difficult to debug the design. A custom bonded On-Chip Debug (OCD) device is available in a 48-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and is connected to the ICE through a high density connector.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com/psocprogrammer>.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The **CY3215-DK** is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66A Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466A-24PXI 28-PDIP Chip Samples

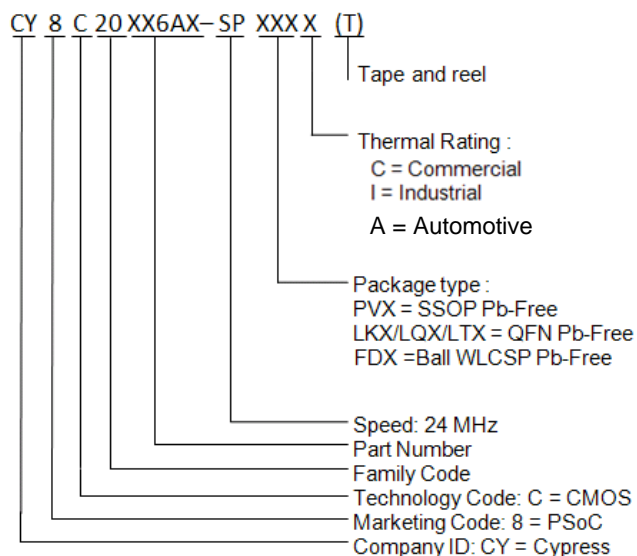
Ordering Information

The following table lists the CY8C20x36A/66A PSoC devices' key package features and ordering codes..

Table 26. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs ^[21]	XRES Pin	USB	ADC
16-Pin (3 × 3 × 0.6 mm) QFN	CY8C20236A-24LKXA	8 K	1 K	1	13	13	Yes	No	Yes
16-Pin (3 × 3 × 0.6 mm) QFN (Tape and Reel)	CY8C20236A-24LKXAT	8 K	1 K	1	13	13	Yes	No	Yes
48-Pin SSOP	CY8C20566A-24PVXA	32 K	2 K	1	34	34	Yes	No	Yes
48-Pin SSOP (Tape and Reel)	CY8C20566A-24PVXAT	32 K	2 K	1	34	34	Yes	No	Yes

Ordering Code Definitions



Note

21. Dual-function Digital I/O Pins also connect to the common analog mux.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

Glossary

Crosspoint connection	Connection between any GPIO combination via analog multiplexer bus.
Differential non-linearity	Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step.
Hold time	Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.
I ² C	It is a serial multi-master bus used to connect low speed peripherals to MCU.
Integral nonlinearity	It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level.
Latch-up current	Current at which the latch-up test is conducted according to JESD78 standard (at 125 degree celsius)
Power supply rejection ratio (PSRR)	The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device.
Scan	The conversion of all sensor capacitances to digital values.
Setup time	Period required to prepare a device, machine, process, or system for it to be ready to function.
Signal-to-noise ratio	The ratio between a capacitive finger signal and system noise.
SPI	Serial peripheral interface is a synchronous serial data link standard.