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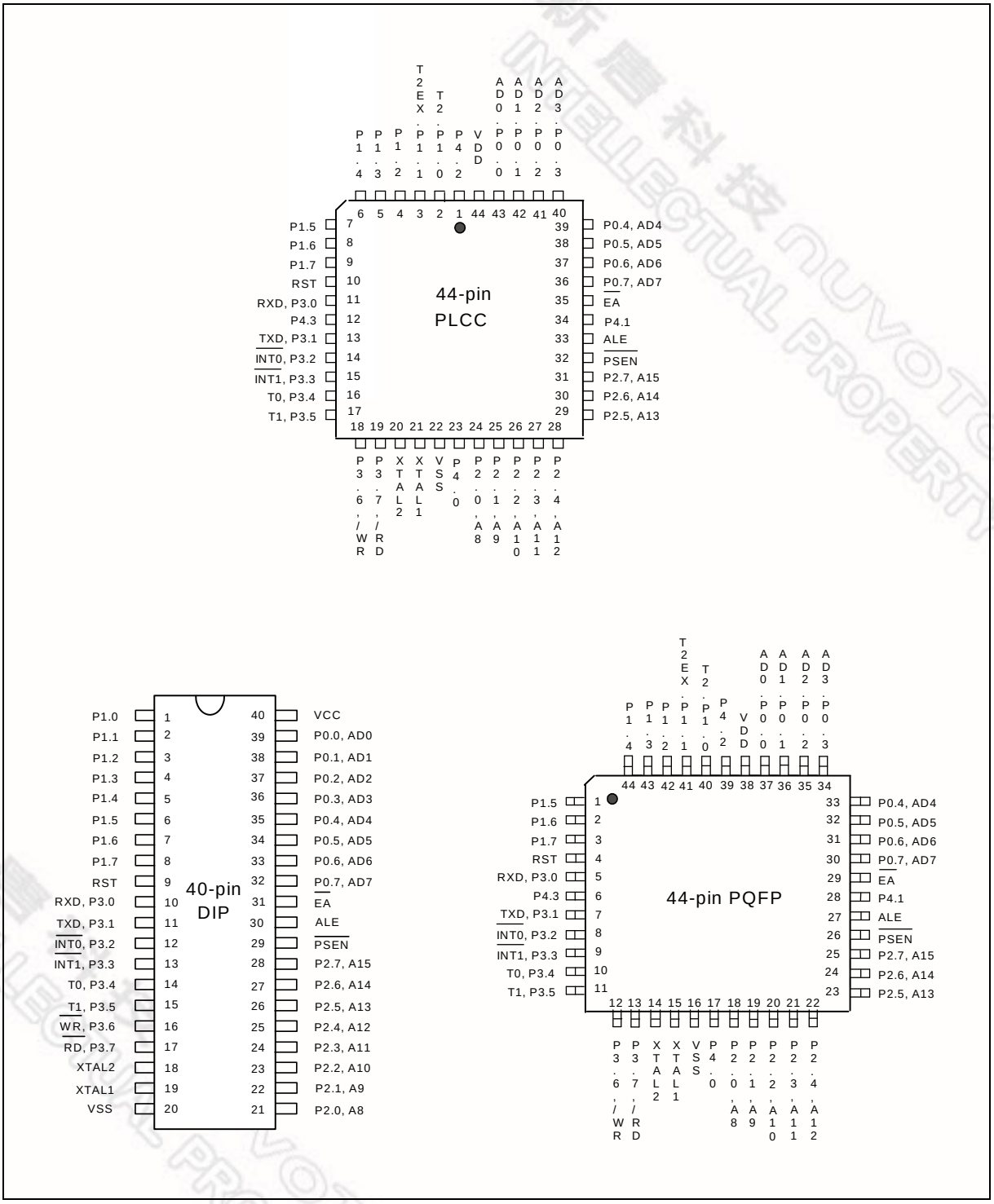
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e858a40fl

3. PIN CONFIGURATIONS



4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	**External Access Enable:** $\overline{EA}$ low forces the processor to execute the external ROM. The ROM address and data will not be present on the bus if the $\overline{EA}$ pin is high and the program counter is within the 32 KB area. Otherwise they will be present on the bus.
$\overline{PSEN}$	O/H	**Program Strobe Enable:** $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O/H	**Address Latch Enable:** ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. An ALE pulse is omitted during external data memory accesses.
RST	I/L	**RESET:** A high on this pin for two machine cycles while the oscillator is running resets the device. RST has a Schmitt trigger input stage to provide additional noise immunity with a slow rising input voltage.
XTAL1	I	**Crystal 1:** This is the crystal oscillator input. This pin may be driven by an external clock
XTAL2	O	**Crystal 2:** This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	I	**Ground:** Ground potential.
V_{DD}	I	**Power Supply:** Supply voltage for operation.
P0.0 – P0.7	I/O D	**Port 0:** Function is the same as that of the standard 8052.
P1.0 – P1.7	I/O H	**Port 1:** Function is the same as that of the standard 8052. Port1 also service the alternative function INT2 – INT9. P1.0 provide a timer2 programmable clock output. Four channel PWM clock output via P1.4 – P1.7
P2.0 – P2.7	I/O H	**Port 2:** Port 2 is a bi-directional I/O port with internal pull-ups and emits the high-order address byte during accesses external memory
P3.0 – P3.7	I/O H	**Port 3:** Function is the same as that of the standard 8052
P4.0 – P4.3	I/O H	**Port 4:** Function is the same as Port1

* **Note:** TYPE I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

5. FUNCTIONAL DESCRIPTION

The W78E858 architecture consists of a core controller surrounded by various registers, four 8-bit general purpose I/O ports, one 4-bits general purpose I/O port, 256 bytes data RAM and 512 bytes auxiliary RAM, 128 bytes embedded EEPROM memory, three timer/counters, one serial port, 17-bit watch-dog timer, 8-bit four channels PWM, programmable timer2 clock output, extra external interrupts INT2 to INT9, power-down wake up via external interrupts INT0 – INT9. The CPU supports 111 different op-codes and references both a 64K program address space and a 64 K data storage space.

5.1 RAM

The internal data RAM in W78E858 is 768 bytes. It is divided into two banks: 256 bytes of data RAM and 512 bytes of auxiliary RAM. These RAM are addressed by different ways.

- RAM 00H – 7FH can be addressed directly and indirectly as the same as in 80C51. Address pointers are R0 and R1 of the selected register bank.
- RAM 80H – FFH can only be addressed indirectly as the same as in 80C51. Address pointers are R0, R1 of the selected registers bank.
- Auxiliary RAM 0000H – 01FFH is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointers are R0 and R1 of the selected register bank and DPTR register. By setting ENAUXRAM flag in CHPCON register bit4 to enable on-chip auxiliary RAM 512 bytes. When the auxiliary RAM is enabled, the data and address will not appear on P0 and P2, they will keep their previous status that before the MOVX instruction be executed. Write the page select 00H or 01H to MXPSR register if R0 and R1 are used as address pointer. When the address of external data memory locations higher than 01FFH or disable auxiliary RAM 512 bytes micro-controller will be performed with the MOVX instruction in the same way as in the 80C51. The auxiliary RAM 512 bytes default is disabled after chip reset.

5.2 EEPROM

The 128 bytes EEPROM is defined in external data memory space that located in FF80H-FFFFH in standard 8-bit series. It is accessed the same as auxiliary RAM512 bytes, the ENEEPROM flag in CHPCON register bit5 is set. Write the page select 02H to MXPSR register, R0 and R1are used as address pointer. The EEPROM provided byte write, page write mode and software write protection is used to protect the data lose when power on or noise. They are described as below:

5.2.1 Byte Write Mode

Once a byte write has been started, it will automatically time itself to completion. A BUSY signal (MXPSR.7) will be used to detect the end of write operation.

5.2.2 Page Write Mode

The EEPROM is divided into 2 pages and each page contains 64 bytes. The page write allows one to 64 bytes of data to be written into the memory during a single internal programming cycle. Page write is initiated in the same manner as byte write mode. After the first byte is written, it can then be followed by one to 63 additional bytes. If a second byte is written within a byte-load cycle time (TBLC) of 150us, the EEPROM will stay at page load cycle. Additional bytes can then be loaded consecutively. The page load cycle will be terminated and the internal programming cycle will start if no additional byte is load within 300us from the last byte be loaded. The address bit6 specify the page address. All bytes that are loaded to the buffer must have the same page address. The data for page write may be loaded in any order, the sequential loading is not required.

```
        org     0000h
                jmp     start

                org     500h
start:
                mov     chpenr,#87h
                mov     chpenr,#59h
                orl     chpcon,#00100000b       ; enable eeprom
                mov     chpenr,#00h
                call    enable_protect
                mov     dptr,#EEPROM_BASE
                mov     r0,#40h                 ; only write up to 64
byte/page. Write from FF80h to FFBFh.
                mov     r1,#55h                 ; write 55 data.
                call    write_eeprom_block
                call    enable_protect          ; Call it before writing
                mov     dptr,#EEPROM_BASE+40h
                mov     r0,#40h                 ; Write from FFC0h to FFFFh
address.
                mov     r1,#55h
                call    write_eeprom_block

                mov     dptr,#EEPROM_BASE
                mov     r0,#80h
                mov     r1,#55h
                call    read_eeprom_block
                jc      $error

                mov     chpenr,#87h
                mov     chpenr,#59h
                anl     chpcon,#11011111b       ; disable eeprom
                mov     chpenr,#00h
                clr     c
                jmp     $end
$error:
                mov     chpenr,#87h
                mov     chpenr,#59h
                anl     chpcon,#11011111b       ; disable eeprom
                mov     chpenr,#00h
                setb    c
$end:
                sjmp    $
;---------------------------------------------------------------------
disable_protect:
                mov     dptr,#EEPROM_BASE+55h
                mov     a,#aah
                movx    @dptr,a
                mov     dptr,#EEPROM_BASE+2ah
                mov     a,#55h
                movx    @dptr,a
                mov     dptr,#EEPROM_BASE+55h
                mov     a,#80h
                movx    @dptr,a
                mov     dptr,#EEPROM_BASE+55h
```

```
write_eeprom_block:
;input r0:counter
;input r1:pattern form
;input dptr:eeprom base address
$write_loop:
                mov     a,r1
                movx    @dptr,a
                inc     dpl
                djnz    r0,$write_loop
                call    busy_waiting
                ret
;---------------------------------------------------------------
read_eeprom_block:
;input r0:counter
;input r1:pattern form
;input dptr:eeprom base address
;output setb c --> fail
                push    b
$read_loop:
                movx    a,@dptr
                mov     b,a
                mov     a,r1
                cjne    a,b,$error
                inc     dpl
                djnz    r0,$read_loop
                clr     c
                jmp     $end
$error:
                setb    c
$end:
                pop     b
                ret
                .end
```

5.4 On-chip Flash EPROM

The W78E858 includes two banks of FLASH EPROM. One is 32K bytes of main FLASH EPROM for application program (APROM) and another 4K bytes of FLASH EPROM for loader program (LDROM) when operating the in-system programming feature. In normal operation, the micro-controller will execute the code from the 32K bytes of APROM. By setting program registers, user can force CPU to switch to the programming mode which will execute the code (loader program) from the 4K bytes of auxiliary LDROM, and this loader program is going to update the contents of the 32K bytes of APROM. After chip reset, the micro-controller executes the new application program in the APROM. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible that end-user is able to easily update the system firmware by themselves without opening the chassis.

5.5 Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

5.6 Clock

The W78E858 is designed to use with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78E858 relatively insensitive to duty cycle variations in the clock.

5.7 Crystal Oscillator

The W78E858 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

5.8 External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5 volts.

5.9 Power Management

5.9.1 Idle Mode

The CPU will enter to idle by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

5.9.2 Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks, including the oscillator are stopped. There are two ways to exit power-down mode, one is by a chip reset and another is via external interrupts wake up if the related control flags are enabled.

5.11 Pulse Width Modulator System

The pulse width modulator system of W78E858 contains four PWM output channels with a common 8-bit counter. These channels generate pulses of programmable length and interval. The prescaler and counter are common to four PWM channels.

5.11.1 PWMCON (91H)

BIT	NAME	FUNCTION
7 – 4	-	Reverse
3	PWM3	Enable P1.7 as PWM clock output.
2	PWM2	Enable P1.6 as PWM clock output.
1	PWM1	Enable P1.5 as PWM clock output.
0	PWM0	Enable P1.4 as PWM clock output.

5.11.2 PWMP (92H)

The prescaler is loaded with the complement of the PWMP register during counter overflow. The repetition frequency is defined by 8-bit prescaler which clocks the counter. The prescaler division factor = (PWMP + 1). Reading the PWMP gives the current reload value. The actual count of the prescaler can't be read.

The PWM counter is enabled with any bit PWMENn (n = 0, 1, 2, 3) of the PWMCON register. Output to the port pin is separately enabled by setting the PWMENn bits in the PWMCON register. The PWM function is reset by a chip reset. In idle mode, the PWM will function as configurated in PWMCON. In power-down state of the PWM will freeze when the internal clock stops. If the chip is awakened with an external interrupt, the PWM will continue to function its state when power-down was entered.

The repetition frequency is given by:

$$Fpwm = \frac{Fosc}{[255 \times (1+PWMP)]}$$

An oscillator frequency of 24 MHz results in a repetition range of 367.65 Hz to 94.12 KHz. The high/low ratio of PWMn is DACn/(255-DACn) for DACn values except 255. A DACn value 255 results in a high PWMn output.

5.16 External Interrupts INT2 to INT9

Port1 lines serve an alternative purpose at eight additional interrupts INT2 to INT9. When enabled, each of these lines may "wake-up" the device from power-down mode. Using the IX1 register, the each pin may be initialized to either active HIGH or LOW. IRQ1 is the interrupt request flag register. Each flag, if the interrupt is enabled will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disable.

The Port1 interrupts are level sensitive. A Port1 interrupt will be recognized when a level (HIGH or LOW depending on Interrupt Polarity Register IX1) on P1.x is held active for at least one machine cycle. The interrupt request is not served until the next machine cycle.

5.16.1 IE_1 (E8H)

BIT	NAME	FUNCTION
7	EX9	Enable external interrupt 9
6	EX8	Enable external interrupt 8
5	EX7	Enable external interrupt 7
4	EX6	Enable external interrupt 6
3	EX5	Enable external interrupt 5
2	EX4	Enable external interrupt 4
1	EX3	Enable external interrupt 3
0	EX2	Enable external interrupt 2

5.16.2 IP1 (F8H)

BIT	NAME	FUNCTION
7	PX9	External interrupt 9 priority level
6	PX8	External interrupt 8 priority level
5	PX7	External interrupt 7 priority level
4	PX6	External interrupt 6 priority level
3	PX5	External interrupt 5 priority level
2	PX4	External interrupt 4 priority level
1	PX3	External interrupt 3 priority level
0	PX2	External interrupt 2 priority level

5.16.3 IX1 (E9H)

BIT	NAME	FUNCTION
7	IL9	External interrupt 9 polarity level
6	IL8	External interrupt 8 polarity level
5	IL7	External interrupt 7 polarity level
4	IL6	External interrupt 6 polarity level
3	IL5	External interrupt 5 polarity level
2	IL4	External interrupt 4 polarity level
1	IL3	External interrupt 3 polarity level
0	IL2	External interrupt 2 polarity level

5.16.4 IRQ1 (C0H)

BIT	NAME	FUNCTION
7	IQ9	External interrupt 9 request flag
6	IQ8	External interrupt 8 request flag
5	IQ7	External interrupt 7 request flag
4	IQ6	External interrupt 6 request flag
3	IQ5	External interrupt 5 request flag
2	IQ4	External interrupt 4 request flag
1	IQ3	External interrupt 3 request flag
0	IQ2	External interrupt 2 request flag

5.16.5 Interrupt Priority and Vector Address

PRIORITY	INTERRUPT	VECTOR	SOURCE	PRIORITY	INTERRUPT	VECTOR	SOURCE
1	INT0	0003H	External 0	8	TF1	001BH	Timer 1
2	INT5	0053H	External 5	9	SINT	0023H	UART
3	TF0	000BH	Timer 0	10	TF2	002BH	Timer 2
4	INT6	005BH	External 6	11	INT3	0043H	External 3
5	INT1	0013H	External 1	12	INT8	006BH	External 8
6	INT2	003BH	External 2	13	INT4	004BH	External 4
7	INT7	0063H	External 7	14	INT9	0073H	External 9

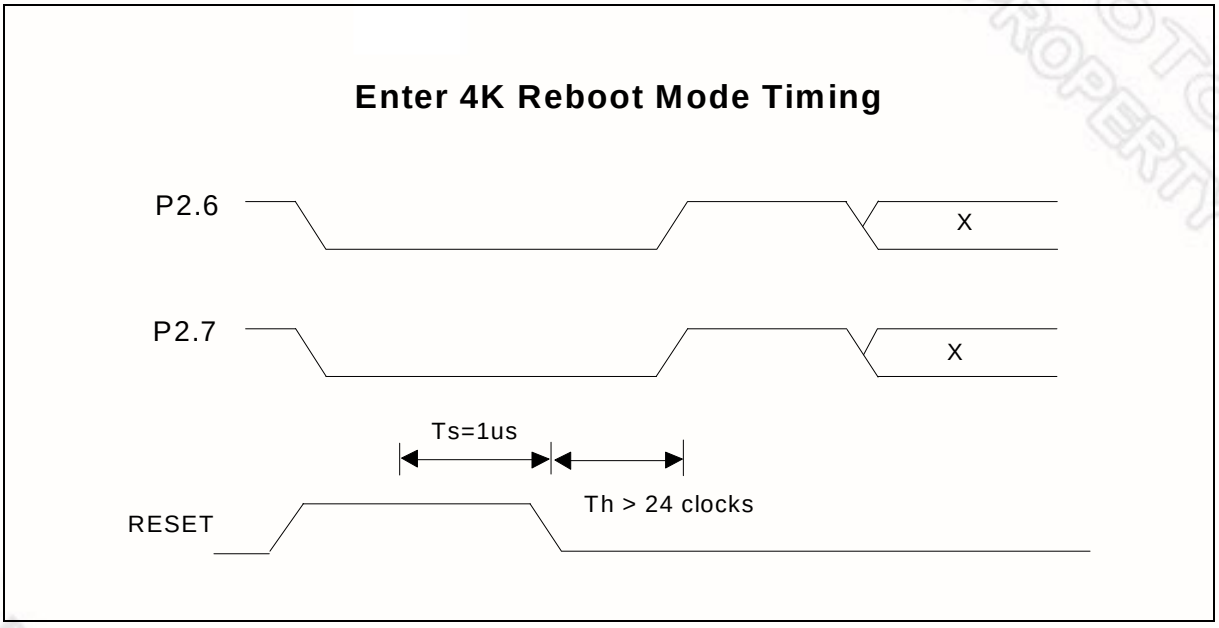
5.17 F04KBOOT Mode (Boot From 4K Bytes LDROM)

The W78E858 boots from APROM program (32K bytes bank) by default after chip reset. On some occasions, user can force the W78E858 to boot from the LDROM program (4K bank) after chip reset. The setting for this special mode is as follow.

5.17.1 F04KBOOT Mode

RST	P4.3	P2.7	P2.6	MODE
H↓	X	L	L	FO4KBOOT
H↓	L	X	X	FO4KBOOT

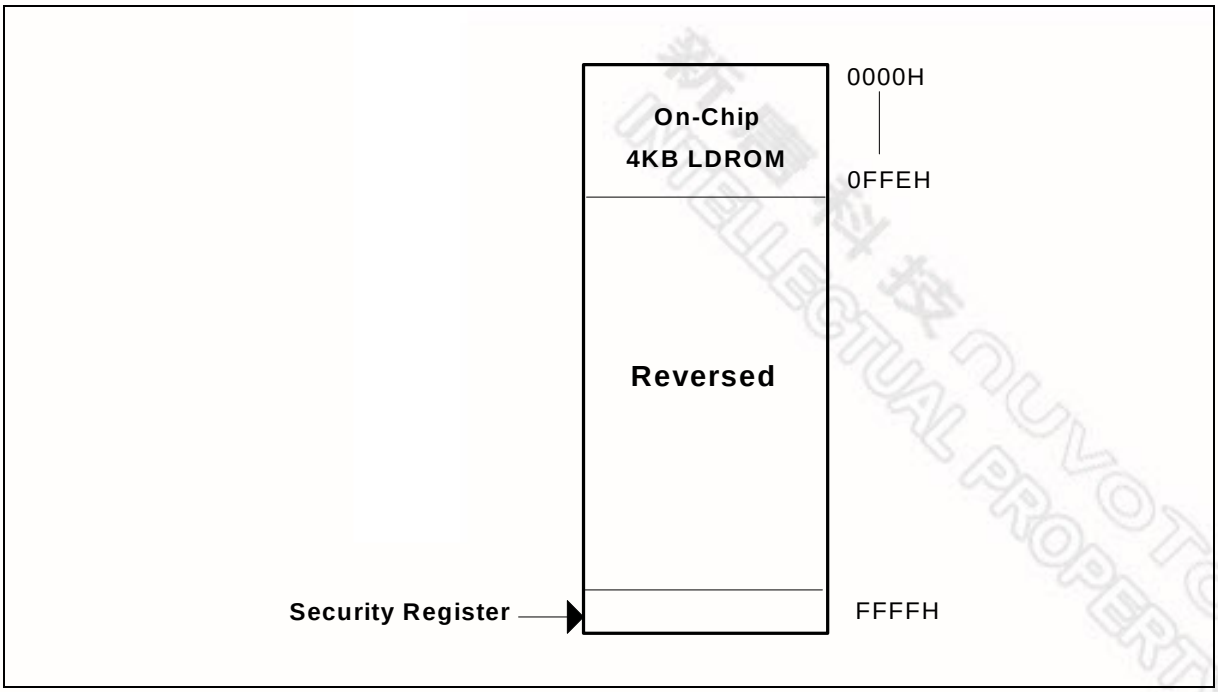
Note: In application system design, user must take care the P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ pin status at reset to avoid W78E858 entering the programming mode or F04KBOOT mode in normal operation.



5.18 Security

During the on-chip FLASH EPROM programming mode, the FLASH EPROM can be programmed and verified repeatedly. Until the code inside the FLASH EPROM is confirmed OK, the code can be protected. The protection of FLASH EPROM and those operations on it are described below:

The W78E858 has several special setting registers in FLASH EPROM block. Those bits of the security register can't be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The security register is located at the FFFFH on the same bank with 4K LDROM i.e., P3.6 must set high at writer mode.



5.18.1 Lock Bit (Bit0)

This bit is used to protect the customer's program code in the W78E858. It may be set after the programmer finishes the programming and verifies sequence. Once these bits are set to logic 0, both the FLASH EPROM data and all data in FLASH EPROM block can't be accessed again.

5.18.2 MOVC Lock (Bit1)

When this bit is program to "0", the MOVC instruction will be disable when the program counter more than 7FFFh or $\overline{EA}$ pin is forced low.

5.18.3 Scramble Enable (Bit2)

This bit is used to protect the customer's program code in the W78E858. If this bit is set to logic 0, the dump ROM code are scrambled by a scramble circuit and the dump ROM code will become a random ROM code.

5.18.4 Oscillator Gain Select (Bit7)

If this bit is set to logic 0 (for 24 MHz), the EMI effect will be reduce. If this bit is set to logic 1 (for 40 MHz), the W78E858 could to use 40 MHz crystal, but the EMI effect is major. So we provide the option bit which could be chose by customer.

5.19 Watch Dog Timer

For more system reliability, W78E858 provides a programmable watch-dog time-out reset function. From programming prescaler select, user can choose a variable prescaler from divided by 2 to divided by 256 to get a suitable time-out period. The time-out period is given by:

$$T_{time\text{-}out} = \frac{1}{Fosc} \times 2^{14} \times PRESCALER \times 1000 \times 12 \ (mS)$$

(Note: Fosc unit = Hz)

5.19.1 WDTC (8FH)

BIT	NAME	FUNCTION
7	ENW	Enable watch-dog timer if set.
6	CLRW	Clear watch-dog timer and prescaler if set. This flag will be cleared auto-matically.
5	WIDL	If this bit is set, watch-dog is enabled under idle mode. If cleared, watch-dog is disable under idle mode. Default is cleared.
4 – 3	-	Reversed.
2	PS2	Watch-dog prescaler timer select.
1	PS1	Watch-dog prescaler timer select.
0	PS0	Watch-dog prescaler timer select.

PS2	PS1	PS0	PRESCALER SELCET	WATCH-DOG TIME-OUT PERIOD (Fosc = 20 MHz)
0	0	0	2	19.66 mS
0	1	0	4	39.32 mS
0	0	1	8	78.64 mS
0	1	1	16	157.28 mS
1	0	0	32	314.57 mS
1	0	1	64	629.14 mS
1	1	0	128	1.25 mS
1	1	1	256	2.52 mS

D.C. Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage XTAL1[*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4 mA
Sink Current P1, P3, P4	I_{SK1}	4	12	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Sink Current P0, P2, ALE, $\overline{PSEN}$	I_{SK2}	10	20	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 μA
Source Current P1, P2, P3, P4	I_{SR1}	-120	-250	μA	V_{DD} = 4.5V V_{IN} = 2.4V (latch)
Source Current P0, P2, ALE, $\overline{PSEN}$	I_{SR2}	-8	-20	mA	V_{DD} = 4.5V V_{IN} = 2.4V

Notes:

*1. RST pin is a Schmitt trigger input.

*3. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

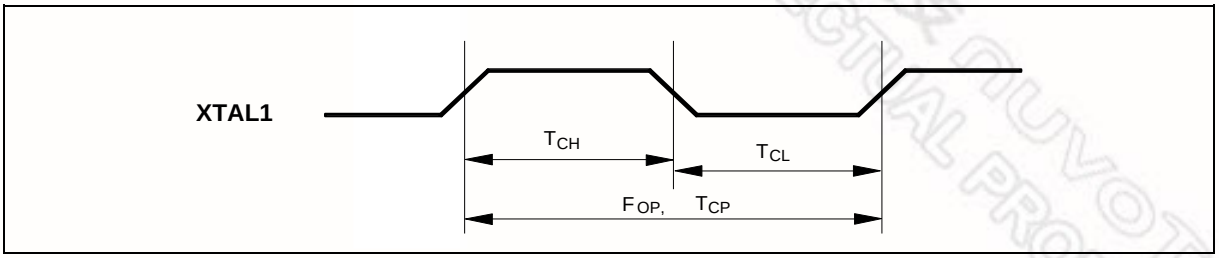
*4. XTAL1 is a CMOS input.

*5. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} approximates to 2V.

6.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

6.3.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	40	MHz	1
Clock Period	T_{CP}	25	-	-	nS	2
Clock High	T_{CH}	10	-	-	nS	3
Clock Low	T_{CL}	10	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

6.3.2 Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	T_{AAS}	1 T_{CP}-Δ	-	-	nS	4
Address Hold from ALE Low	T_{AAH}	1 T_{CP}-Δ	-	-	nS	1, 4
ALE Low to $\overline{PSEN}$ Low	T_{APL}	1 T_{CP}-Δ	-	-	nS	4
$\overline{PSEN}$ Low to Data Valid	T_{PDA}	-	-	2 T_{CP}	nS	2
Data Hold after $\overline{PSEN}$ High	T_{PDH}	0	-	1 T_{CP}	nS	3
Data Float after $\overline{PSEN}$ High	T_{PDZ}	0	-	1 T_{CP}	nS	
ALE Pulse Width	T_{ALW}	2 T_{CP}-Δ	2 T_{CP}	-	nS	4
$\overline{PSEN}$ Pulse Width	T_{PSW}	3 T_{CP}-Δ	3 T_{CP}	-	nS	4

Notes:
1. P0.0 – P0.7, P2.0 – P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 T_{CP}.
3. Data have been latched internally prior to $\overline{PSEN}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

6.3.3 Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	Tdar	3 TCP-Δ	-	3 TCP+Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	Tdda	-	-	4 TCP	nS	1
Data Hold from $\overline{RD}$ High	Tddh	0	-	2 TCP	nS	
Data Float from $\overline{RD}$ High	Tddz	0	-	2 TCP	nS	
$\overline{RD}$ Pulse Width	Tdrd	6 TCP-Δ	6 TCP	-	nS	2

Notes:

1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

6.3.4 Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	nS
Data Valid to $\overline{WR}$ Low	TDAD	1 TCP-Δ	-	-	nS
Data Hold from $\overline{WR}$ High	TDWD	1 TCP-Δ	-	-	nS
$\overline{WR}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

6.3.5 Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

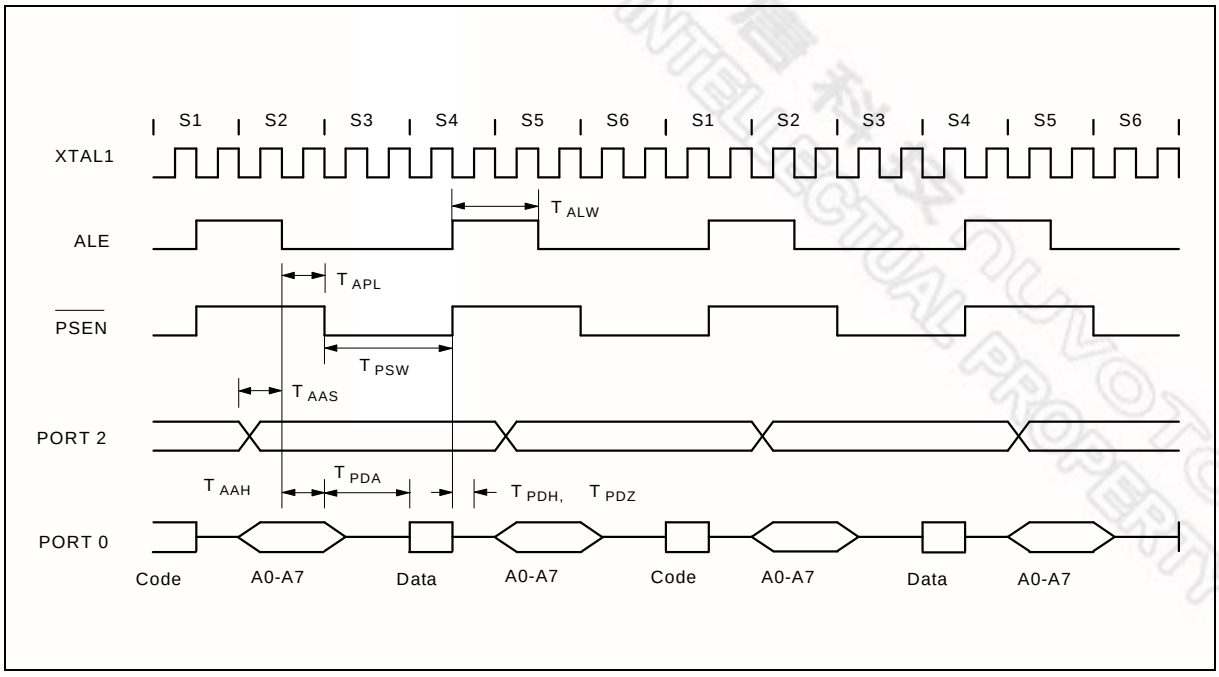
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

6.3.6 Flash Mode Timing

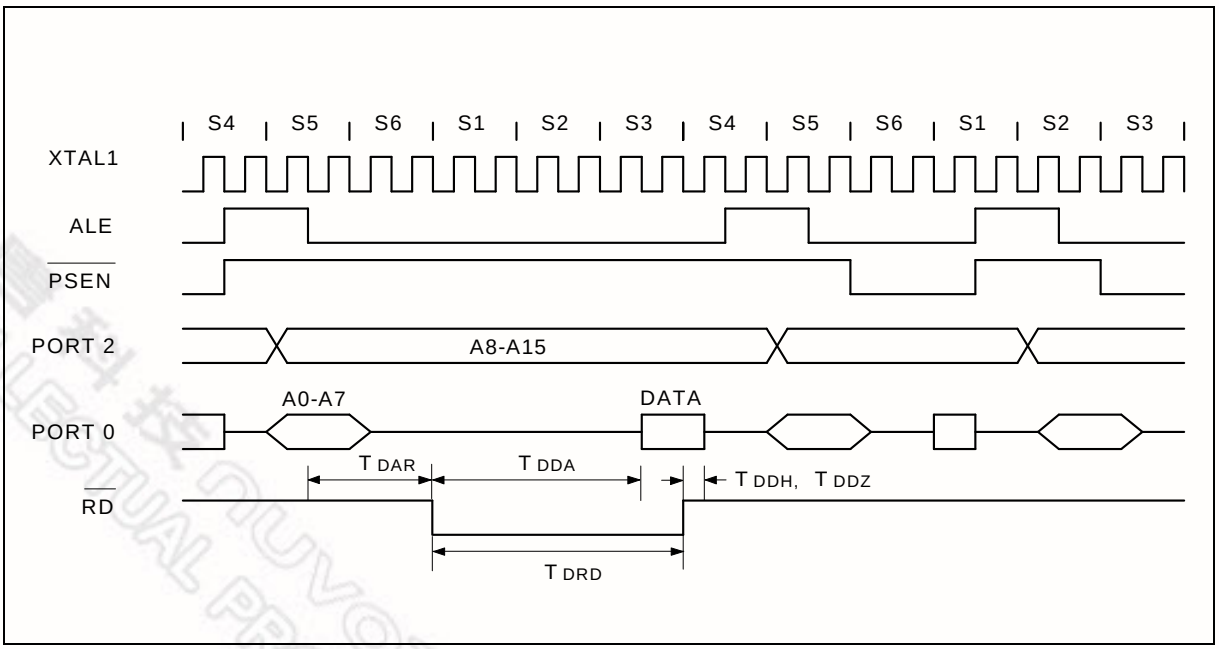
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Reset Valid	TRV	9	10	11	μS	-
Enter Flash Mode Reset Low	TEFRL	9	10	11	μS	-
Program Pulse High	TPPH	18	20	22	μS	-
Program Pulse Low	TPPL	40	50	60	μS	-
Erase Pulse Low	TEPL	25	30	50	mS	-
Read Pulse Low	TRPL	1.35	1.5	1.65	μS	-
Address PreFix	TAPF	45	50	55	nS	-
Data Remain	TDR	81	90	99	nS	-

7. TIMING WAVEFORMS

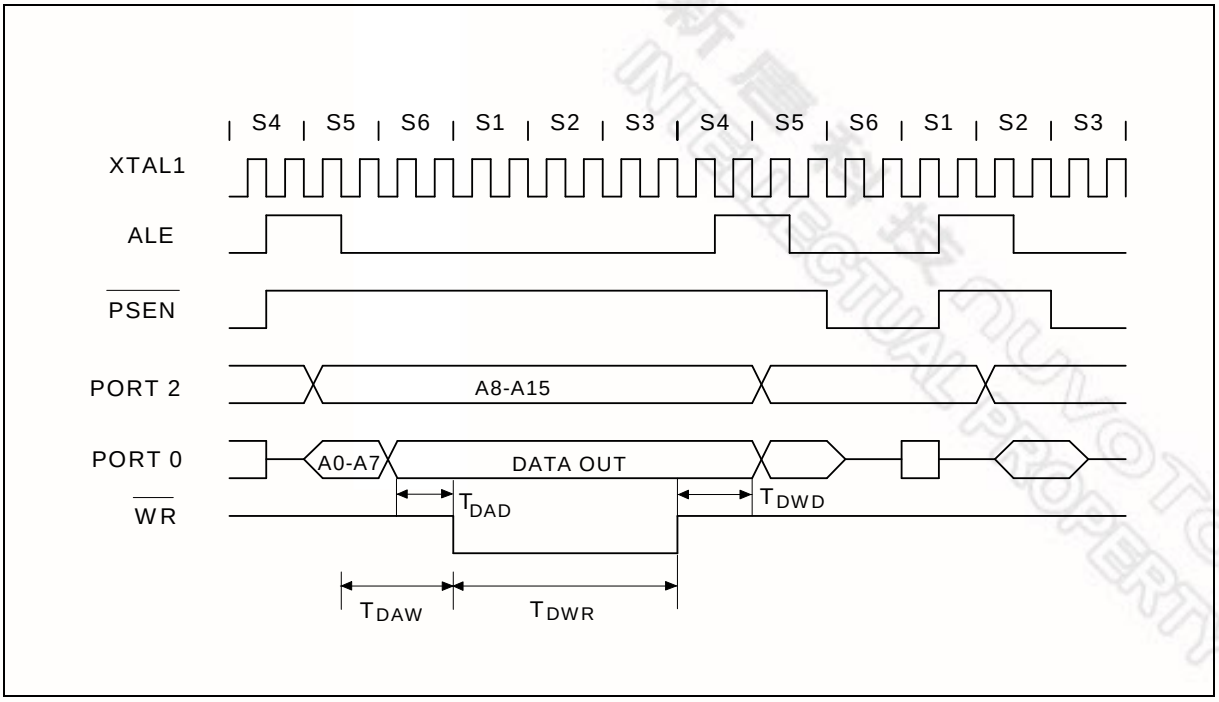
7.1 Program Fetch Cycle



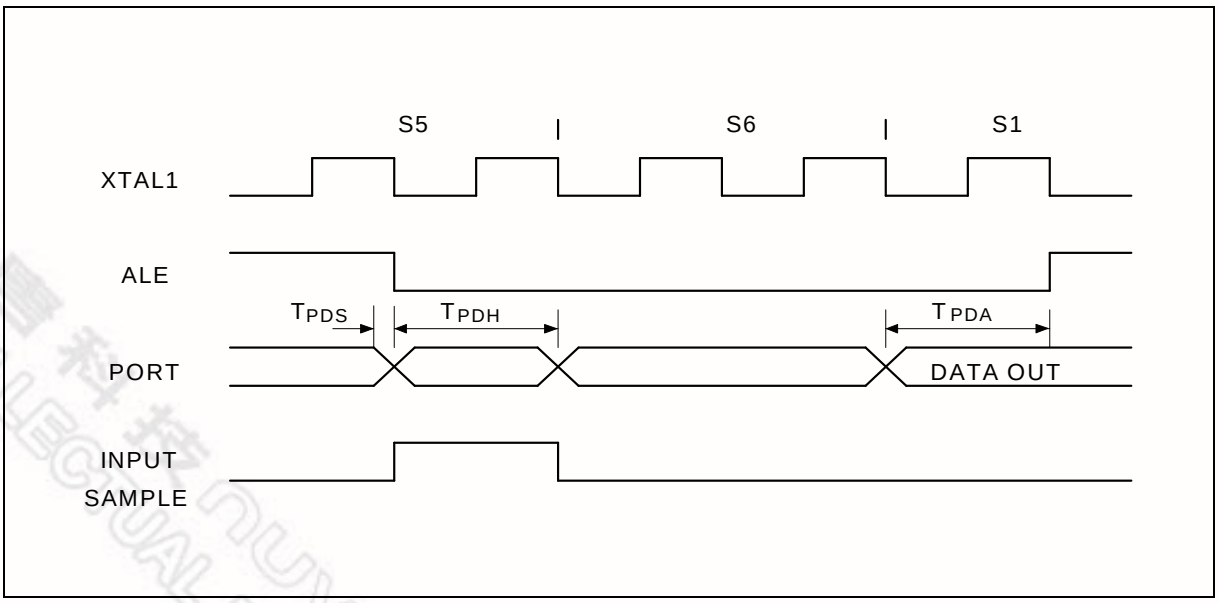
7.2 Data Read Cycle



7.3 Data Write Cycle



7.4 Port Access Cycle



8. TYPICAL APPLICATION CIRCUITS

8.1 Expanded External Program Memory and Crystal

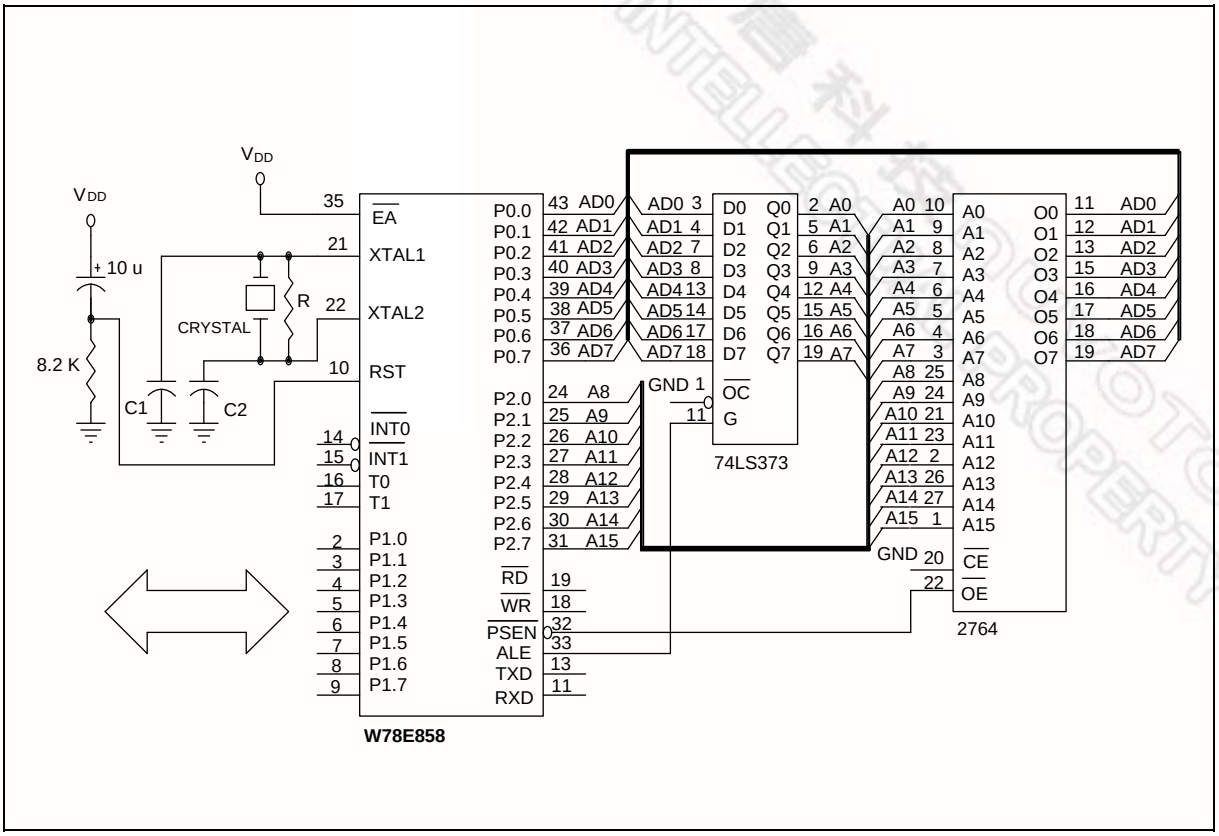


Figure A

CRYSTAL	C1	C2	R
6 MHz	68P – 100P	68P – 100P	6.8K
16 MHz	20P – 100P	20P – 100P	6.8K
24 MHz	10P – 68P	10P – 68P	6.8K
32 MHz	5P – 20P	5P – 20P	6.8K
40 MHz	5P	5P	3.3K

Above table shows the reference values for crystal applications.

Notes:

1. C1, C2, R components refer to Figure A
2. Crystal layout must get close to XTAL1 and XTAL2 pins on user's application board.

8.2 Expanded External Data Memory and Oscillator

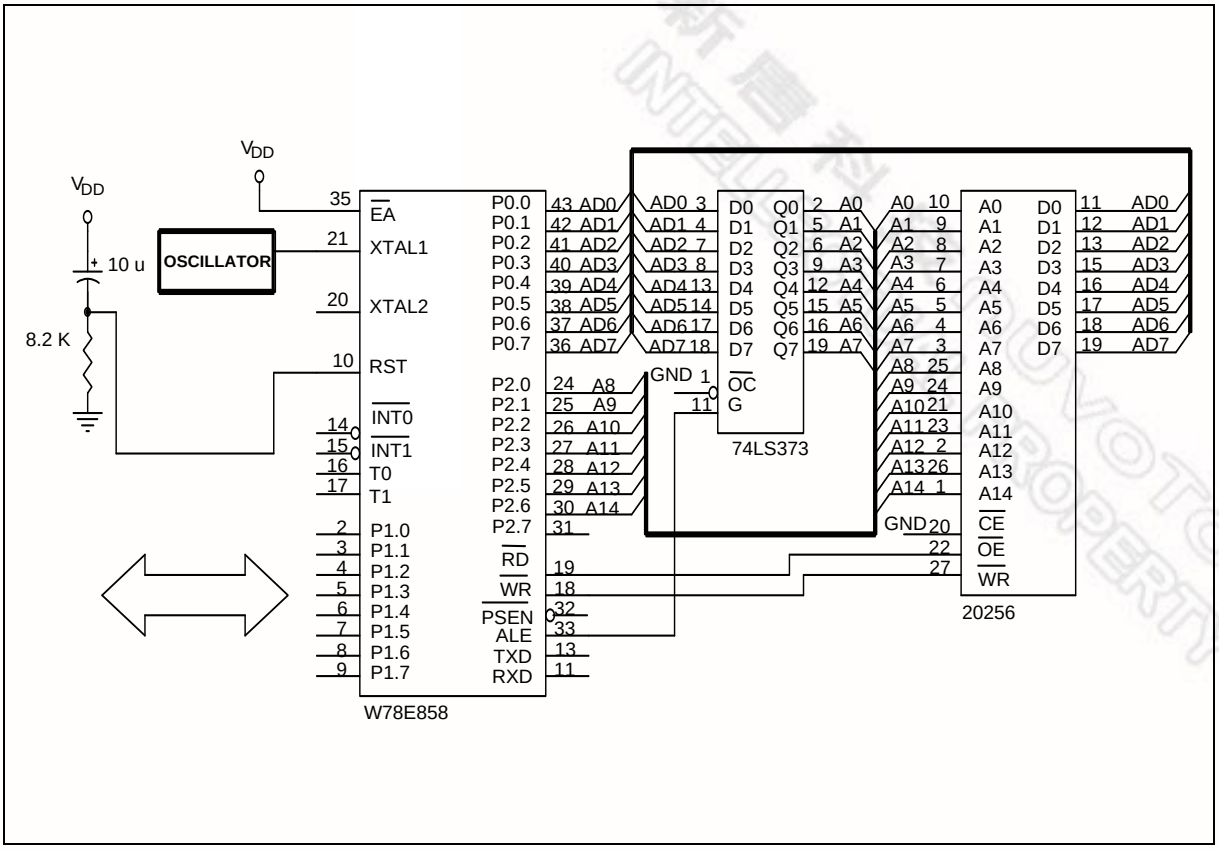


Figure B