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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e858a40pl

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1. GENERAL DESCRIPTION

The W78E858 is an 8-bit microcontroller which has an in-system programmable Flash EPROM for firmware updating. The instruction set of the W78E858 is fully compatible with the standard 8052. The W78E858 contains a 32K bytes of main Flash EPROM and a 4K bytes of auxiliary Flash EPROM which allows the contents of the 32KB main Flash EPROM to be updated by the loader program located at the 4KB auxiliary Flash EPROM ROM; 768 bytes of on-chip RAM; 128 bytes of EEPROM, 8 extra power down wake-up through INT2 to INT9; 4 channel 8-bit PWM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters where the TIMER2 with programmable clock output and 17-bit watchdog timer are built in this device; a serial port. These peripherals are supported by a eight sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78E858 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

2. FEATURES

- Fully static design 8-bit CMOS micro-controller up to 40 MHz
- 32K bytes of in-system programmable FLASH EPROM for Application Program (APROM)
- 4K bytes of auxiliary FLASH EPROM for Loader Program (LDROM)
- Low standby current at full supply voltage
- 256 + 512 bytes of on-chip RAM
- 128 bytes on-chip EEPROM memory
- 64K bytes program memory address space and 64K bytes data memory address space
- Four 8-bit bi-directional ports
- One 4-bit bi-directional port
- Extra interrupts INT2 to INT9 at PORT1
- Wake-up via external interrupts INT0 – INT9
- Three 16-bit timer/counters
- One full duplex serial port
- Fourteen-sources, two-level interrupt capability
- Programmable Timer2 clock output via P1.0
- 17-bits watchdog timer
- Four channels 8-bit PWM
- Built-in power management
- Code protection
- Packaged in PDIP 40 / PLCC 44 / PQFP 44

```
        org     0000h
                jmp     start

                org     500h
start:
                mov     chpenr,#87h
                mov     chpenr,#59h
                orl     chpcon,#00100000b       ; enable eeprom
                mov     chpenr,#00h
                call    enable_protect
                mov     dptr,#EEPROM_BASE
                mov     r0,#40h                 ; only write up to 64
byte/page. Write from FF80h to FFBFh.
                mov     r1,#55h                 ; write 55 data.
                call    write_eeprom_block
                call    enable_protect          ; Call it before writing
                mov     dptr,#EEPROM_BASE+40h
                mov     r0,#40h                 ; Write from FFC0h to FFFFh
address.
                mov     r1,#55h
                call    write_eeprom_block

                mov     dptr,#EEPROM_BASE
                mov     r0,#80h
                mov     r1,#55h
                call    read_eeprom_block
                jc      $error

                mov     chpenr,#87h
                mov     chpenr,#59h
                anl     chpcon,#11011111b       ; disable eeprom
                mov     chpenr,#00h
                clr     c
                jmp     $end
$error:
                mov     chpenr,#87h
                mov     chpenr,#59h
                anl     chpcon,#11011111b       ; disable eeprom
                mov     chpenr,#00h
                setb    c
$end:
                sjmp    $
;---------------------------------------------------------------------
disable_protect:
                mov     dptr,#EEPROM_BASE+55h
                mov     a,#aah
                movx    @dptr,a
                mov     dptr,#EEPROM_BASE+2ah
                mov     a,#55h
                movx    @dptr,a
                mov     dptr,#EEPROM_BASE+55h
                mov     a,#80h
                movx    @dptr,a
                mov     dptr,#EEPROM_BASE+55h
```

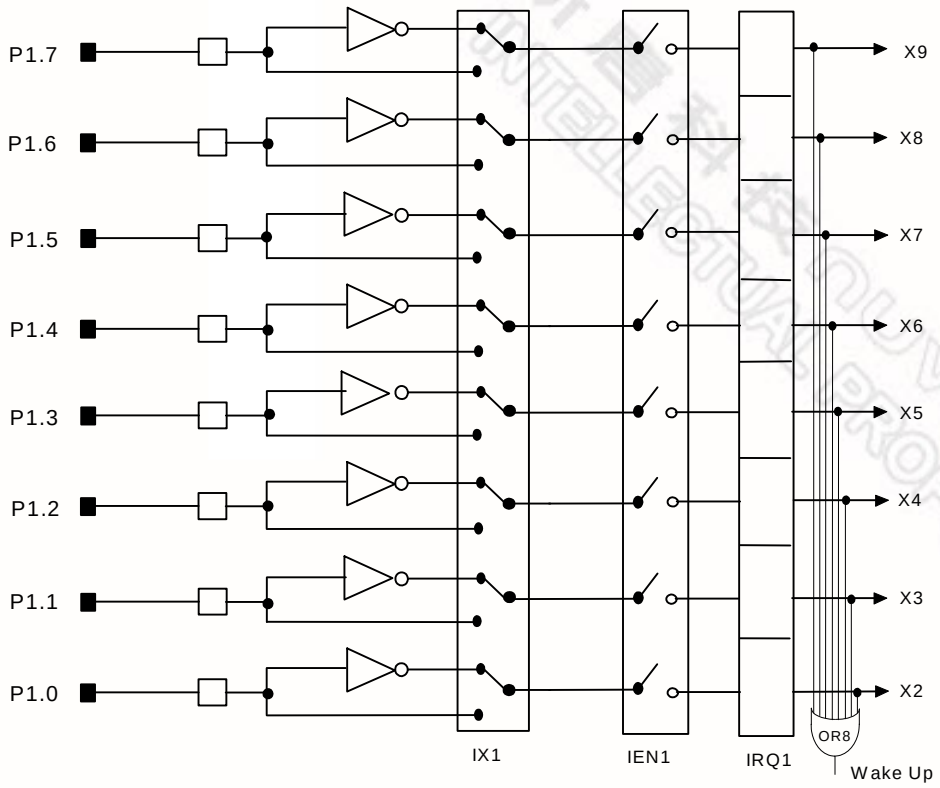


Fig. Port1 External Interrupt Configuration

5.10 Reset

The external RST signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the RA80xx is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

W78E858 Special Function Registers and Reset Values

F8	+IP1 0000000								FF
F0	+B 00000000						**CHPENR 00000000**		F7
E8	+IE_1 00000000	IX1 00000000							EF
E0	+ACC 00000000								E7
D8	**+P4 11111111**								DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000	T2MOD Xxxxxx0x	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	+IRQ1 00000000				**SFRAL 00000000**	**SFRAH 00000000**	**SFRFD 00000000**	**SFRCN 00000000**	C7
B8	+IP 000000							**CHPCON 0xx00000**	BF
B0	+P3 11111111								B7
A8	+IE 01000000								AF
A0	+P2 11111111		MXPSR 0xxxxx00						A7
98	+SCON 00000000	SBUF xxxxxxxx							9F
90	+P1 11111111	PWMCON xxxx0000	PWMP 00000000	DAC0 00000000	**DAC1 00000000**	**DAC2 00000000**	DAC3 00000000		97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR xxxx0110	WDTC 000xx000	8F
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 00110000	87

Note: the SFRs marked with a plus sign(+) are both byte and bit-addressable.

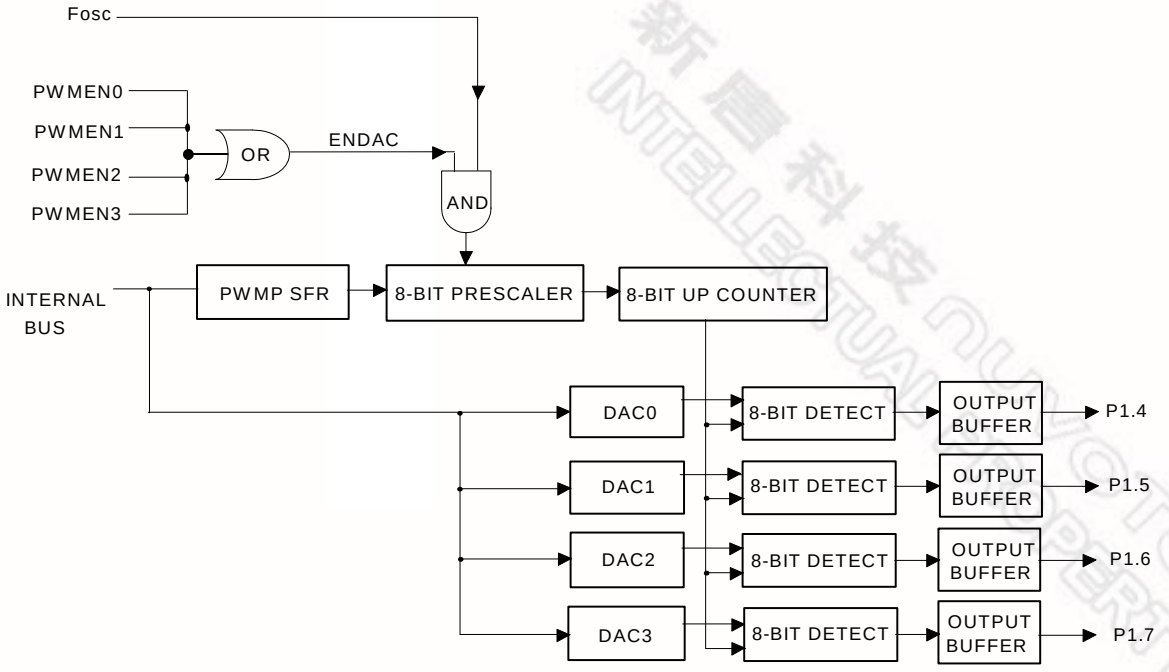


Fig. Four Channels 8-Bit PWM Function Block Diagram

5.12 In-system Programming System

The W78E858 provided in-system programming function for new firmware updated. After the related register and flags are set, user can start timer and force the CPU enter idle mode, then W78E858 will perform the in-system program mode function specify in SFRCN register, the destination data and address will come from the related SFR.

The CHPCON is read only by default. Firmware designer must write 87H, 59H sequentially to this special register CHPENR to enable the CHPCON write attribute, and write other value to disable CHPCON write attribute. This register protects from writing to the CHPCON register carelessly.

5.12.1 SFRAL (C4H)

The programming low-order byte address of FLASH EPROM in-system programming mode

5.12.2 SFRAH (C5H)

The programming high-order byte address of FLASH EPROM in-system programming mode

5.12.3 SFRFD (C6H)

The programming data for on-chip FLASH EPROM in-system programming mode

5.12.4 SFRCN (C7H)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip FLASH EPROM bank select for in-system programming. = 0: 32K bytes FLASH EPROM bank is selected as destination for re-programming. = 1: 4K bytes FLASH EPROM bank is selected as destination for re-programming.
5	OEN	FLASH EPROM output enable.
4	CEN	FLASH EPROM chip enable.
3 – 0	CTRL[3:0]	The flash control signals

5.13 In-system Programming Mode Operating Table

MODE	CTRL<3:0>	WFWIN	OEN	CEN	SFRAL	SFRAH	SFRFD
Erase 32K APROM	0010	0	1	0	X	X	X
Erase 4K LDROM	0010	1	1	0	X	X	X
Program 32K APROM	0001	0	1	0	Address	Address	Data In
Program 4K LDROM	0001	1	1	0	Address	Address	Data In
Read 32K APROM	0000	0	0	0	Address	Address	Data Out
Read 4K LDROM	0000	1	0	0	Address	Address	Data Out

5.13.1 CHPCON (BFH)

BIT	NAME	FUNCTION
7	SWRESET (F04KMODE)	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit can determine that the F04KBOOT mode is running.
6	-	Reserve.
5	ENEEPROM	Enable on-chip 128 bytes EEPROM.
4	ENAUXRAM	Enable on-chip 512 bytes auxiliary RAM.
3 – 2	-	-
1	FBOOTSL	The loader program location selection. = 0: loader program in 32K memory bank. = 1: loader program in 4K memory bank.
0	FPROGEN	In system programming enable flag. = 1: enable. The CPU switches to the programming flash mode after entering the idle mode and waken up from interrupt. The CPU will execute the loader program while in on-chip programming mode. = 0: disable. The on-chip FLASH EPROM read-only. In-system programmability is inhibit.

5.14 MXPSR (A2H)

BIT	NAME	FUNCTION
7	BUSY	EEPROM BUSY signal. 1: EEPROM is writing.
6-2	-	Reserved.
1-0	ADDRPNT	Address pointer by MOVX instruction 0: read or write lower 256 byte Auxiliary RAM by pointer of R0 or R1 register 1: read or write Higher 256 byte Auxiliary RAM by pointer of R0 or R1 register 2: 128 byte EEPROM by pointer of R0 or R1 register

5.15 Interrupt System

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to do execution of any particular section of code. To tie the asynchronous actives of these functions to normal program execution, a multiple-source, two-priority-level, nested interrupt system is provided. The W78E858 acknowledges interrupt requests from fourteen sources as below:

- INT0 and INT1
- Timer0 and Timer1
- UART serial I/O
- INT2 to INT9 (at Port1)

5.16 External Interrupts INT2 to INT9

Port1 lines serve an alternative purpose at eight additional interrupts INT2 to INT9. When enabled, each of these lines may "wake-up" the device from power-down mode. Using the IX1 register, the each pin may be initialized to either active HIGH or LOW. IRQ1 is the interrupt request flag register. Each flag, if the interrupt is enabled will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disable.

The Port1 interrupts are level sensitive. A Port1 interrupt will be recognized when a level (HIGH or LOW depending on Interrupt Polarity Register IX1) on P1.x is held active for at least one machine cycle. The interrupt request is not served until the next machine cycle.

5.16.1 IE_1 (E8H)

BIT	NAME	FUNCTION
7	EX9	Enable external interrupt 9
6	EX8	Enable external interrupt 8
5	EX7	Enable external interrupt 7
4	EX6	Enable external interrupt 6
3	EX5	Enable external interrupt 5
2	EX4	Enable external interrupt 4
1	EX3	Enable external interrupt 3
0	EX2	Enable external interrupt 2

5.16.2 IP1 (F8H)

BIT	NAME	FUNCTION
7	PX9	External interrupt 9 priority level
6	PX8	External interrupt 8 priority level
5	PX7	External interrupt 7 priority level
4	PX6	External interrupt 6 priority level
3	PX5	External interrupt 5 priority level
2	PX4	External interrupt 4 priority level
1	PX3	External interrupt 3 priority level
0	PX2	External interrupt 2 priority level

5.16.3 IX1 (E9H)

BIT	NAME	FUNCTION
7	IL9	External interrupt 9 polarity level
6	IL8	External interrupt 8 polarity level
5	IL7	External interrupt 7 polarity level
4	IL6	External interrupt 6 polarity level
3	IL5	External interrupt 5 polarity level
2	IL4	External interrupt 4 polarity level
1	IL3	External interrupt 3 polarity level
0	IL2	External interrupt 2 polarity level

5.16.4 IRQ1 (C0H)

BIT	NAME	FUNCTION
7	IQ9	External interrupt 9 request flag
6	IQ8	External interrupt 8 request flag
5	IQ7	External interrupt 7 request flag
4	IQ6	External interrupt 6 request flag
3	IQ5	External interrupt 5 request flag
2	IQ4	External interrupt 4 request flag
1	IQ3	External interrupt 3 request flag
0	IQ2	External interrupt 2 request flag

5.16.5 Interrupt Priority and Vector Address

PRIORITY	INTERRUPT	VECTOR	SOURCE	PRIORITY	INTERRUPT	VECTOR	SOURCE
1	INT0	0003H	External 0	8	TF1	001BH	Timer 1
2	INT5	0053H	External 5	9	SINT	0023H	UART
3	TF0	000BH	Timer 0	10	TF2	002BH	Timer 2
4	INT6	005BH	External 6	11	INT3	0043H	External 3
5	INT1	0013H	External 1	12	INT8	006BH	External 8
6	INT2	003BH	External 2	13	INT4	004BH	External 4
7	INT7	0063H	External 7	14	INT9	0073H	External 9

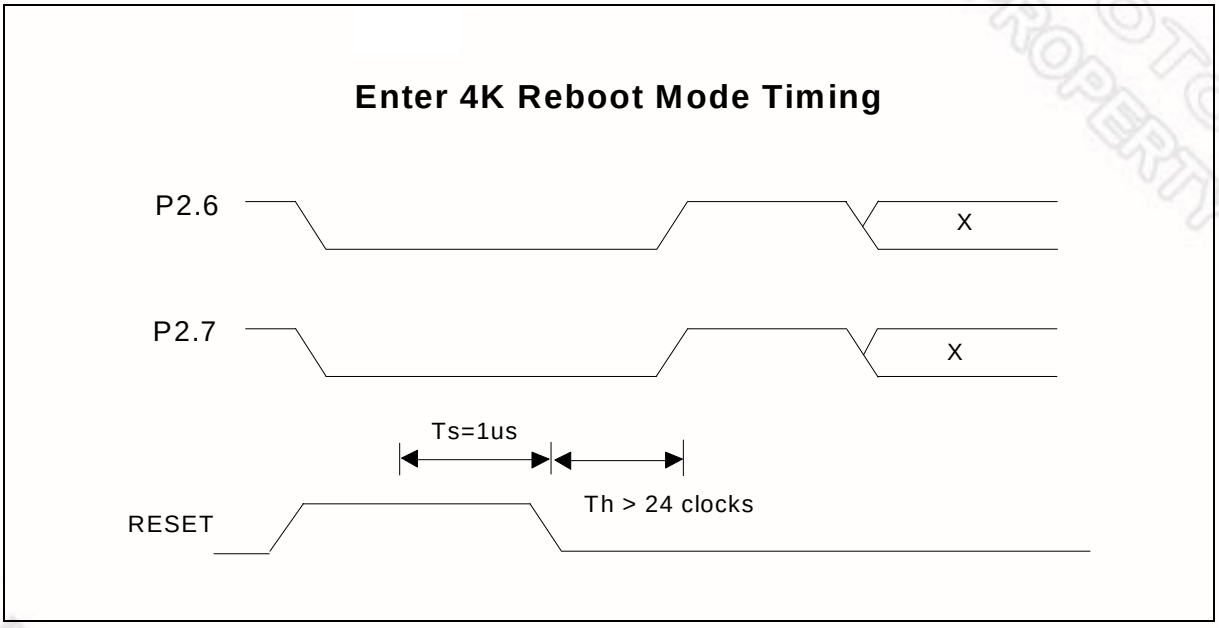
5.17 F04KBOOT Mode (Boot From 4K Bytes LDROM)

The W78E858 boots from APROM program (32K bytes bank) by default after chip reset. On some occasions, user can force the W78E858 to boot from the LDROM program (4K bank) after chip reset. The setting for this special mode is as follow.

5.17.1 F04KBOOT Mode

RST	P4.3	P2.7	P2.6	MODE
H↓	X	L	L	FO4KBOOT
H↓	L	X	X	FO4KBOOT

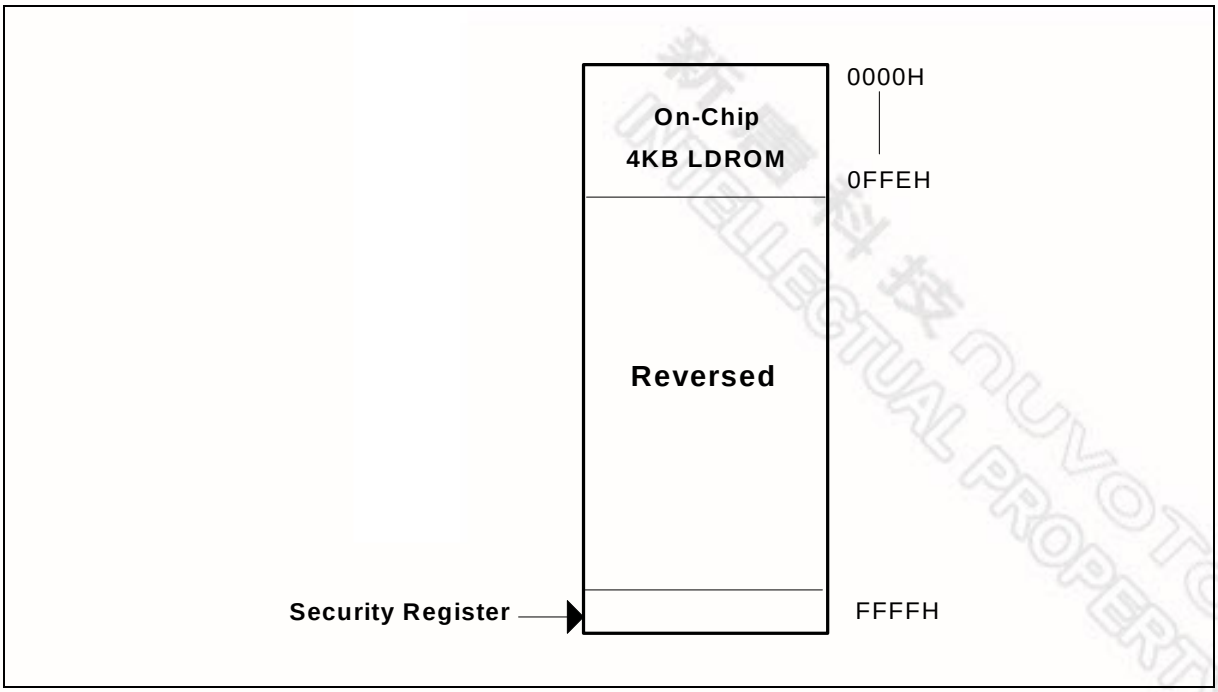
Note: In application system design, user must take care the P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ pin status at reset to avoid W78E858 entering the programming mode or F04KBOOT mode in normal operation.



5.18 Security

During the on-chip FLASH EPROM programming mode, the FLASH EPROM can be programmed and verified repeatedly. Until the code inside the FLASH EPROM is confirmed OK, the code can be protected. The protection of FLASH EPROM and those operations on it are described below:

The W78E858 has several special setting registers in FLASH EPROM block. Those bits of the security register can't be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The security register is located at the FFFFH on the same bank with 4K LDROM i.e., P3.6 must set high at writer mode.



5.18.1 Lock Bit (Bit0)

This bit is used to protect the customer's program code in the W78E858. It may be set after the programmer finishes the programming and verifies sequence. Once these bits are set to logic 0, both the FLASH EPROM data and all data in FLASH EPROM block can't be accessed again.

5.18.2 MOVC Lock (Bit1)

When this bit is program to "0", the MOVC instruction will be disable when the program counter more than 7FFFh or $\overline{EA}$ pin is forced low.

5.18.3 Scramble Enable (Bit2)

This bit is used to protect the customer's program code in the W78E858. If this bit is set to logic 0, the dump ROM code are scrambled by a scramble circuit and the dump ROM code will become a random ROM code.

5.18.4 Oscillator Gain Select (Bit7)

If this bit is set to logic 0 (for 24 MHz), the EMI effect will be reduce. If this bit is set to logic 1 (for 40 MHz), the W78E858 could to use 40 MHz crystal, but the EMI effect is major. So we provide the option bit which could be chose by customer.

5.19 Watch Dog Timer

For more system reliability, W78E858 provides a programmable watch-dog time-out reset function. From programming prescaler select, user can choose a variable prescaler from divided by 2 to divided by 256 to get a suitable time-out period. The time-out period is given by:

$$T_{time\text{-}out} = \frac{1}{Fosc} \times 2^{14} \times PRESCALER \times 1000 \times 12 \ (mS)$$

(Note: Fosc unit = Hz)

5.19.1 WDTC (8FH)

BIT	NAME	FUNCTION
7	ENW	Enable watch-dog timer if set.
6	CLRW	Clear watch-dog timer and prescaler if set. This flag will be cleared auto-matically.
5	WIDL	If this bit is set, watch-dog is enabled under idle mode. If cleared, watch-dog is disable under idle mode. Default is cleared.
4 – 3	-	Reversed.
2	PS2	Watch-dog prescaler timer select.
1	PS1	Watch-dog prescaler timer select.
0	PS0	Watch-dog prescaler timer select.

PS2	PS1	PS0	PRESCALER SELCET	WATCH-DOG TIME-OUT PERIOD (Fosc = 20 MHz)
0	0	0	2	19.66 mS
0	1	0	4	39.32 mS
0	0	1	8	78.64 mS
0	1	1	16	157.28 mS
1	0	0	32	314.57 mS
1	0	1	64	629.14 mS
1	1	0	128	1.25 mS
1	1	1	256	2.52 mS

5.20 Programmable Clock-out

A 50% duty cycle clock can be programmed to come out on P1.0. To configure the timer/counter2 as a clock generator, bit C/T2 in T2CON register must be cleared and bit T2OE in T2MOD register must be set. Bit TR2 (T2CON.2) also must be set to start timer. The clock-out frequency depends on the oscillator frequency and reload value of Timer2 capture register (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{oscillatotr\ \ frequency}{4\times(65536-(RCAP2H,RCAP2L))}$$

In the clock-out mode, timer2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer2 as a baud-rate generator and a clock and a clock generator simultaneously.

5.21 Reduce EMI Emission

The transition of ALE will cause noise, so it cab be turned off to reduce the EMI emission if it is useless. Turn off the ALE signal transition only need too set the ALEOFF flag in the AUXR register When ALE is turned off, it will be reactived when program access external ROM or RAM data or jump to execute external ROM code. After access completely or program returns to internal ROM code, ALE signal will turn off again.

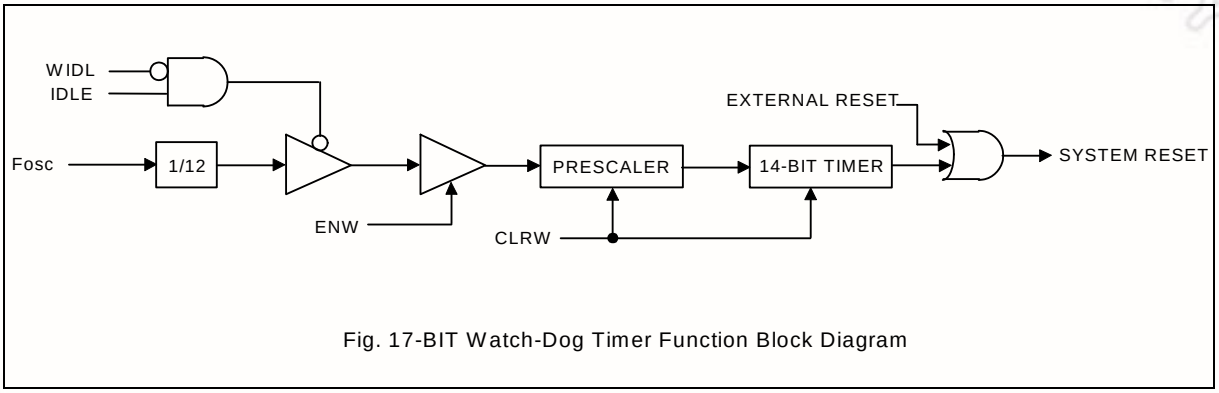
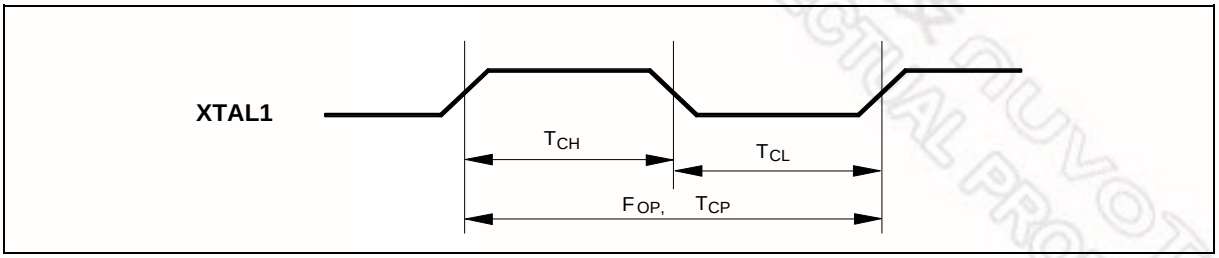


Fig. 17-BIT Watch-Dog Timer Function Block Diagram

6.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

6.3.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	40	MHz	1
Clock Period	T_{CP}	25	-	-	nS	2
Clock High	T_{CH}	10	-	-	nS	3
Clock Low	T_{CL}	10	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

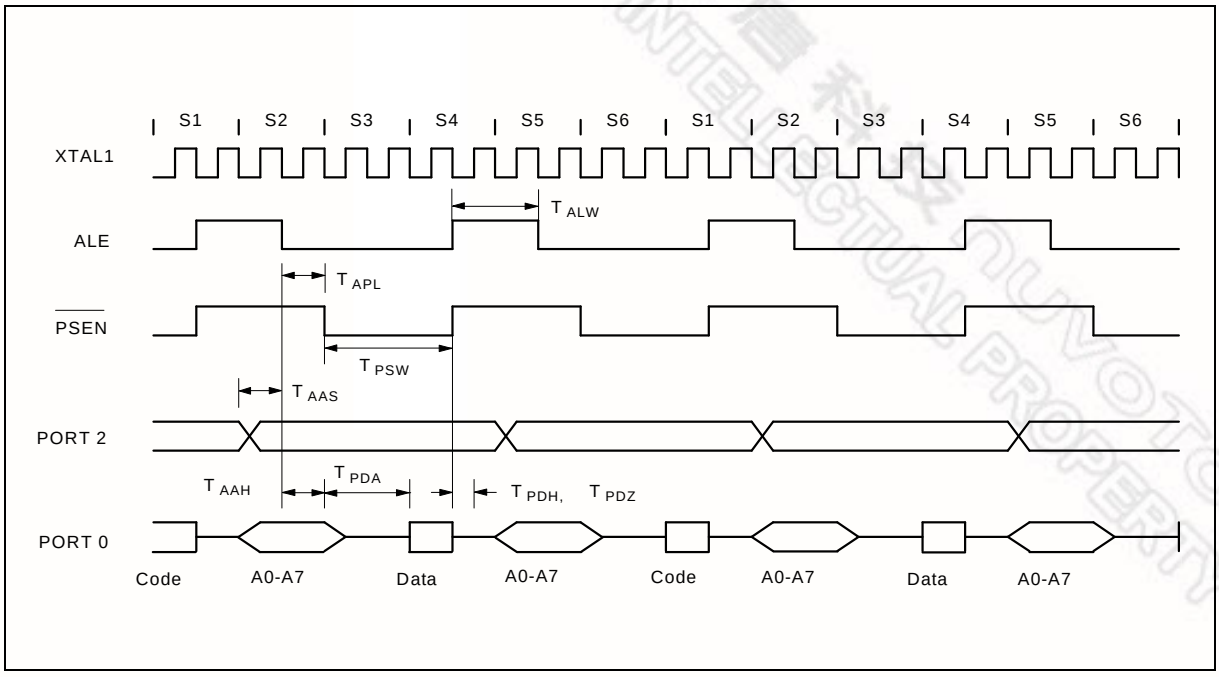
6.3.2 Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	T_{AAS}	1 T_{CP}-Δ	-	-	nS	4
Address Hold from ALE Low	T_{AAH}	1 T_{CP}-Δ	-	-	nS	1, 4
ALE Low to $\overline{PSEN}$ Low	T_{APL}	1 T_{CP}-Δ	-	-	nS	4
$\overline{PSEN}$ Low to Data Valid	T_{PDA}	-	-	2 T_{CP}	nS	2
Data Hold after $\overline{PSEN}$ High	T_{PDH}	0	-	1 T_{CP}	nS	3
Data Float after $\overline{PSEN}$ High	T_{PDZ}	0	-	1 T_{CP}	nS	
ALE Pulse Width	T_{ALW}	2 T_{CP}-Δ	2 T_{CP}	-	nS	4
$\overline{PSEN}$ Pulse Width	T_{PSW}	3 T_{CP}-Δ	3 T_{CP}	-	nS	4

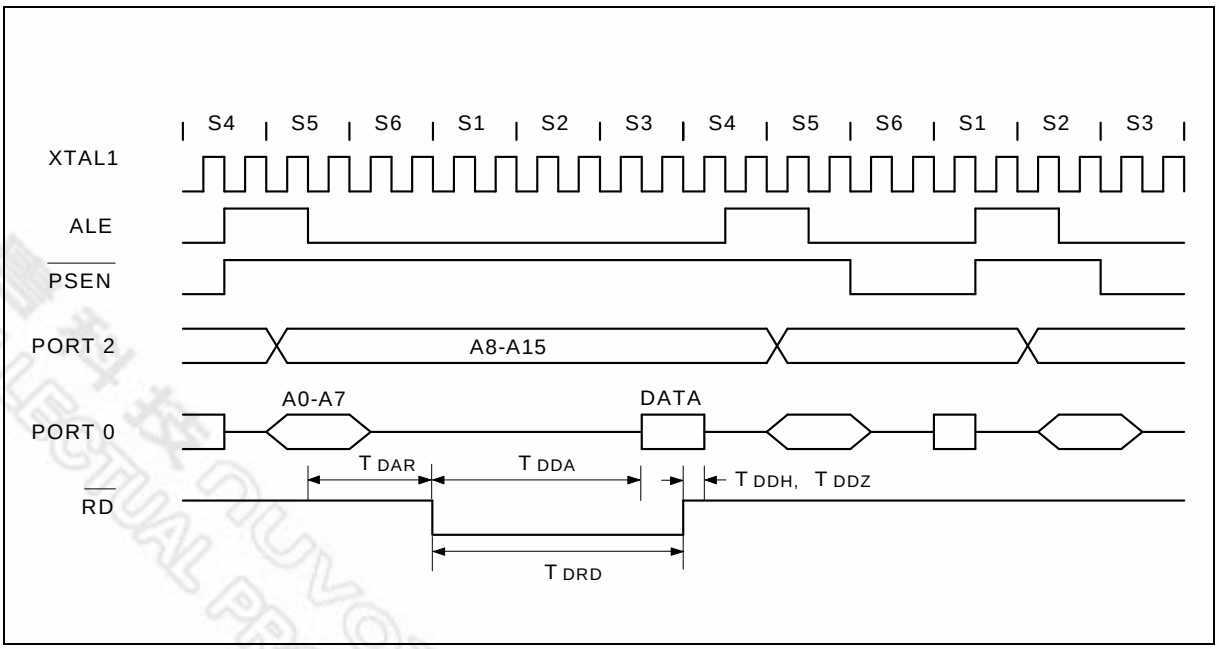
Notes:
1. P0.0 – P0.7, P2.0 – P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 T_{CP}.
3. Data have been latched internally prior to $\overline{PSEN}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

7. TIMING WAVEFORMS

7.1 Program Fetch Cycle



7.2 Data Read Cycle



8.2 Expanded External Data Memory and Oscillator

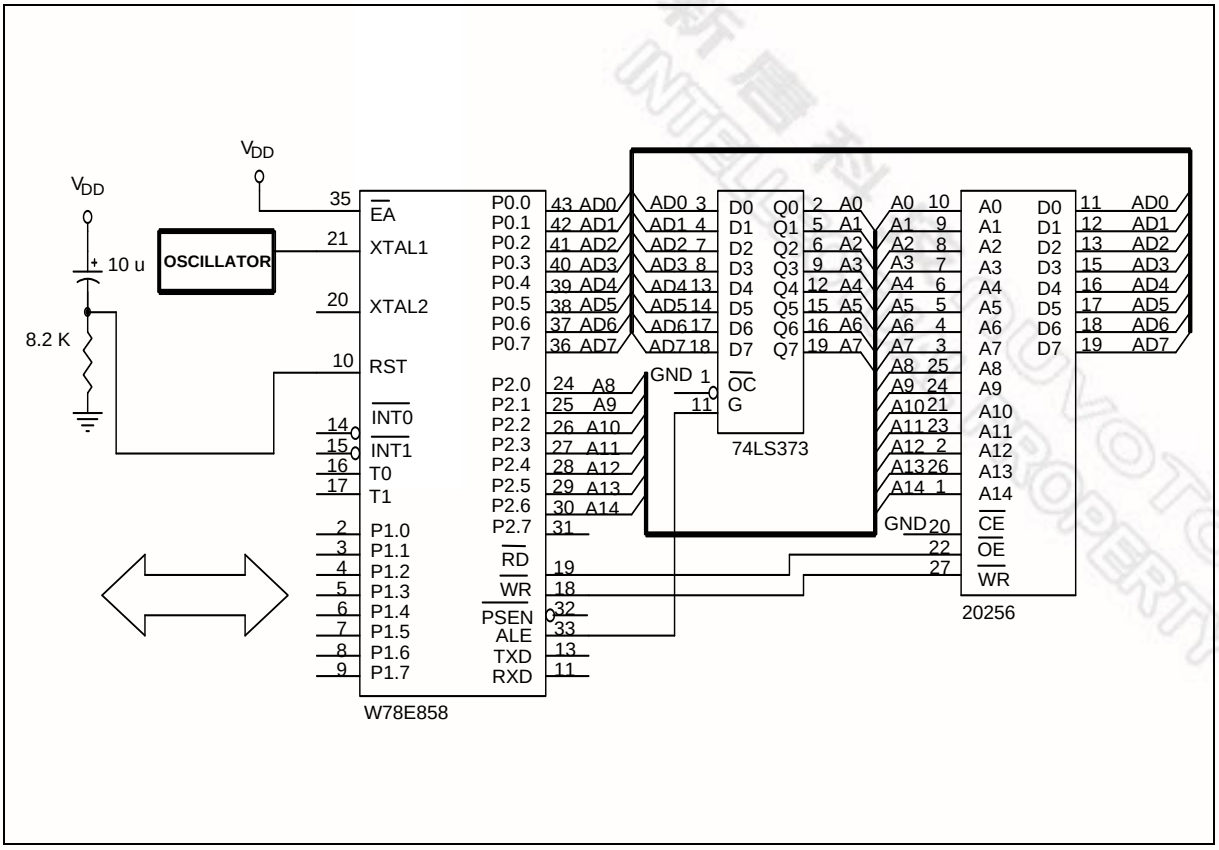
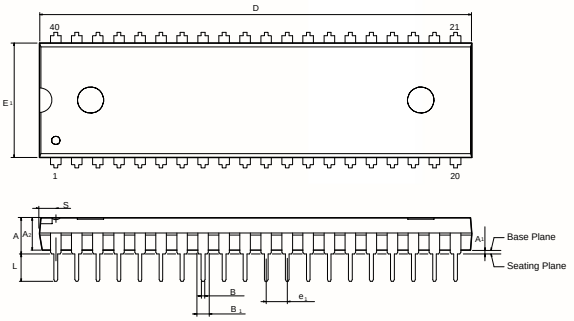


Figure B

9. PACKAGE DIMENSIONS

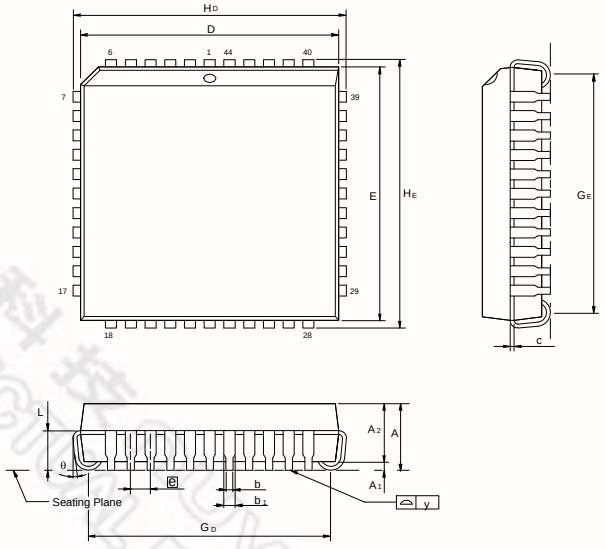
9.1 40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

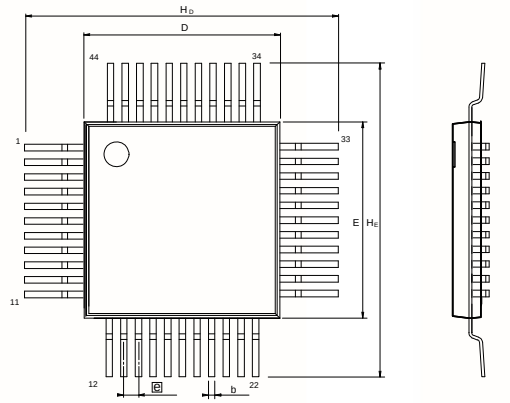
9.2 44-pin PLCC

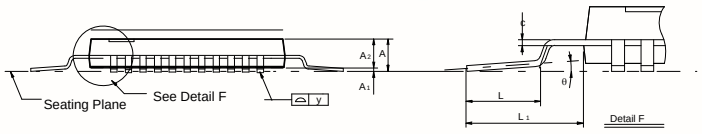


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

9.3 44-pin PQFP





Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

10. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	Oct. 2001	-	Initial Issued
B	Jul. 2002	15	Modify timer 2 interrupt vector address
C	Nov. 2002	5	EEPROM address of command code
D	May. 2004	6	Remove erase acquisition flow
		6	Add a demo code
A5	April 20, 2005	33	Add Important Notice
A6	May 3, 2006	7	Revise “03H to MXPSR” to ”02H to MXPSR”
A7	November 6, 2006		Remove block diagram
A8	April 22, 2008	14	Update P3 reset state