Trenz Electronic GmbH - TE0600-02B Datasheet

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Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Spartan-6 LX-100
Co-Processor	-
Speed	125MHz
Flash Size	16MB
RAM Size	256MB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0600-02b

Key Features

- Industrial-grade Xilinx Spartan-6 LX FPGA micromodule (LX45 / LX100 / LX150)
- 10/100/1000 tri-speed Gigabit Ethernet transceiver (PHY)
- 2 x 16-bit-wide 1 Gb (128 MB) or 4Gb (512 MB) DDR3 SDRAM
- 128Mb (16 MB) SPI Flash memory (for configuration and operation) accessible through:
- 1Kb Protected 1-Wire EEPROM with SHA-1 Engine
- JTAG port (SPI indirect)
- FPGA configuration through:
  - B2B connector
  - JTAG port
  - SPI Flash memory
- Plug-on module with 2 × 100-pin high-speed hermaphroditic strips
- Up to 52 differential, up to 109 single-ended (+ 1 dual-purpose) FPGA I/O pins available on B2B strips
- 4.0 A x 1.2 V power rail
- 1.5 A x 1.5 V power rail
- 125 MHz reference clock signal
- Single-ended custom oscillator (option)
- eFUSE bit-stream encryption (LX100 or larger)
- 1 user LED
- Evenly-spread supply pins for good signal integrity
- Other assembly options for cost or performance optimization available upon request.

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1 Technical Specifications

1.1 Components

- Xilinx Spartan-6 LX FPGA:
  - XC6SLX**45**-2FGG484**C** = 43 K logic cells, commercial grade
    XC6SLX**45**-2FGG484**I** = 43 K logic cells, industrial grade
  - XC6SLX**100**-2FGG484**C** = 101 K logic cells, commercial grade
    XC6SLX**100**-2FGG484**I** = 101 K logic cells, industrial grade
  - XC6SLX**150**-2FGG484**C** = 147 K logic cells, commercial grade
    XC6SLX**150**-2FGG484**I** = 147 K logic cells, industrial grade
- 10/100/1000 Gigabit Ethernet transceiver (physical layer)
  Marvell Semiconductor 88E1111
- 2 × independent 16-bit-wide (data-bus) 1 Gigabit (128 megabyte) or 4 Gigabit (512 megabyte) DDR3 SDRAM
- 128 megabit (16 megabyte) serial Flash memory with dual/quad SPI interface
- 48-bit node address chip
  Maxim Integrated Products DS2502-E48
- 1Kb Protected 1-Wire EEPROM with SHA-1 Engine

  Maxim Embedded Security Products DS2432
- 2 x fine-pitch (0.5 mm) 100-pin high-speed (up to 10.0 GHz / 20 Gbps) hermaphroditic strips
  LSHM-150-04.0-L-DV-A-S-K-TR
- Up to 52 differential FPGA input/output pins available on B2B strips
- Up to 109 single-ended (+ 1 dual-purpose) FPGA input/output pins available on B2B strips
- Ethernet (PHY), JTAG and SPI pins available on B2B strips
- 4.0 A high-efficiency DC-DC switching regulator for power rail 1.2V
- 1.5 A high-efficiency DC-DC switching regulator for power rail 1.5V
- 2 x 800 mA DC-DC linear regulator for power rails 2.5V and VCCAUX
- Processor supervisory circuits with power-fail and watchdog
  Texas Instruments TPS3705-33
- 125 MHz clock signal (system + user)
- Footprint for custom single-ended oscillator (option)
- 1 x LED (user)
- Power supply voltage: 3.3 V
- Power supply source: board-to-board interconnect (e.g. carrier board)
- Dimensions: 50 mm × 40 mm (20 cm^2)
- Minimum module height: 8 mm (without connectors)

- Maximum height on carrier board surface: ≈ 13 mm (standard connectors)
- Minimum height on carrier board surface: ≈ 5 mm (standard connectors)
- Weight: 17.2 ± 0.1 g
- Temperature grades:
- commercial (C-type FPGA device)
- industrial (I-type FPGA device)

1.2 Dimensions

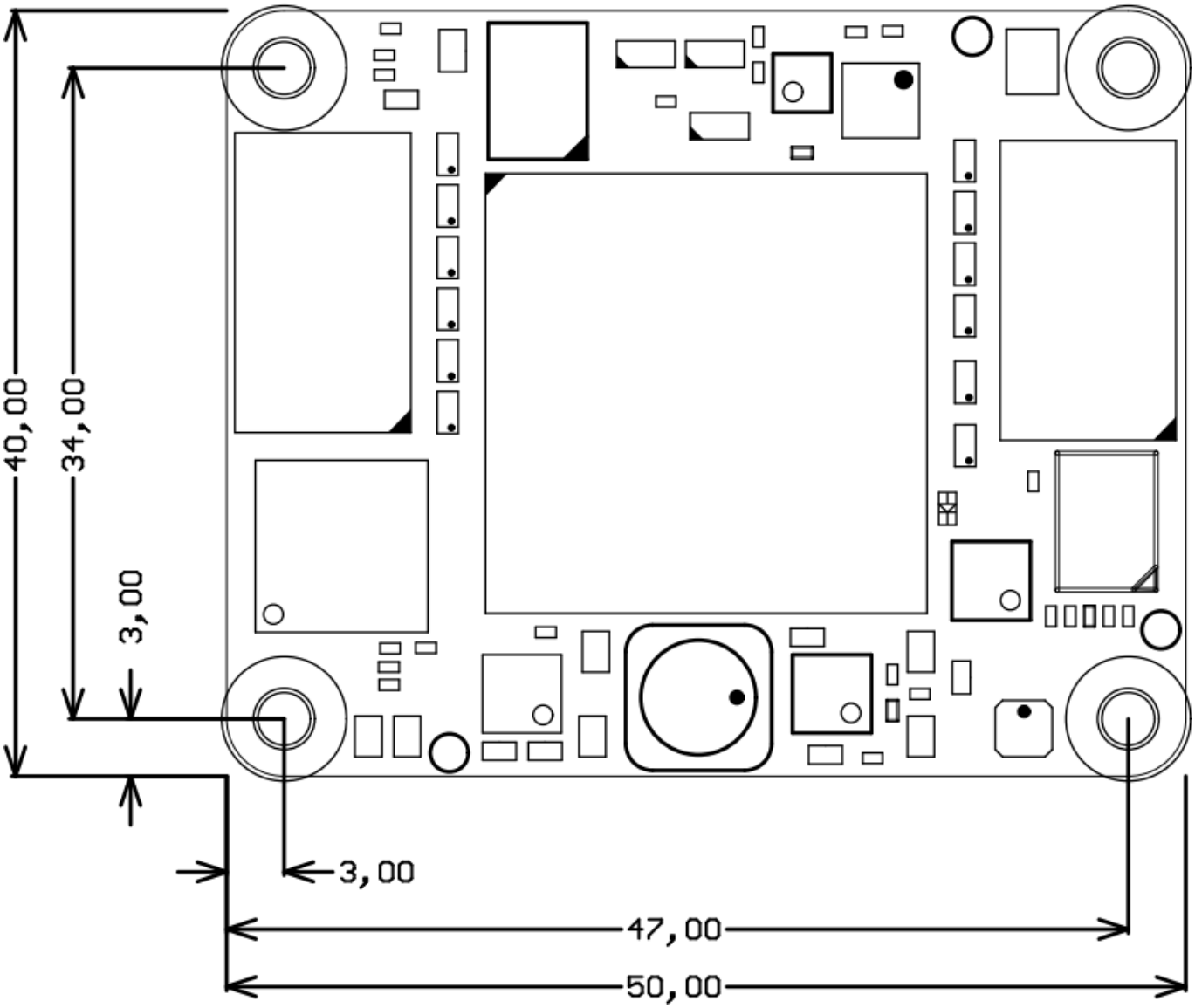

Figure 3: GigaBee board dimensions (top view)

GigaBee XC6SLX can reach a minimum vertical height of about 8 mm, if B2B

connectors are not assembled. The maximum component height on the module board on the top side is about 3.5 mm. The maximum component height on the module board on the bottom side is about 3.0 mm.

The typical minimum and maximum height from the carrier board surface, of a GigaBee XC6SLX when it mounted on a carrier board, is respectively about 5.0 mm and about 13 mm.

GigaBee XC6SLX has 4 mounting holes, one in each corner. The module can be fixed by screwing M3 screws (ISO 262) onto a carrier board through those mounting holes.

GigaBee XC6SLX weighs between 17.1 and 17.3 g with standard connectors.

1.3 Power Consumption

Power consumption of GigaBee XC6SLX modules highly depend on the FPGA design implemented. Some typical power consumptions are provided in Table 1 for the following reference systems:

- Boards – GigaBee XC6SLX 45/100/150
- Base board – TE0603-02
- Power supply – 5 V from baseboard
- Connected Gigabit Ethernet cable

FPGA type	Unconfigured	Configured with Web-server reference design
LX45	0.15 A	0.6 A
LX100	0.17 A	0.5 A
LX150	0.2 A	0.5 A

Table 1: Power consumption

- J2 connector (option: if zero-resistor R80 **is** populated and zero-resistor R79 is **not** populated).

2.2.3.5 VCCAUX Power Rail

It is converted from the 3.3V rail by a linear voltage regulator and can provide up to 0.8 A to:

- FPGA auxiliary circuits;
- J2 connector.

2.2.3.6 VCCIO0 Power Rail

There are 4 options to supply this rail:

- from 3.3 V power rail (if zero-resistor R79 **is** populated[2] and R80 is **not**);
- from 2.5 V power rail (if zero-resistor R80 **is** populated and R79 is **not**);
- from 1.5 V power rail (if zero-resistors R79 and R80 are **not** populated and VCCIO0 connected to 1.5 V power rail);
- from an external power source through J2 B2B connector (pins 1, 3, 5, 7, 9) (if R79 and R80 are **not** populated)

It supplies:

- FPGA bank 0 $V_{CCO.}$

Figure 6 show simplified schematic of power options. Dashed resistors are not populated by default.

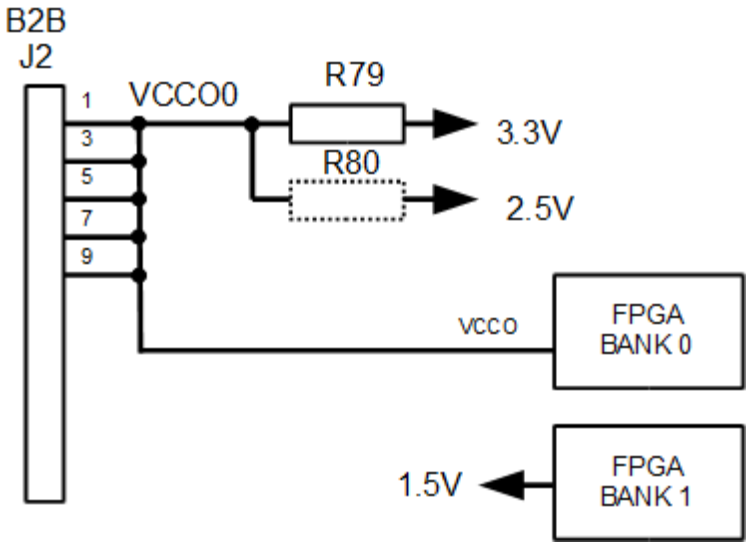

Figure 6: Power options diagram

2 Default assembling for VCCIO0 rail

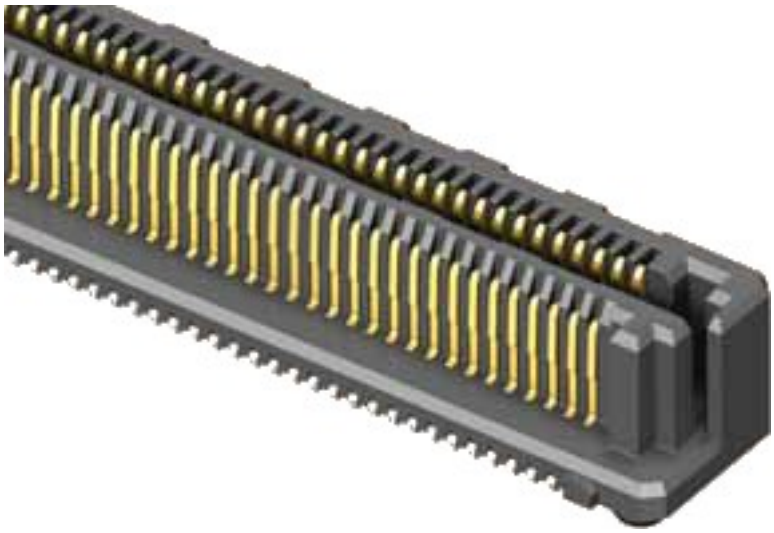

Figure 9: Samtec Razor Beam LSHM connector

The overall number of connector contacts on the GigaBee XC6SLX is 200.

Samtec Razor Beam LSHM is a high-speed interconnect system with very fine pitch (50 mil) and low profile design. Razor Beam connectors are well suited for high speed applications with performance up to 11.5 GHz (23 Gb/s) at -3 dB insertion loss. Razor Beam contacts are ideal for high speed and rugged applications featuring undercut retention notches that increase the withdrawal force and provide an audible click when the contacts engage. In addition, the self-mating (hermaphroditic) design can help reduce inventory costs. The LSHM Series features also optional shielding for EMI protection (default on GigaBee XC6SLX).

Samtec Razor Beam LSHM connectors are keyed. On the bottom side of the GigaBee XSL6, the connectors are assembled in such a way to prevent the module to be reverse mounted on carrier boards.

Samtec Razor Beam LSHM are available in different lead styles, see Table 4 for details.

lead style	A [mm]	B [mm]
-02.5	3.95	1.00
-03.0	4.45	1.50
-04.0	5.45	2.50
-06.0	7.45	4.50

Table 4: Samtec Razor Beam LSHM lead styles

2.7 Flash Memory

GigaBee XC6SLX board contains 128 Mb (16 MB) serial flash memory chip Winbond W25Q128BV (U11). This serial flash chip can operate as general SPI memory mode and in double or quad modes. Usage of dual and quad modes increase bandwidth up to 40 MB/s.

For more information see Winbond W25Q128BV product overview.

Flash can be programmed in several ways:

- Direct SPI programming via J1 connector.
- Indirect SPI programming via FPGA pins, controlled by JTAG.
- Direct SPI programming by FPGA, using SPI core.

Serial flash is connected to FPGA bank 2 and B2B connector J1; used pins are listed in Table 8.

Flash signal	FPGA pin	J1 pin
/CS	T5	87
CLK	Y21	91
DI(IO0)	AB20	95
DO(IO1)	AA20	93
/WP(IO2)	U14	99
/HOLD(IO3)	U13	97

Table 8: Serial flash signals connection

2.8 Ethernet

The board contains a Marvell Alaska Ethernet PHY chip (88E1111) operating at 10/100/1000 Mb/s. The board supports GMII interface mode with the FPGA. Configuration details:

- PHY address – 00111
- Advertise pause
- Auto Neg
- Advertise all caps
- Prefer slave
- Auto crossover
- 125clk - enabled
- GMII to copper
- Fiber auto-detect - disabled
- Sleep mode - disabled

Ethernet signals from PHY are connected to B2B connector J1. To use Ethernet in your design, GigaBee module should be connected to the carrier board, which have Ethernet magnetics and RJ45 connector. TE0603 carrier board can be used to access Ethernet capabilities of GigaBee XC6SLX series modules.

For correct operation of the Marvell PHY it is required that PHY Reset pin sees valid low level each time power is applied and also during any brownout situations where system Power is removed for short time, but some pins are not at valid logic levels.

Solutions:

1) if GbE PHY is not used PHY reset pin can be tied off to GND
2) if PLL is used from PHY clock, then PLL "locked" output can be used to reset PHY - as long PLL is not locked, it will keep PHY in reset
3) Reset pulse generation circuit clocked from FPGA internal configuration clock, this circuit can force PHY reset pin to low when external clock from PHY is not available
4) any custom Reset circuit that is guaranteed to drive PHY reset to low level at least once after FPGA configuration when PHY clock is not running.
5) any user logic that is guaranteed to drive PHY reset low after FPGA configuration (without using PHY clock).

Explanation: Marvell PHY samples the MODE pins ONLY when it sees low level on PHY reset input, it does not sample those pins during short power off situations (if the reset pin holds high level because of pin capacitance and high impedance of the pins)! So it is possible that the PHY mode is reset, but the mode pins are not sampled again - this yields in mode setting where 125MHz reference clock from PHY is not available.

2.9 Oscillators

The module has one 25 MHz oscillator for Ethernet PHY (U9). Ethernet PHY provides clock multiplication and resulting 125 MHz clock acts as a system and user clock for the FPGA (FPGA input pin AA12).

Note: For correct generation start, PHY should receive reset pulse. Recommended way to do it it's to connect PHY reset signal (ETHERNET_PHY_RST_N) to LOCKED output of corresponding DCM (DCM which use 125 MHz from PHY).

The module also provides the footprint for custom 3.3 V single-ended oscillator (U12) which can be installed as an option (FPGA input pin Y13).

2.10 User LED

The module contains one user active-low LED connected to FPGA output pin T20. To access more LEDs, use a carrier board and drive FPGA signals connected to B2B connectors. As LED connected to FPGA bank with configurable VCCIO to light LED FPGA pin should in '0' (low) state. To disable LED FPGA pin should be in 'Z' (High impedance).

2.11 Watchdog

GigaBee XS6LX has a watchdog timer that is periodically triggered by a positive or negative transition of the WDI (watchdog input) line (FPGA pin V9). When the supervising system fails to re-trigger the watchdog circuit within the time-out interval (min 1.1 s, typ 1.6 s, max 2.3 s), the /WDO (watchdog output) line becomes active (low). This event also re-initializes the watchdog timer.

If zero-resistors R2 is not assembled, the watchdog is disabled (alternate assembly).

If zero-resistors R2 is assembled, the watchdog can be enabled (standard assembly). In this case there is still two options:

To **enable** the watchdog, after module power-up, drive the WDI signal to generate at least one transition (no matter positive or negative).

To keep watchdog **disabled**, set WDI FPGA signal output to high-impedance. One way to reach this goal is to leave FPGA pin V9 (label IO_L50N_2) undeclared in user constrains file (UCF) and set “unused IOB pins” to “float” in the Xilinx Project Navigator options, see Fig. 12.

(Project properties > Configuration options > Unused IOB Pins > Float).

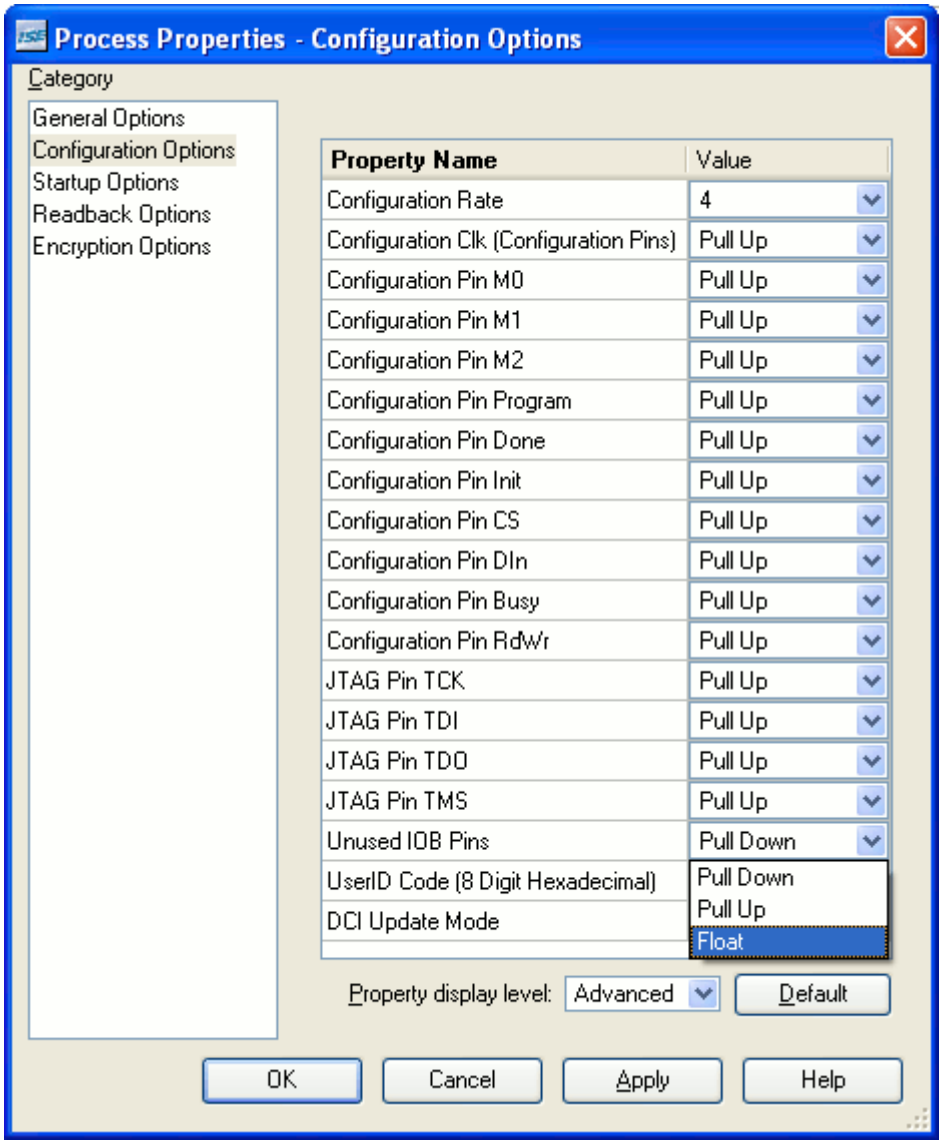

Figure 12: Unused IOB Pins option selection

In the standard assembly, the /WDO (watchdog output) line is left unconnected[3] and the only possibility to reset the module is by driving the /MR (master reset) line active (low) through pin 18 of connector J2.

In the alternate assembly, the /WDO (watchdog output) line is connected through zero-resistor R3 to /MR (master reset) line.

If alternate assembly is used, pin 18 of connector J2 must be left unconnected.

3 Configuration Options

The FPGA on GigaBee XC6SLX board can be configured by means of the following devices:

- Xilinx download cable (JTAG)
- SPI Flash memory

3.1 JTAG Configuration

The FPGA can be configured through the JTAG interface. JTAG signals are connected to B2B connector J2. When GigaBee XC6SLX board is used with the TE0603 carrier board, the JTAG interface can be accessed via connectors J5 and J6 on the carrier board.

3.2 Flash Configuration

Default configuration option for FPGA is “Master Serial/SPI”. The bit-stream for the FPGA is stored in a serial Flash chip (U11). See chapter 2.7 Flash Memory for additional information.

3.3 eFUSE Programming

eFUSE programming feature is not directly supported by GigaBee XC6SLX modules, but it is possible to use it. To program eFUSE, please follow the steps below:

- Connect VCCAUX to 3.3V power rail.

  On TE0603 it can be done by connecting J5 pin 2 or J6 “VREF” (VCCAUX) to J1 any pin from 1,2,3,4 (3.3V). See Figure 13.

- Program eFUSE using JTAG cable and iMPACT software.
- Remove power supply connections to VCCAUX

3 Resistor R3 is not populated.

4.1 Pin Labelling

FPGA user signals connected to B2B connectors are characterized by the "B2B_Bx_Lyy_p" naming convention, where:

- B2B defines a "FPGA to B2B" signal type;
- Bx defines the FPGA bank (x = bank number);
- Lyy defines a differential pair or signal number (yy = pair number);
- p defines a differential signal polarity (P = positive, N = negative); single ended signals do not have this field.

Ethernet PHY signals use "PHY_name" naming conversions where "PHY" defines signal type "PHY to B2B" and "name" is PHY signal name.

Remaining signals use custom names.

4.2 Pin Numbering

Note that GigaBee XC6SLX have hermaphroditic B2B connectors. A feature of hermaphroditic connector numbering is that connected signal numbers don't match. Odd signals on module connect to even signals on baseboard. For example module signal 1 to baseboard signal 2, module signal 2 to baseboard signal 1, module signal 3 to baseboard signal 4 and so on.

4.3 Pin Types

Most pins of B2B connectors J1 and J2 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 8 different functional types of pins on the TE0600, as outlined in Table 10. In pin-out tables Table 11 and Table 12, the individual pins are colour-coded according to pin type as in Table 10.

type colour code	description
DIO[4]	Unrestricted, general-purpose differential user-I/O pin.
SIO	Unrestricted, general-purpose user-I/O pin.
CONFIG	Dedicated configuration signals.
PWRMGMT	Control and status signals for the power-saving Suspend mode.
JTAG	Dedicated JTAG signals.
GND	Dedicated ground pin. All must be connected.
TE	Trenz Electronic specific pin type. See the description of each pin in the user manual for additional information on the corresponding signals.
POW	Power signals.
SPI	SPI signals.
PHY	Ethernet PHY signals.

Table 10: TE0600 pin types

Note that some of Spartan-6 I/O types are partially compatible, so pins of compatible types can be used as inputs for signal of other type. For example pins from FPGA bank with 1.5V VCCO (IOSTANDARD = LVCMOS15) can be used as inputs for 1.2V, 1.8V, 2.5V and 3.3V signals.

See “Spartan-6 FPGA SelectIO Resources” page 38 for detailed information.

4 DIO pins can be used as SIO.

4.4 External Bank 2 differential clock connection

TE0600-02 module have optional connection to FPGA bank 2 differential clock input pins. To provide connection from B2B_B2_L41_P signal to Y13 FPGA pin, zero-resistor R69 should be soldered. To provide connection B2B_B2_L41_N signal to AB13 FPGA pin, zero-resistor R81 should be soldered. Note that in this case optional user oscillator U13 can't be used.

4.5 J1 Pin-out

J1 pin	Net	Type	FPGA pin	Net Length	J1 pin	Net	Type	FPGA pin	Net Length
1	3.3V	POW	-	-	2	GND	GND	-	-
3	3.3V	POW	-	-	4	PHY_MDI0_P	PHY	-	-
5	3.3V	POW	-	-	6	PHY_MDI0_N	PHY	-	-
7	3.3V	POW	-	-	8	GND	GND	-	-
9	3.3V	POW	-	-	10	PHY_MDI1_P	PHY	-	-
11	3.3V	POW	-	-	12	PHY_MDI1_N	PHY	-	-
13	3.3V	POW	-	-	14	PHY_AVDD	PHY	-	-
15	3.3V	POW	-	-	16	PHY_MDI2_P	PHY	-	-
17	PHY_L10	PHY	-	-	18	PHY_MDI2_N	PHY	-	-
19	PHY_L100	PHY	-	-	20	GND	GND	-	-
21	PHY_L1000	PHY	-	-	22	PHY_MDI3_P	PHY	-	-
23	PHY_DUP	PHY	-	-	24	PHY_MDI3_N	PHY	-	-
25	PHY_LED_TX	PHY	-	-	26	GND	GND	-	-
27	PHY_LED_RX	PHY	-	-	28	EN	TE	-	-
29	GND	GND	-	-	30	INIT	CONFIG	T6	-
31	B2B_B2_L57_N	DIO	AB4	8.66mm	32	B2B_B2_L32_N	SIO	AB11	8.12mm
33	B2B_B2_L57_P	DIO	AA4	9.84mm	34	GND	GND	-	-
35	B2B_B2_L49_N	DIO	AB6	8.66mm	36	B2B_B2_L60_P	DIO	T7	9.96mm
37	B2B_B2_L49_P	DIO	AA6	9.58mm	38	B2B_B2_L60_N	DIO	R7	11.16mm
39	2.5V	POW	-	-	40	B2B_B2_L59_N	DIO	R8	11.42mm
41	1.2V	POW	-	-	42	B2B_B2_L59_P	DIO	R9	11.36mm
43	1.2V	POW	-	-	44	GND	GND	-	-
45	B2B_B2_L48_N	DIO	AB7	9.98mm	46	B2B_B2_L44_N	DIO	Y10	11.34mm
47	B2B_B2_L48_P	DIO	Y7	10.98mm	48	B2B_B2_L44_P	DIO	W10	10.21mm
49	B2B_B2_L45_N	DIO	AB8	10.60mm	50	B2B_B2_L42_N	DIO	W11	7.52mm
51	B2B_B2_L45_P	DIO	AA8	11.053mm	52	B2B_B2_L42_P	DIO	V11	8.36mm
53	GND	GND	-	-	54	GND	GND	-	-
55	B2B_B2_L43_N	DIO	AB9	13.75mm	56	B2B_B2_L18_P	DIO	V13	7.94mm
57	B2B_B2_L43_P	DIO	Y9	12.97mm	58	B2B_B2_L18_N	DIO	W13	6.96mm
59	B2B_B2_L41_N	DIO	AB10, AB13	10.33mm	60	B2B_B2_L8_N	DIO	U16	9.92mm
61	B2B_B2_L41_P	DIO	AA10, Y13	11.01mm	62	B2B_B2_L8_P	DIO	U17	9.94mm
63	GND	GND	-	-	64	GND	GND	-	-
65	B2B_B2_L21_P	DIO	Y15	13.12mm	66	B2B_B2_L11_P	DIO	V17	8.31mm
67	B2B_B2_L21_N	DIO	AB15	12.37mm	68	B2B_B2_L11_N	DIO	W17	7.29mm
69	B2B_B2_L15_P	DIO	Y17	14.20mm	70	B2B_B2_L6_P	DIO	W18	7.40mm
71	B2B_B2_L15_N	DIO	AB17	13.77mm	72	B2B_B2_L6_N	DIO	Y18	6.94mm
73	GND	GND	-	-	74	GND	GND	-	-
75	B2B_B2_L31_N	SIO	AB12	12.30mm	76	B2B_B2_L5_P	DIO	Y19	6.18mm

J1 pin	Net	Type	FPGA pin	Net Length	J1 pin	Net	Type	FPGA pin	Net Length
77	SUSPEND	SYS	N15	19.23mm	78	B2B_B2_L5_N	DIO	AB19	6.12mm
79	VBATT	CONFIG	R17	-	80	B2B_B2_L9_N	DIO	V18	8.43mm
81	VFS	CONFIG	P16	-	82	B2B_B2_L9_P	DIO	V19	8.36mm
83	RFUSE	CONFIG	P15	-	84	GND	GND	-	-
85	AWAKE	SYS	T19	14.15mm	86	B2B_B2_L4_N	DIO	T17	11.88mm
87	CSO_B	SPI	T5	-	88	B2B_B2_L4_P	DIO	T18	11.96mm
89	GND	GND	-	-	90	GND	GND	-	-
91	CCLK	SPI	Y21	-	92	B2B_B2_L29_N	SIO	Y12	13.58mm
93	MISO	SPI	AA20	-	94	B2B_B2_L10_N	DIO	R15	17.01mm
95	MOSI	SPI	AB20	-	96	B2B_B2_L10_P	DIO	R16	16.97mm
97	MISO3	SPI	U13	-	98	B2B_B2_L2_N	DIO	AB21	5.06mm
99	MISO2	SPI	U14	-	100	B2B_B2_L2_P	DIO	AA21	6.19mm

Table 11: J1 pin-out

4.6 J2 Pin-out

J2 pin	Net	Type	FPGA pin	Net Length	J2 pin	Net	Type	FPGA pin	Net Length
1	VCCIO0	POW	-	-	2	3.3V	POW	-	-
3	VCCIO0	POW	-	-	4	3.3V	POW	-	-
5	VCCIO0	POW	-	-	6	3.3V	POW	-	-
7	VCCIO0	POW	-	-	8	3.3V	POW	-	-
9	VCCIO0	POW	-	-	10	3.3V	POW	-	-
11	B2B_PROGB	CONFIG	-	-	12	3.3V	POW	-	-
13	HSWAPEN	CONFIG	A3	-	14	B2B_B0_L1	SIO	A4	9.017mm
15	B2B_B3_L60_N	DIO	B1	5.44mm	16	PFI	TE	-	-
17	B2B_B3_L60_P	DIO	B2	5.27mm	18	/MR	TE	-	-
19	1.5V	POW	-	-	20	GND	GND	-	-
21	B2B_B3_L9_N	DIO	T3	19.36mm	22	B2B_B0_L2_P	DIO	C5	10.17mm
23	B2B_B3_L9_P	DIO	T4	18.76mm	24	B2B_B0_L2_N	DIO	A5	9.60mm
25	B2B_B0_L3_P	DIO	D6	6.76mm	26	B2B_B0_L4_N	DIO	A6	7.65mm
27	B2B_B0_L3_N	DIO	C6	5.66mm	28	B2B_B0_L4_P	DIO	B6	8.71mm
29	GND	GND	-	-	30	GND	GND	-	-
31	B2B_B3_L59_P	DIO	J7	11.90mm	32	B2B_B0_L5_N	DIO	A7	8.59mm
33	B2B_B3_L59_N	DIO	H8	11.71mm	34	B2B_B0_L5_P	DIO	C7	9.54mm
35	B2B_B0_L32_P	DIO	D7	6.93mm	36	B2B_B0_L6_N	DIO	A8	7.42mm
37	B2B_B0_L32_N	DIO	D8	6.87mm	38	B2B_B0_L6_P	DIO	B8	8.43mm
39	GND	GND	-	-	40	GND	GND	-	-
41	B2B_B0_L7_N	DIO	C8	6.62mm	42	B2B_B0_L8_N	DIO	A9	9.28mm
43	B2B_B0_L7_P	DIO	D9	6.71mm	44	B2B_B0_L8_P	DIO	C9	9.92mm
45	B2B_B0_L33_N	DIO	C10	5.66mm	46	B2B_B0_L34_N	DIO	A10	7.58mm
47	B2B_B0_L33_P	DIO	D10	6.76mm	48	B2B_B0_L34_P	DIO	B10	8.60mm
49	GND	GND	-	-	50	GND	GND	-	-
51	B2B_B0_L36_P	DIO	D11	6.76mm	52	B2B_B0_L35_N	DIO	A11	8.89mm
53	B2B_B0_L36_N	DIO	C12	5.87mm	54	B2B_B0_L35_P	DIO	C11	9.92mm
55	B2B_B0_L49_P	DIO	D14	6.96mm	56	B2B_B0_L37_N	DIO	A12	7.52mm
57	B2B_B0_L49_N	DIO	C14	5.96mm	58	B2B_B0_L37_P	DIO	B12	8.74mm

J2 pin	Net	Type	FPGA pin	Net Length	J2 pin	Net	Type	FPGA pin	Net Length
59	GND	GND	-	-	60	GND	GND	-	-
61	B2B_B0_L62_P	DIO	D15	7.44mm	62	B2B_B0_L38_N	DIO	A13	8.38mm
63	B2B_B0_L62_N	DIO	C16	6.95mm	64	B2B_B0_L38_P	DIO	C13	9.87mm
65	B2B_B0_L66_P	DIO	E16	8.07mm	66	B2B_B0_L50_N	DIO	A14	7.66mm
67	B2B_B0_L66_N	DIO	D17	6.96mm	68	B2B_B0_L50_P	DIO	B14	8.87mm
69	GND	GND	-	-	70	GND	GND	-	-
71	B2B_B1_L10_P	DIO	F16	9.56mm	72	B2B_B0_L51_N	DIO	A15	10.22mm
73	B2B_B1_L10_N	DIO	F17	8.85mm	74	B2B_B0_L51_P	DIO	C15	10.67mm
75	B2B_B1_L9_P	DIO	G16	10.59mm	76	B2B_B0_L63_N	DIO	A16	7.95mm
77	B2B_B1_L9_N	DIO	G17	10.23mm	78	B2B_B0_L63_P	DIO	B16	9.12mm
79	GND	GND	-	-	80	GND	GND	-	-
81	B2B_B1_L21_N	DIO	J16	13.22mm	82	B2B_B0_L64_N	DIO	A17	9.55mm
83	B2B_B1_L21_P	DIO	K16	14.41mm	84	B2B_B0_L64_P	DIO	C17	10.25mm
85	B2B_B1_L61_P	DIO	L17	14.89mm	86	B2B_B0_L65_N	DIO	A18	8.51mm
87	B2B_B1_L61_N	DIO	K18	13.59mm	88	B2B_B0_L65_P	DIO	B18	9.29mm
89	GND	GND	-	-	90	GND	GND	-	-
91	VCCAUX	POW	-	-	92	B2B_B1_L20_P	DIO	A20	8.02mm
93	TMS	JTAG	C18	-	94	B2B_B1_L20_N	DIO	A21	7.82mm
95	TDI	JTAG	E18	-	96	B2B_B1_L19_P	DIO	B21	9.63mm
97	TDO	JTAG	A19	-	98	B2B_B1_L19_N	DIO	B22	9.06mm
99	TCK	JTAG	G15	-	100	B2B_B1_L59	SIO	P19	27.19mm

Table 12: J2 pin-out

4.7 Signal Integrity Considerations

Traces of differential signals pairs are routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length[5]. For applications where traces length has to be matched or timing differences have to be compensated, Table 11 and Table 12 list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 100 ohm. Single ended traces are routed with 60 ohm impedance.

An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.

5 Module revisions and assembly variants

Module revision coded by 4 FPGA BR[3:0] pins, which can be read by FPGA firmware. All these pins should be configures to have internal PULLUP.

5 Difference in signal lines length is negligible for used signal frequency.

Signal FPGA pin	BR3 R19	BR2 P18	BR1 N16	BR0 P17
Revision 01	1	1	1	1
Revision 02	1	1	1	0

Table 13: Board revisions pin coding

Main differences between 01 and 02 revisions:

- More powerful regulators for 1.2V and 1.5V rails
- VCCAUX separated from 2.5V power rail
- 128Mbit SPI Flash
- Additional secure 1Kbit EEPROM
- Optional B2B connection to bank 2 differential clock input

Module assembly variants coded by 4 zero ohm resistors, connected to FPGA AV[3:0] pins. All these pins should be configures to have internal PULLUP.

Signal FPGA pin	AV3 M18	AV2 M17	AV1 V20	AV0 U19	Speed grade	SDRAM	Temp grade
TE0600-02[V|B]	0	0	0	0	2	2x128MBit	C
TE0600-02[V|B]I	0	0	0	1	2	2x128MBit	I
TE0600-02[V|B]F	0	0	1	0	3	2x128MBit	C
TE0600-02[V|B]IF	0	0	1	1	3	2x128MBit	I
TE0600-02[V|B]MF	0	1	0	0	3	2x512MBit	C

Table 14: Assembly variants pin coding

6 Related Materials and References

The following documents provide supplementary information useful with this user manual.

6.1 Data Sheets

- Xilinx DS160: Spartan-6 Family Overview
  This overview outlines the features and product selection of the Spartan®-6 family.
  http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf
- Xilinx DS162: Spartan-6 FPGA Data Sheet: DC and Switching Characteristics
  This data sheet contains the DC and switching characteristic specifications for the Spartan®-6 family.
  http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf
- Samtec Razor Beam LSHM series overview.
  http://www.samtec.com/LSHM
- Maxim DS2502-E48 product overview.

  http://www.maxim-ic.com/datasheet/index.mvp/id/3748
- Winbond W25Q128BV product overview.

  http://www.winbond.com/hq/enu/ProductAndSales/ProductLines/FlashMemory/SerialFlash/W25Q128BV.htm
- Maxim DS2432 product page.

  http://www.maximintegrated.com/datasheet/index.mvp/id/2914

6.2 Documentation Archives

- Xilinx Spartan-6 Documentation
  http://www.xilinx.com/support/documentation/spartan-6.htm
- Xilinx Documentation
  http://www.xilinx.com/documentation/
  http://www.xilinx.com/support/documentation/
- Trenz Electronic GigaBee Series Documentation
  http://docs.trenz-electronic.de/Trenz_Electronic/products/TE0600-GigaBee_series/

6.3 User Guides

- Xilinx UG380: Spartan-6 FPGA Configuration User Guide
  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.
  http://www.xilinx.com/support/documentation/user_guides/ug380.pdf
- Xilinx UG381: Spartan-6 FPGA SelectIO Resources

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