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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details

Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Spartan-6 LX-100
Co-Processor	-
Speed	125MHz
Flash Size	16MB
RAM Size	1GB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0600-02bm

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- Maximum height on carrier board surface: ≈ 13 mm (standard connectors)

- Minimum height on carrier board surface: ≈ 5 mm (standard connectors)

- Weight: 17.2 ± 0.1 g

- Temperature grades:

- commercial (C-type FPGA device)

- industrial (I-type FPGA device)

1.2 Dimensions
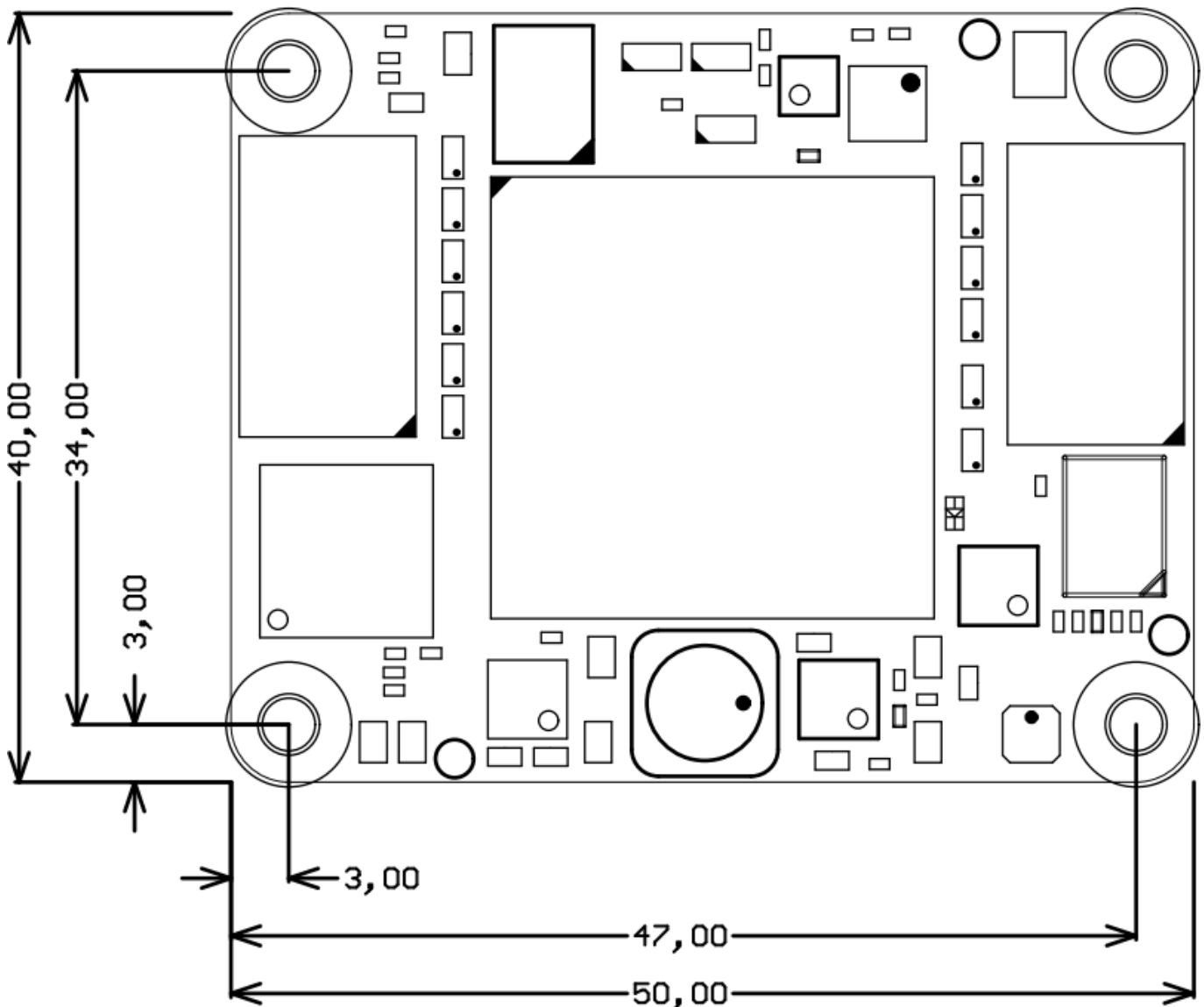
Figure 3: GigaBee board dimensions (top view)

GigaBee XC6SLX can reach a minimum vertical height of about 8 mm, if B2B

1.5 V, see Chapter 2.2.3.6 VCCIO0 Power Rail. Bank 1 VCCIO supply voltage is configured to 1.5 V to communicate with DDR3 SDRAM memory chip.[1]

2.2.3 On-board Power Rails

GigaBee XC6SLX has the following power rails on-board.

2.2.3.1 3.3V Power Rail

It is the main internal power rail and must be supplied from an external power source.

It supplies the other following power rails:

- 1.2V / 4 A on-board high-efficiency switching voltage regulator;
- 1.5V / 1.5 A on-board high-efficiency switching voltage regulator;
- 2.5V 0.8 A linear voltage regulator;
- VCCIO0 power rail (option) (if zero-resistor R80 is not populated and zero-resistor R79 is populated).

2.2.3.2 1.2V Power Rail

It is converted from the 3.3V rail by a switching voltage regulator and can provide up to 4.0 A to:

- FPGA V_{CCINT} power supply pins;
- Ethernet PHY;
- J1 connector.

2.2.3.3 1.5V Power Rail

It is converted from the 3.3V rail by a switching voltage regulator and can provide up to 1.5 A to:

- DDR3 SDRAM;
- Vref1 / Vref2 DDR3 SDRAM reference voltages;
- FPGA bank 3 V_{CCO};
- J1 connector.

2.2.3.4 2.5V Power Rail

It is converted from the 3.3V rail by a linear voltage regulator and can provide up to 0.8 A to:

- VCCAUX power rail;
- Ethernet physical layer;
- J1 connector;

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1   By special request modules can be supplied without DDR3 SDRAM chips. Contact Trenz Electronic support for details

Table 3 summarizes power rails information.

power-rail name	nominal voltage(V)	maximum current (A)	power source	system supply	user supply
3.3V	3.3	2.4 (3.3 option)	J1, J2	module	J1 (≤1.2 A) J2 (≤1.2 A, ≤2.1 option)
2.5V	2.5	0.8	3.3V ▸ linear	Ethernet	J1 (≤0.3 A) J2 (option)
1.5V	1.5	1.5	3.3V ▸ switch.	DDR3 SDRAM VCCO (1+3)	J1 (≤0.3 A)
1.2V	1.2	4.0	3.3V ▸ switch.	VCCINT Ethernet	J1 (≤0.6 A)
VCCAUX	2.5	0.8	3.3V ▸ linear	FPGA	J2 (≤0.3 A)
VCCCIO0	1.2, 1.5, 1.8, 2.5, 3.3	0.9	J2	VCCO (0)	J2 (≤0.9 A)

Table 3: On-board power rails summary

2.3 Power Supervision

2.3.1 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the supply rail remains below the threshold voltage (2.93 volt). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset prior to a regular system start-up. The typical delay time t_d of 200 ms starts after the supply rail has risen above the threshold voltage.
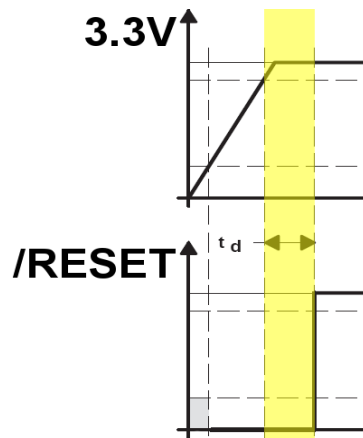
Figure 7: Reset on power-on
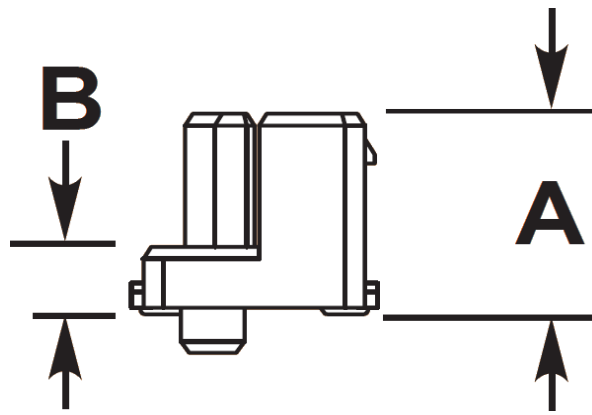
Figure 10: A and B features of Samtec Razor Beam LSHM series
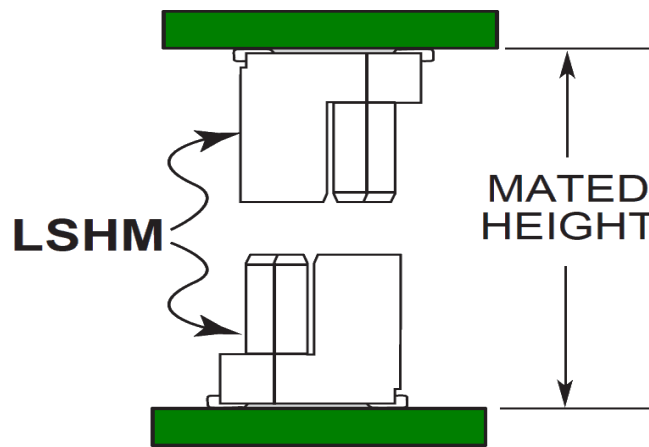
Figure 11: Definition of mated height for Samtec Razor Beam LSHM series.

The standard connector mounted on the GigaBee XC6SLX is Samtec Razor Beam LSHM-150-04.0-L-DV-A-S-K-TR (lead style: –04.0, tail option: vertical, shield option: with shield).

Trenz Electronic recommends the same part as mating connector, due to its self-mating capability.

The Samtec Razor Beam LSHM series offers a variety of mated heights form 5.0 mm to 12.0 mm. Two mated standard GigaBee XC6SLX connectors have a typical mated height of 8.0 mm. Processing conditions will affect the following heights.

standard connector lead style	mating connector lead style	mated height [mm]	min. height from carrier board [mm]	max. height on carrier board [mm]
−04.0	−02.5	6.5	≈ 3.5	≈ 11.5
−04.0	−03.0	7.0	≈ 4.0	≈ 12.0
−04.0	**−04.0**	**8.0**	**≈ 5.0**	**≈ 13.0**
−04.0	−06.0	10.0	≈ 7.0	≈ 15.0

Table 5: Samtec Razor Beam LSHM mated heights

Ordering codes for connectors J1 and J2 used in GigaBee XC6SLX board, and their mating connectors are given in Table 6.

lead style	gender	Samtec	Trenz Electronic
−02.5	hermaphroditic	LSHM-150-02.5-L-DV-A-S-K-TR	23836
−03.0	hermaphroditic	LSHM-150-03.0-L-DV-A-S-K-TR	23837
−04.0	hermaphroditic	LSHM-150-04.0-L-DV-A-S-K-TR	23838
−06.0	hermaphroditic	LSHM-150-06.0-L-DV-A-S-K-TR	23839

Table 6: Ordered codes of recommended B2B connectors

2.4.1 Connector Speed Rating

Samtec provides speed rating data for the Samtec Razor Beam LSHM connector system. The data presented in Table 7 are applicable only to the maximum and minimum mated heights. The speed rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signalling environment.

mated height	5 mm	12 mm
single-ended signalling	11.5 GHz 23.0 Gb/s	7.5 GHz 15.0 Gb/s
differential pair signalling	7.0 GHz 14.0 Gb/s	6.5 GHz 13.0 Gb/s

Table 7: Connectors speed rating

More details can be found in the Samtec Razor Beam LSHM series overview ("High Speed Characterization Reports").

2.5 EPROM

GigaBee XC6SLX board contains a Maxim DS2502-E48 node address chip with factory-programmed valid MAC-48 address and 768 bits of OTP-EPROM memory for user data.

Address chip provide convenient data access through 1-Wire interface up to 16.3 kbps (FPGA pin T11).

More information can be found in the Maxim DS2502-E48 product overwiew.

Additional 1Kb protected 1-Wire EEPROM with SHA-1 engine DS2432 accessible via the same line.

More information can be found at the Maxim DS2432 product page.

2.6 DDR3 SDRAM Memory

The board contains two 1 Gb (128 MB) or 4 Gb (512 MB) DDR3 SDRAM chips. Data width of each chip is 16 bit. DDR3 memory connected to FPGA bank 1 and FPGA bank 3. Spartan-6 Memory controller Blocks operations can be merged to implement effective 32-bit memory interface. Refer Xilinx XAPP496 for detailed information.

2.7 Flash Memory

GigaBee XC6SLX board contains 128 Mb (16 MB) serial flash memory chip Winbond W25Q128BV (U11). This serial flash chip can operate as general SPI memory mode and in double or quad modes. Usage of dual and quad modes increase bandwidth up to 40 MB/s.

For more information see Winbond W25Q128BV product overview.

Flash can be programmed in several ways:

● Direct SPI programming via J1 connector.

● Indirect SPI programming via FPGA pins, controlled by JTAG.

● Direct SPI programming by FPGA, using SPI core.

Serial flash is connected to FPGA bank 2 and B2B connector J1; used pins are listed in Table 8.

Flash signal	FPGA pin	J1 pin
/CS	T5	87
CLK	Y21	91
DI(IO0)	AB20	95
DO(IO1)	AA20	93
/WP(IO2)	U14	99
/HOLD(IO3)	U13	97

Table 8: Serial flash signals connection

2.8 Ethernet

The board contains a Marvell Alaska Ethernet PHY chip (88E1111) operating at 10/100/1000 Mb/s. The board supports GMII interface mode with the FPGA. Configuration details:

● PHY address – 00111

● Advertise pause

● Auto Neg

● Advertise all caps

● Prefer slave

● Auto crossover

● 125clk - enabled

● GMII to copper

● Fiber auto-detect - disabled

● Sleep mode - disabled

Ethernet signals from PHY are connected to B2B connector J1. To use Ethernet in your design, GigaBee module should be connected to the carrier board, which have Ethernet magnetics and RJ45 connector. TE0603 carrier board can be used to access Ethernet capabilities of GigaBee XC6SLX series modules.

For correct operation of the Marvell PHY it is required that PHY Reset pin sees valid low level each time power is applied and also during any brownout situations where system Power is removed for short time, but some pins are not at valid logic levels.

Solutions:

1) if GbE PHY is not used PHY reset pin can be tied off to GND
2) if PLL is used from PHY clock, then PLL "locked" output can be used to reset PHY - as long PLL is not locked, it will keep PHY in reset
3) Reset pulse generation circuit clocked from FPGA internal configuration clock, this circuit can force PHY reset pin to low when external clock from PHY is not available
4) any custom Reset circuit that is guaranteed to drive PHY reset to low level at least once after FPGA configuration when PHY clock is not running.
5) any user logic that is guaranteed to drive PHY reset low after FPGA configuration (without using PHY clock).

Explanation: Marvell PHY samples the MODE pins ONLY when it sees low level on PHY reset input, it does not sample those pins during short power off situations (if the reset pin holds high level because of pin capacitance and high impedance of the pins)! So it is possible that the PHY mode is reset, but the mode pins are not sampled again - this yields in mode setting where 125MHz reference clock from PHY is not available.

2.9 Oscillators

The module has one 25 MHz oscillator for Ethernet PHY (U9). Ethernet PHY provides clock multiplication and resulting 125 MHz clock acts as a system and user clock for the FPGA (FPGA input pin AA12).

Note: For correct generation start, PHY should receive reset pulse. Recommended way to do it it's to connect PHY reset signal (ETHERNET_PHY_RST_N) to LOCKED output of corresponding DCM (DCM which use 125 MHz from PHY).

The module also provides the footprint for custom 3.3 V single-ended oscillator (U12) which can be installed as an option (FPGA input pin Y13).

2.10 User LED

The module contains one user active-low LED connected to FPGA output pin T20. To access more LEDs, use a carrier board and drive FPGA signals connected to B2B connectors. As LED connected to FPGA bank with configurable VCCIO to light LED FPGA pin should in '0' (low) state. To disable LED FPGA pin should be in 'Z' (High impedance).
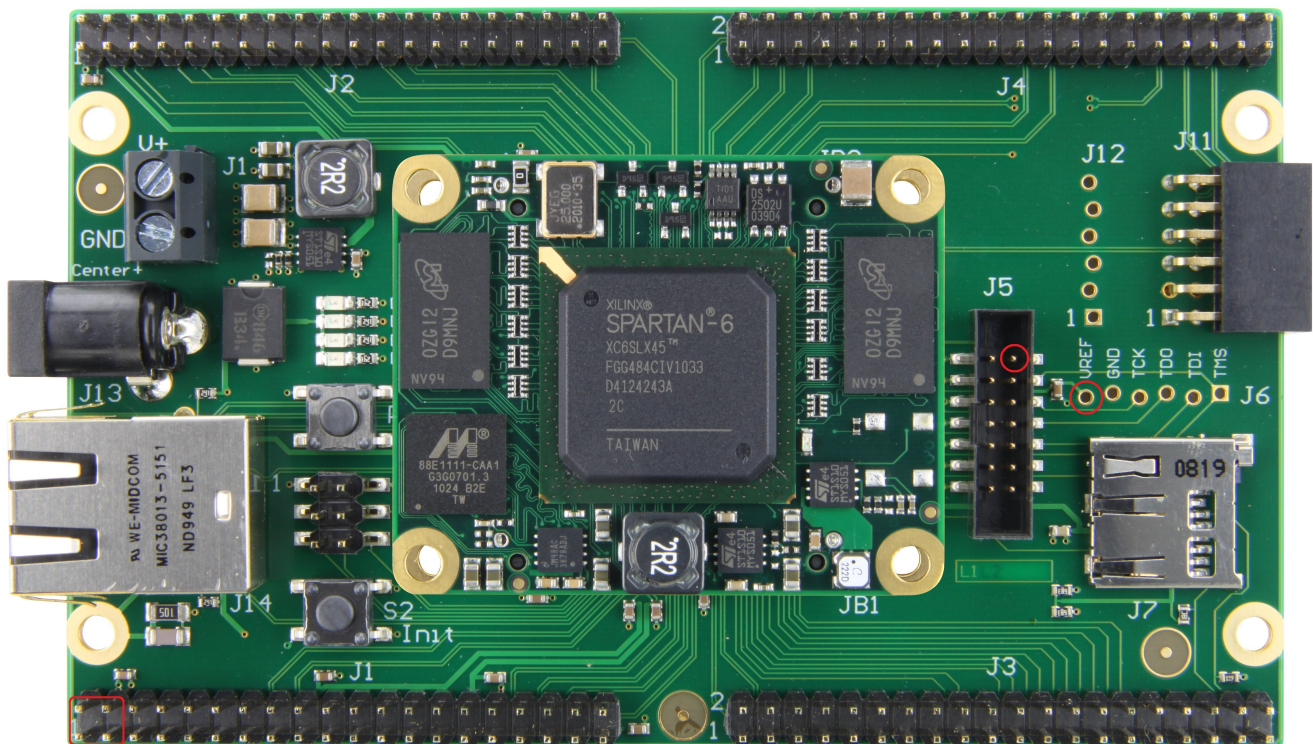
Figure 13: eFUSE Powering

4 B2B Connectors Pin Descriptions

This section describes how the various pins on B2B connectors J1 and J2 connects to TE0600 on-board components. There are five main signal types connected to B2B connectors:

- FPGA users signals;
- FPGA system signals;
- Power signals;
- Ethernet PHY signals;
- Other system signals.

FPGA Bank	Single-ended	Differential	Total	VCCIO
Bank 0	1	22	45	VCCIO 0 (3.3 V)
Bank 1	1	6	13	VCCIO 1 (1.5 V)
Bank 2	3	21	45	3.3 V
Bank 3	0	3	6	1.5 V
	5	52	109	

Table 9: B2B signals count

4.1 Pin Labelling

FPGA user signals connected to B2B connectors are characterized by the "B2B_Bx_Lyy_p" naming convention, where:

- B2B defines a "FPGA to B2B" signal type;

- Bx defines the FPGA bank (x = bank number);

- Lyy defines a differential pair or signal number (yy = pair number);

- p defines a differential signal polarity (P = positive, N = negative); single ended signals do not have this field.

Ethernet PHY signals use "PHY_name" naming conversions where "PHY" defines signal type "PHY to B2B" and "name" is PHY signal name.

Remaining signals use custom names.

4.2 Pin Numbering

Note that GigaBee XC6SLX have hermaphroditic B2B connectors. A feature of hermaphroditic connector numbering is that connected signal numbers don't match. Odd signals on module connect to even signals on baseboard. For example module signal 1 to baseboard signal 2, module signal 2 to baseboard signal 1, module signal 3 to baseboard signal 4 and so on.

4.3 Pin Types

Most pins of B2B connectors J1 and J2 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 8 different functional types of pins on the TE0600, as outlined in Table 10. In pin-out tables Table 11 and Table 12, the individual pins are colour-coded according to pin type as in Table 10.

type colour code	description
DIO[4]	Unrestricted, general-purpose differential user-I/O pin.
SIO	Unrestricted, general-purpose user-I/O pin.
CONFIG	Dedicated configuration signals.
PWRMGMT	Control and status signals for the power-saving Suspend mode.
JTAG	Dedicated JTAG signals.
GND	Dedicated ground pin. All must be connected.
TE	Trenz Electronic specific pin type. See the description of each pin in the user manual for additional information on the corresponding signals.
POW	Power signals.
SPI	SPI signals.
PHY	Ethernet PHY signals.

Table 10: TE0600 pin types

Note that some of Spartan-6 I/O types are partially compatible, so pins of compatible types can be used as inputs for signal of other type. For example pins from FPGA bank with 1.5V VCCO (IOSTANDARD = LVCMOS15) can be used as inputs for 1.2V, 1.8V, 2.5V and 3.3V signals.

See "Spartan-6 FPGA SelectIO Resources" page 38 for detailed information.

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4   DIO pins can be used as SIO.

4.4 External Bank 2 differential clock connection

TE0600-02 module have optional connection to FPGA bank 2 differential clock input pins. To provide connection from B2B_B2_L41_P signal to Y13 FPGA pin, zero-resistor R69 should be soldered. To provide connection B2B_B2_L41_N signal to AB13 FPGA pin, zero-resistor R81 should be soldered. Note that in this case optional user oscillator U13 can't be used.

4.5 J1 Pin-out

J1 pin	Net	Type	FPGA pin	Net Length	J1 pin	Net	Type	FPGA pin	Net Length
1	3.3V	POW	-	-	2	GND	GND	-	-
3	3.3V	POW	-	-	4	PHY_MDI0_P	PHY	-	-
5	3.3V	POW	-	-	6	PHY_MDI0_N	PHY	-	-
7	3.3V	POW	-	-	8	GND	GND	-	-
9	3.3V	POW	-	-	10	PHY_MDI1_P	PHY	-	-
11	3.3V	POW	-	-	12	PHY_MDI1_N	PHY	-	-
13	3.3V	POW	-	-	14	PHY_AVDD	PHY	-	-
15	3.3V	POW	-	-	16	PHY_MDI2_P	PHY	-	-
17	PHY_L10	PHY	-	-	18	PHY_MDI2_N	PHY	-	-
19	PHY_L100	PHY	-	-	20	GND	GND	-	-
21	PHY_L1000	PHY	-	-	22	PHY_MDI3_P	PHY	-	-
23	PHY_DUP	PHY	-	-	24	PHY_MDI3_N	PHY	-	-
25	PHY_LED_TX	PHY	-	-	26	GND	GND	-	-
27	PHY_LED_RX	PHY	-	-	28	EN	TE	-	-
29	GND	GND	-	-	30	INIT	CONFIG	T6	-
31	B2B_B2_L57_N	DIO	AB4	8.66mm	32	B2B_B2_L32_N	SIO	AB11	8.12mm
33	B2B_B2_L57_P	DIO	AA4	9.84mm	34	GND	GND	-	-
35	B2B_B2_L49_N	DIO	AB6	8.66mm	36	B2B_B2_L60_P	DIO	T7	9.96mm
37	B2B_B2_L49_P	DIO	AA6	9.58mm	38	B2B_B2_L60_N	DIO	R7	11.16mm
39	2.5V	POW	-	-	40	B2B_B2_L59_N	DIO	R8	11.42mm
41	1.2V	POW	-	-	42	B2B_B2_L59_P	DIO	R9	11.36mm
43	1.2V	POW	-	-	44	GND	GND	-	-
45	B2B_B2_L48_N	DIO	AB7	9.98mm	46	B2B_B2_L44_N	DIO	Y10	11.34mm
47	B2B_B2_L48_P	DIO	Y7	10.98mm	48	B2B_B2_L44_P	DIO	W10	10.21mm
49	B2B_B2_L45_N	DIO	AB8	10.60mm	50	B2B_B2_L42_N	DIO	W11	7.52mm
51	B2B_B2_L45_P	DIO	AA8	11.053mm	52	B2B_B2_L42_P	DIO	V11	8.36mm
53	GND	GND	-	-	54	GND	GND	-	-
55	B2B_B2_L43_N	DIO	AB9	13.75mm	56	B2B_B2_L18_P	DIO	V13	7.94mm
57	B2B_B2_L43_P	DIO	Y9	12.97mm	58	B2B_B2_L18_N	DIO	W13	6.96mm
59	B2B_B2_L41_N	DIO	AB10, AB13	10.33mm	60	B2B_B2_L8_N	DIO	U16	9.92mm
61	B2B_B2_L41_P	DIO	AA10, Y13	11.01mm	62	B2B_B2_L8_P	DIO	U17	9.94mm
63	GND	GND	-	-	64	GND	GND	-	-
65	B2B_B2_L21_P	DIO	Y15	13.12mm	66	B2B_B2_L11_P	DIO	V17	8.31mm
67	B2B_B2_L21_N	DIO	AB15	12.37mm	68	B2B_B2_L11_N	DIO	W17	7.29mm
69	B2B_B2_L15_P	DIO	Y17	14.20mm	70	B2B_B2_L6_P	DIO	W18	7.40mm
71	B2B_B2_L15_N	DIO	AB17	13.77mm	72	B2B_B2_L6_N	DIO	Y18	6.94mm
73	GND	GND	-	-	74	GND	GND	-	-
75	B2B_B2_L31_N	SIO	AB12	12.30mm	76	B2B_B2_L5_P	DIO	Y19	6.18mm

J1 pin	Net	Type	FPGA pin	Net Length	J1 pin	Net	Type	FPGA pin	Net Length
77	SUSPEND	SYS	N15	19.23mm	78	B2B_B2_L5_N	DIO	AB19	6.12mm
79	VBATT	CONFIG	R17	-	80	B2B_B2_L9_N	DIO	V18	8.43mm
81	VFS	CONFIG	P16	-	82	B2B_B2_L9_P	DIO	V19	8.36mm
83	RFUSE	CONFIG	P15	-	84	GND	GND	-	-
85	AWAKE	SYS	T19	14.15mm	86	B2B_B2_L4_N	DIO	T17	11.88mm
87	CSO_B	SPI	T5	-	88	B2B_B2_L4_P	DIO	T18	11.96mm
89	GND	GND	-	-	90	GND	GND	-	-
91	CCLK	SPI	Y21	-	92	B2B_B2_L29_N	SIO	Y12	13.58mm
93	MISO	SPI	AA20	-	94	B2B_B2_L10_N	DIO	R15	17.01mm
95	MOSI	SPI	AB20	-	96	B2B_B2_L10_P	DIO	R16	16.97mm
97	MISO3	SPI	U13	-	98	B2B_B2_L2_N	DIO	AB21	5.06mm
99	MISO2	SPI	U14	-	100	B2B_B2_L2_P	DIO	AA21	6.19mm

Table 11: J1 pin-out

4.6 J2 Pin-out

J2 pin	Net	Type	FPGA pin	Net Length	J2 pin	Net	Type	FPGA pin	Net Length
1	VCCIO0	POW	-	-	2	3.3V	POW	-	-
3	VCCIO0	POW	-	-	4	3.3V	POW	-	-
5	VCCIO0	POW	-	-	6	3.3V	POW	-	-
7	VCCIO0	POW	-	-	8	3.3V	POW	-	-
9	VCCIO0	POW	-	-	10	3.3V	POW	-	-
11	B2B_PROGB	CONFIG	-	-	12	3.3V	POW	-	-
13	HSWAPEN	CONFIG	A3	-	14	B2B_B0_L1	SIO	A4	9.017mm
15	B2B_B3_L60_N	DIO	B1	5.44mm	16	PFI	TE	-	-
17	B2B_B3_L60_P	DIO	B2	5.27mm	18	/MR	TE	-	-
19	1.5V	POW	-	-	20	GND	GND	-	-
21	B2B_B3_L9_N	DIO	T3	19.36mm	22	B2B_B0_L2_P	DIO	C5	10.17mm
23	B2B_B3_L9_P	DIO	T4	18.76mm	24	B2B_B0_L2_N	DIO	A5	9.60mm
25	B2B_B0_L3_P	DIO	D6	6.76mm	26	B2B_B0_L4_N	DIO	A6	7.65mm
27	B2B_B0_L3_N	DIO	C6	5.66mm	28	B2B_B0_L4_P	DIO	B6	8.71mm
29	GND	GND	-	-	30	GND	GND	-	-
31	B2B_B3_L59_P	DIO	J7	11.90mm	32	B2B_B0_L5_N	DIO	A7	8.59mm
33	B2B_B3_L59_N	DIO	H8	11.71mm	34	B2B_B0_L5_P	DIO	C7	9.54mm
35	B2B_B0_L32_P	DIO	D7	6.93mm	36	B2B_B0_L6_N	DIO	A8	7.42mm
37	B2B_B0_L32_N	DIO	D8	6.87mm	38	B2B_B0_L6_P	DIO	B8	8.43mm
39	GND	GND	-	-	40	GND	GND	-	-
41	B2B_B0_L7_N	DIO	C8	6.62mm	42	B2B_B0_L8_N	DIO	A9	9.28mm
43	B2B_B0_L7_P	DIO	D9	6.71mm	44	B2B_B0_L8_P	DIO	C9	9.92mm
45	B2B_B0_L33_N	DIO	C10	5.66mm	46	B2B_B0_L34_N	DIO	A10	7.58mm
47	B2B_B0_L33_P	DIO	D10	6.76mm	48	B2B_B0_L34_P	DIO	B10	8.60mm
49	GND	GND	-	-	50	GND	GND	-	-
51	B2B_B0_L36_P	DIO	D11	6.76mm	52	B2B_B0_L35_N	DIO	A11	8.89mm
53	B2B_B0_L36_N	DIO	C12	5.87mm	54	B2B_B0_L35_P	DIO	C11	9.92mm
55	B2B_B0_L49_P	DIO	D14	6.96mm	56	B2B_B0_L37_N	DIO	A12	7.52mm
57	B2B_B0_L49_N	DIO	C14	5.96mm	58	B2B_B0_L37_P	DIO	B12	8.74mm

Signal FPGA pin	BR3 R19	BR2 P18	BR1 N16	BR0 P17
Revision 01	1	1	1	1
Revision 02	1	1	1	0

Table 13: Board revisions pin coding

Main differences between 01 and 02 revisions:

- More powerful regulators for 1.2V and 1.5V rails

- VCCAUX separated from 2.5V power rail

- 128Mbit SPI Flash

- Additional secure 1Kbit EEPROM

- Optional B2B connection to bank 2 differential clock input

Module assembly variants coded by 4 zero ohm resistors, connected to FPGA AV[3:0] pins. All these pins should be configures to have internal PULLUP.

Signal FPGA pin	AV3 M18	AV2 M17	AV1 V20	AV0 U19	Speed grade	SDRAM	Temp grade
TE0600-02[V|B]	0	0	0	0	2	2x128MBit	C
TE0600-02[V|B]I	0	0	0	1	2	2x128MBit	I
TE0600-02[V|B]F	0	0	1	0	3	2x128MBit	C
TE0600-02[V|B]IF	0	0	1	1	3	2x128MBit	I
TE0600-02[V|B]MF	0	1	0	0	3	2x512MBit	C

Table 14: Assembly variants pin coding

6 Related Materials and References

The following documents provide supplementary information useful with this user manual.

6.1 Data Sheets

- Xilinx DS160: Spartan-6 Family Overview
  This overview outlines the features and product selection of the Spartan®-6 family.
  http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf

- Xilinx DS162: Spartan-6 FPGA Data Sheet: DC and Switching Characteristics
  This data sheet contains the DC and switching characteristic specifications for the Spartan®-6 family.
  http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf

- Samtec Razor Beam LSHM series overview.
  http://www.samtec.com/LSHM

- Maxim DS2502-E48 product overview.

  http://www.maxim-ic.com/datasheet/index.mvp/id/3748

- Winbond W25Q128BV product overview.

  http://www.winbond.com/hq/enu/ProductAndSales/ProductLines/FlashMemory/SerialFlash/W25Q128BV.htm

- Maxim DS2432 product page.

  http://www.maximintegrated.com/datasheet/index.mvp/id/2914

6.2 Documentation Archives

- Xilinx Spartan-6 Documentation
  http://www.xilinx.com/support/documentation/spartan-6.htm

- Xilinx Documentation
  http://www.xilinx.com/documentation/
  http://www.xilinx.com/support/documentation/

- Trenz Electronic GigaBee Series Documentation
  http://docs.trenz-electronic.de/Trenz_Electronic/products/TE0600-GigaBee_series/

6.3 User Guides

- Xilinx UG380: Spartan-6 FPGA Configuration User Guide
  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.
  http://www.xilinx.com/support/documentation/user_guides/ug380.pdf

- Xilinx UG381: Spartan-6 FPGA SelectIO Resources

http://www.xilinx.com/support/documentation/user_guides/ug381.pdf

6.4 Design and Development Tools

- Xilinx ISE Design Suite
  http://www.xilinx.com/ISE/
  http://www.xilinx.com/tools/designtools.htm

- Xilinx ISE Design Suite (version archive)
  http://www.xilinx.com/download/
  http://www.xilinx.com/support/download/

- Xilinx ISE WebPACK
  http://www.xilinx.com/tools/webpack.htm
  http://www.xilinx.com/webpack/

6.5 Design Resources

- Trenz Electronic GigaBee Design Resources
  http://www.trenz-electronic.de/download/d0/Trenz_Electronic/d1/TE0600-GigaBee_series.html

- Trenz Electronic GigaBee Reference Designs
  https://github.com/Trenz-Electronic/
  https://github.com/Trenz-Electronic/TE-EDK-IP/
  https://github.com/Trenz-Electronic/TE060X-GigaBee-Reference-Designs/

6.6 Tutorials

- Xilinx UG695: ISE In-Depth Tutorial
  Chapter 8: Configuration Using iMPACT
  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/ise_tutorial_ug695.pdf

7 Glossary of Abbreviations and Acronyms

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

A CAUTION notice denotes a risk. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in a fault. (undesired condition that can lead to an error) Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

API	application programming interface
B2B	board-to-board
DSP	digital signal processing; digital signal processor
EDK	Embedded Development Kit
IOB	input / output blocks; I/O blocks
IP	intellectual property
ISP	In-System Programmability
OTP	one-time programmable
PB	push button
SDK	Software Development Kit
TE	Trenz Electronic
XPS	Xilinx Platform Studio

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