Trenz Electronic GmbH - TE0600-02I Datasheet

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Spartan-6 LX-45
Co-Processor	-
Speed	125MHz
Flash Size	16MB
RAM Size	256MB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0600-02i

Key Features

- Industrial-grade Xilinx Spartan-6 LX FPGA micromodule (LX45 / LX100 / LX150)
- 10/100/1000 tri-speed Gigabit Ethernet transceiver (PHY)
- 2 x 16-bit-wide 1 Gb (128 MB) or 4Gb (512 MB) DDR3 SDRAM
- 128Mb (16 MB) SPI Flash memory (for configuration and operation) accessible through:
- 1Kb Protected 1-Wire EEPROM with SHA-1 Engine
- JTAG port (SPI indirect)
- FPGA configuration through:
  - B2B connector
  - JTAG port
  - SPI Flash memory
- Plug-on module with 2 × 100-pin high-speed hermaphroditic strips
- Up to 52 differential, up to 109 single-ended (+ 1 dual-purpose) FPGA I/O pins available on B2B strips
- 4.0 A x 1.2 V power rail
- 1.5 A x 1.5 V power rail
- 125 MHz reference clock signal
- Single-ended custom oscillator (option)
- eFUSE bit-stream encryption (LX100 or larger)
- 1 user LED
- Evenly-spread supply pins for good signal integrity
- Other assembly options for cost or performance optimization available upon request.

connectors are not assembled. The maximum component height on the module board on the top side is about 3.5 mm. The maximum component height on the module board on the bottom side is about 3.0 mm.

The typical minimum and maximum height from the carrier board surface, of a GigaBee XC6SLX when it mounted on a carrier board, is respectively about 5.0 mm and about 13 mm.

GigaBee XC6SLX has 4 mounting holes, one in each corner. The module can be fixed by screwing M3 screws (ISO 262) onto a carrier board through those mounting holes.

GigaBee XC6SLX weighs between 17.1 and 17.3 g with standard connectors.

1.3 Power Consumption

Power consumption of GigaBee XC6SLX modules highly depend on the FPGA design implemented. Some typical power consumptions are provided in Table 1 for the following reference systems:

- Boards – GigaBee XC6SLX 45/100/150
- Base board – TE0603-02
- Power supply – 5 V from baseboard
- Connected Gigabit Ethernet cable

FPGA type	Unconfigured	Configured with Web-server reference design
LX45	0.15 A	0.6 A
LX100	0.17 A	0.5 A
LX150	0.2 A	0.5 A

Table 1: Power consumption

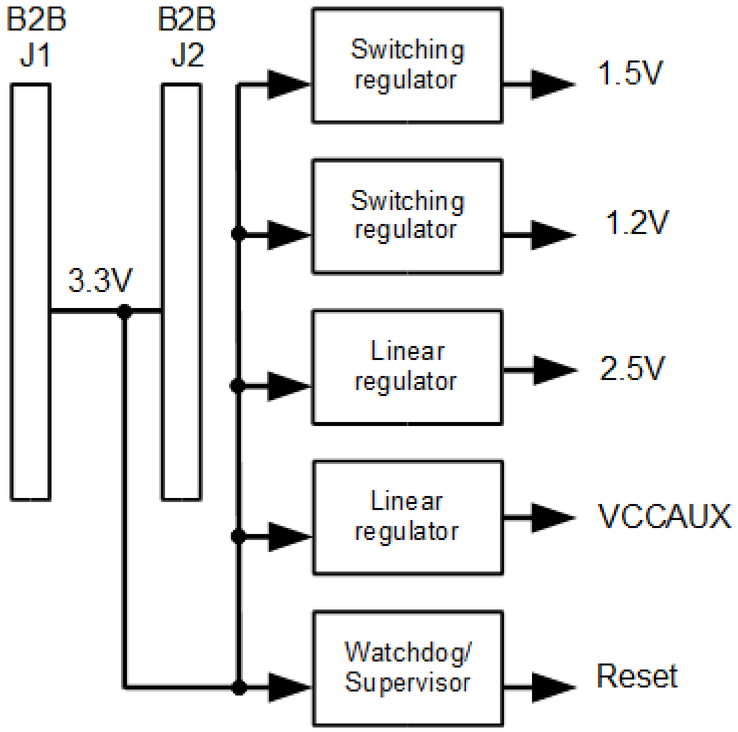

Figure 5: Power supply diagram

2.2.1 Power Supply Sources

GigaBee XC6SLX board must be powered at least in one of the following two ways:

- through B2B connector J1 (pins 1, 3, 5, 7, 9, 11, 13, 15),
- through B2B connector J2 (pins 2, 4, 6, 8, 10, 12).

We recommend to supply the module with all these 14 pins. When one or more of these pins are not power supplied, it or they can be used as power source for user applications.

Please make sure that your logic design does not draw more RMS current per pin than specified in section 2.4 Board-to-board Connectors.

2.2.2 FPGA banks VCCIO power supply

FPGA VCCIO power options shown in Table 2. Default values for configurable voltages shown in braces.

Bank	Supply voltage
B0	VCCIO 0 (3.3 V)
B1	VCCIO 1 (1.5 V)
B2	3.3 V
B3	1.5 V

Table 2: FPGA banks VCCIO power supply

Bank 0 power supply VCCIO 0 can be configured by user to 3.3 V, 2.5 V or

1.5 V, see Chapter 2.2.3.6 VCCIO0 Power Rail. Bank 1 VCCIO supply voltage is configured to 1.5 V to communicate with DDR3 SDRAM memory chip.[1]

2.2.3 On-board Power Rails

GigaBee XC6SLX has the following power rails on-board.

2.2.3.1 3.3V Power Rail

It is the main internal power rail and must be supplied from an external power source.

It supplies the other following power rails:

- 1.2V / 4 A on-board high-efficiency switching voltage regulator;
- 1.5V / 1.5 A on-board high-efficiency switching voltage regulator;
- 2.5V 0.8 A linear voltage regulator;
- VCCIO0 power rail (option) (if zero-resistor R80 is not populated and zero-resistor R79 is populated).

2.2.3.2 1.2V Power Rail

It is converted from the 3.3V rail by a switching voltage regulator and can provide up to 4.0 A to:

- FPGA V_{CCINT} power supply pins;
- Ethernet PHY;
- J1 connector.

2.2.3.3 1.5V Power Rail

It is converted from the 3.3V rail by a switching voltage regulator and can provide up to 1.5 A to:

- DDR3 SDRAM;
- Vref1 / Vref2 DDR3 SDRAM reference voltages;
- FPGA bank 3 V_{CCO};
- J1 connector.

2.2.3.4 2.5V Power Rail

It is converted from the 3.3V rail by a linear voltage regulator and can provide up to 0.8 A to:

- VCCAUX power rail;
- Ethernet physical layer;
- J1 connector;

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[1] By special request modules can be supplied without DDR3 SDRAM chips. Contact Trenz Electronic support for details

Table 3 summarizes power rails information.

power-rail name	nominal voltage(V)	maximum current (A)	power source	system supply	user supply
3.3V	3.3	2.4 (3.3 option)	J1, J2	module	J1 (≤1.2 A) J2 (≤1.2 A, ≤2.1 option)
2.5V	2.5	0.8	3.3V ▸ linear	Ethernet	J1 (≤0.3 A) J2 (option)
1.5V	1.5	1.5	3.3V ▸ switch.	DDR3 SDRAM VCCO (1+3)	J1 (≤0.3 A)
1.2V	1.2	4.0	3.3V ▸ switch.	VCCINT Ethernet	J1 (≤0.6 A)
VCCAUX	2.5	0.8	3.3V ▸ linear	FPGA	J2 (≤0.3 A)
VCCCIO0	1.2, 1.5, 1.8, 2.5, 3.3	0.9	J2	VCCO (0)	J2 (≤0.9 A)

Table 3: On-board power rails summary

2.3 Power Supervision

2.3.1 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the supply rail remains below the threshold voltage (2.93 volt). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset prior to a regular system start-up. The typical delay time t_d of 200 ms starts after the supply rail has risen above the threshold voltage.

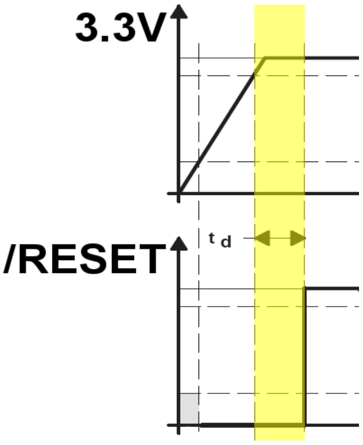

Figure 7: Reset on power-on

After this delay, the /RESET line is reset (high) and the FPGA configuration can start. When the supply rail voltage drops below the threshold voltage, the /RESET line becomes active (low) again and stays active (low) as long as the rail voltage remains below the threshold voltage (2.93 volt). Once the rail voltage raises again and remains over the threshold voltage for more than the typical delay time t_d of 200 ms, the /RESET line returns to the inactive state (high) to allow a new system start-up.

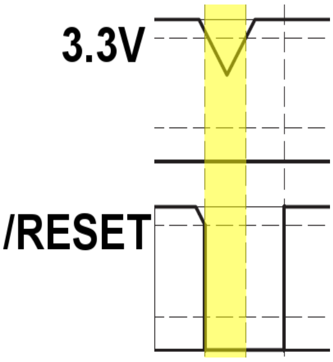

Figure 8: Reset on power drop

2.3.2 Power Fail

GigaBee XC6SLX integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply 3.3 V. When the voltage of the PFI (power-fail comparator input, input pin 16 of connector J2) line drops below 1.25 volt, the /PFO (power-fail comparator output, FPGA pin A2, label IO_L83P_3) line becomes active (low). The user application can sense this line to take action. To set a power fail threshold higher than 1.25 volt, the user can implement a simple resistive voltage divider on the carrier board.

2.4 Board-to-board Connectors

GigaBee XC6SLX mounts two Samtec Razor Beam LSHM connectors (J1 and J2) on the bottom side.

Each connector features the following characteristics:

- rows per connector: 2
- contacts per row: 50
- contacts per connector: 100
- connector gender: hermaphrodite
- pitch: 0.50 mm = 19.7 mil = .0197”
- mated height: min. 5.0 mm | typ. 8.0 mm | max. 12.0 mm
- mating force: min. 39 N | typ. 59 N | max. 62 N
- un-mating force: min. 49 N | typ. 73 N | max. 74 N

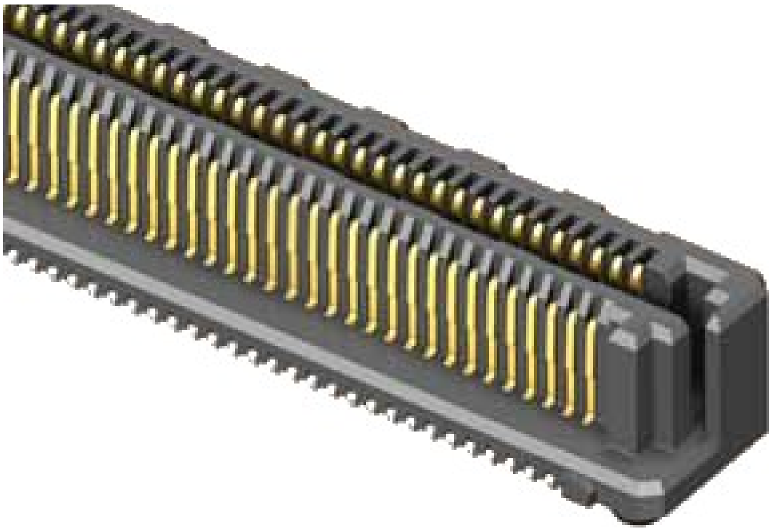

Figure 9: Samtec Razor Beam LSHM connector

The overall number of connector contacts on the GigaBee XC6SLX is 200.

Samtec Razor Beam LSHM is a high-speed interconnect system with very fine pitch (50 mil) and low profile design. Razor Beam connectors are well suited for high speed applications with performance up to 11.5 GHz (23 Gb/s) at -3 dB insertion loss. Razor Beam contacts are ideal for high speed and rugged applications featuring undercut retention notches that increase the withdrawal force and provide an audible click when the contacts engage. In addition, the self-mating (hermaphroditic) design can help reduce inventory costs. The LSHM Series features also optional shielding for EMI protection (default on GigaBee XC6SLX).

Samtec Razor Beam LSHM connectors are keyed. On the bottom side of the GigaBee XSL6, the connectors are assembled in such a way to prevent the module to be reverse mounted on carrier boards.

Samtec Razor Beam LSHM are available in different lead styles, see Table 4 for details.

lead style	A [mm]	B [mm]
–02.5	3.95	1.00
–03.0	4.45	1.50
–04.0	5.45	2.50
–06.0	7.45	4.50

Table 4: Samtec Razor Beam LSHM lead styles

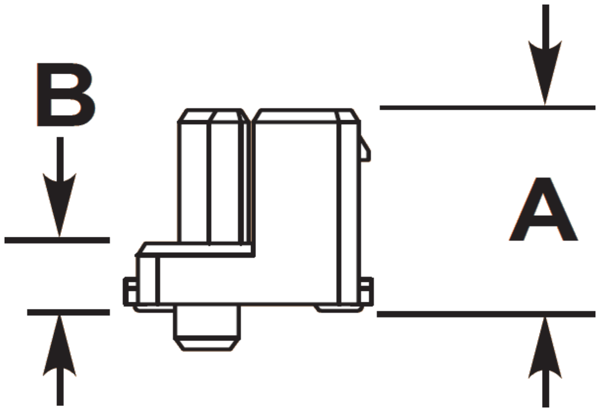

Figure 10: A and B features of Samtec Razor Beam LSHM series

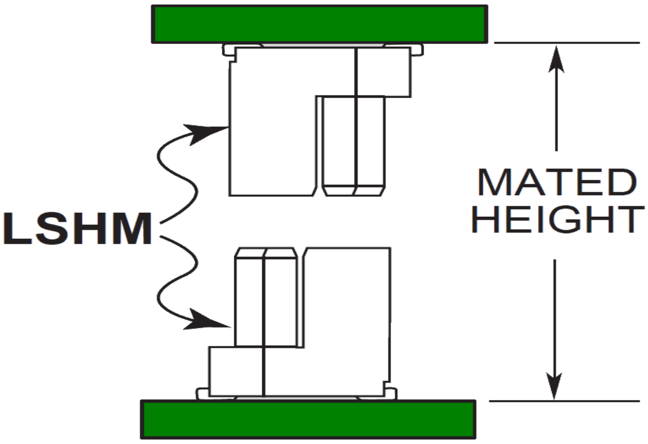

Figure 11: Definition of mated height for Samtec Razor Beam LSHM series.

The standard connector mounted on the GigaBee XC6SLX is Samtec Razor Beam LSHM-150-04.0-L-DV-A-S-K-TR (lead style: –04.0, tail option: vertical, shield option: with shield).

Trenz Electronic recommends the same part as mating connector, due to its self-mating capability.

The Samtec Razor Beam LSHM series offers a variety of mated heights form 5.0 mm to 12.0 mm. Two mated standard GigaBee XC6SLX connectors have a typical mated height of 8.0 mm. Processing conditions will affect the following heights.

standard connector lead style	mating connector lead style	mated height [mm]	min. height from carrier board [mm]	max. height on carrier board [mm]
−04.0	−02.5	6.5	≈ 3.5	≈ 11.5
−04.0	−03.0	7.0	≈ 4.0	≈ 12.0
−04.0	**−04.0**	**8.0**	**≈ 5.0**	**≈ 13.0**
−04.0	−06.0	10.0	≈ 7.0	≈ 15.0

Table 5: Samtec Razor Beam LSHM mated heights

In the standard assembly, the /WDO (watchdog output) line is left unconnected[3] and the only possibility to reset the module is by driving the /MR (master reset) line active (low) through pin 18 of connector J2.

In the alternate assembly, the /WDO (watchdog output) line is connected through zero-resistor R3 to /MR (master reset) line.

If alternate assembly is used, pin 18 of connector J2 must be left unconnected.

3 Configuration Options

The FPGA on GigaBee XC6SLX board can be configured by means of the following devices:

- Xilinx download cable (JTAG)
- SPI Flash memory

3.1 JTAG Configuration

The FPGA can be configured through the JTAG interface. JTAG signals are connected to B2B connector J2. When GigaBee XC6SLX board is used with the TE0603 carrier board, the JTAG interface can be accessed via connectors J5 and J6 on the carrier board.

3.2 Flash Configuration

Default configuration option for FPGA is “Master Serial/SPI”. The bit-stream for the FPGA is stored in a serial Flash chip (U11). See chapter 2.7 Flash Memory for additional information.

3.3 eFUSE Programming

eFUSE programming feature is not directly supported by GigaBee XC6SLX modules, but it is possible to use it. To program eFUSE, please follow the steps below:

- Connect VCCAUX to 3.3V power rail.

  On TE0603 it can be done by connecting J5 pin 2 or J6 “VREF” (VCCAUX) to J1 any pin from 1,2,3,4 (3.3V). See Figure 13.
- Program eFUSE using JTAG cable and iMPACT software.
- Remove power supply connections to VCCAUX

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[3] Resistor R3 is not populated.

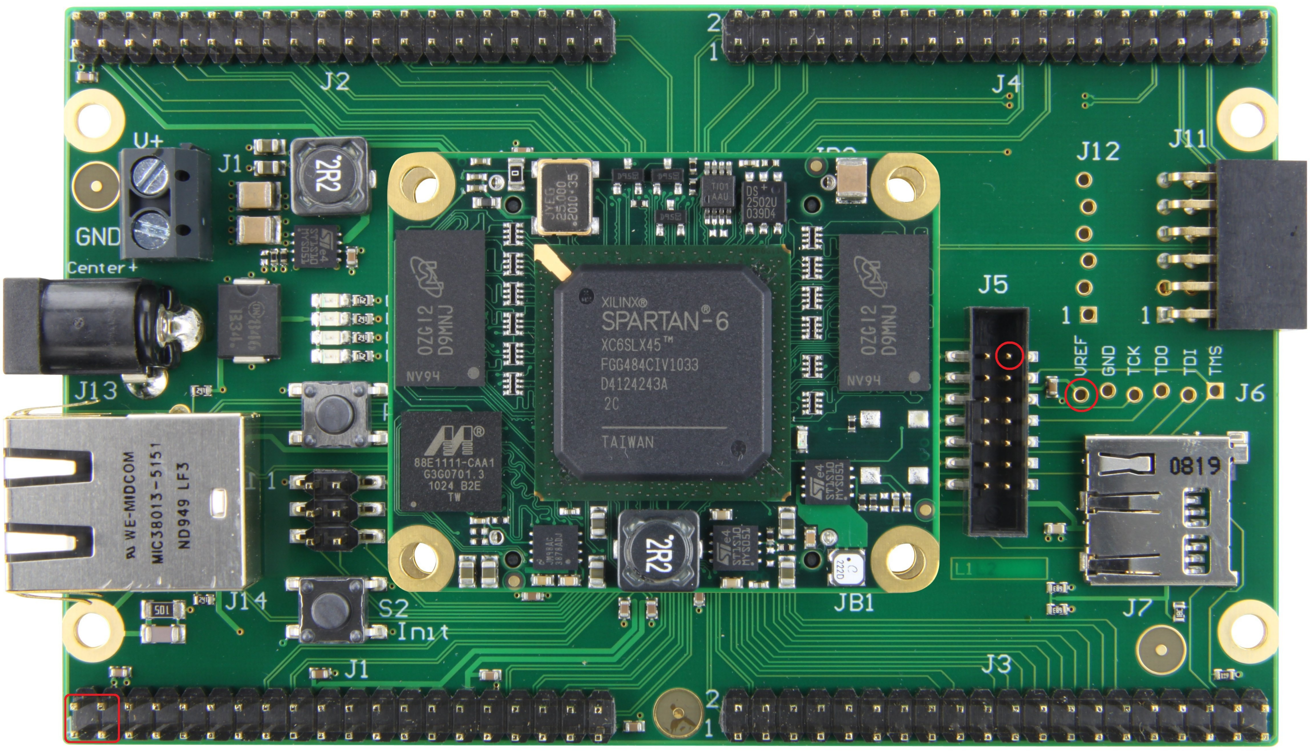

Figure 13: eFUSE Powering

4 B2B Connectors Pin Descriptions

This section describes how the various pins on B2B connectors J1 and J2 connects to TE0600 on-board components. There are five main signal types connected to B2B connectors:

- FPGA users signals;
- FPGA system signals;
- Power signals;
- Ethernet PHY signals;
- Other system signals.

FPGA Bank	Single-ended	Differential	Total	VCCIO
Bank 0	1	22	45	VCCIO 0 (3.3 V)
Bank 1	1	6	13	VCCIO 1 (1.5 V)
Bank 2	3	21	45	3.3 V
Bank 3	0	3	6	1.5 V
	5	52	109	

Table 9: B2B signals count

4.1 Pin Labelling

FPGA user signals connected to B2B connectors are characterized by the "B2B_Bx_Lyy_p" naming convention, where:

- B2B defines a "FPGA to B2B" signal type;
- Bx defines the FPGA bank (x = bank number);
- Lyy defines a differential pair or signal number (yy = pair number);
- p defines a differential signal polarity (P = positive, N = negative); single ended signals do not have this field.

Ethernet PHY signals use "PHY_name" naming conversions where "PHY" defines signal type "PHY to B2B" and "name" is PHY signal name.

Remaining signals use custom names.

4.2 Pin Numbering

Note that GigaBee XC6SLX have hermaphroditic B2B connectors. A feature of hermaphroditic connector numbering is that connected signal numbers don't match. Odd signals on module connect to even signals on baseboard. For example module signal 1 to baseboard signal 2, module signal 2 to baseboard signal 1, module signal 3 to baseboard signal 4 and so on.

4.3 Pin Types

Most pins of B2B connectors J1 and J2 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 8 different functional types of pins on the TE0600, as outlined in Table 10. In pin-out tables Table 11 and Table 12, the individual pins are colour-coded according to pin type as in Table 10.

type colour code	description
DIO[4]	Unrestricted, general-purpose differential user-I/O pin.
SIO	Unrestricted, general-purpose user-I/O pin.
CONFIG	Dedicated configuration signals.
PWRMGMT	Control and status signals for the power-saving Suspend mode.
JTAG	Dedicated JTAG signals.
GND	Dedicated ground pin. All must be connected.
TE	Trenz Electronic specific pin type. See the description of each pin in the user manual for additional information on the corresponding signals.
POW	Power signals.
SPI	SPI signals.
PHY	Ethernet PHY signals.

Table 10: TE0600 pin types

Note that some of Spartan-6 I/O types are partially compatible, so pins of compatible types can be used as inputs for signal of other type. For example pins from FPGA bank with 1.5V VCCO (IOSTANDARD = LVCMOS15) can be used as inputs for 1.2V, 1.8V, 2.5V and 3.3V signals.

See "Spartan-6 FPGA SelectIO Resources" page 38 for detailed information.

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[4] DIO pins can be used as SIO.

4.4 External Bank 2 differential clock connection

TE0600-02 module have optional connection to FPGA bank 2 differential clock input pins. To provide connection from B2B_B2_L41_P signal to Y13 FPGA pin, zero-resistor R69 should be soldered. To provide connection B2B_B2_L41_N signal to AB13 FPGA pin, zero-resistor R81 should be soldered. Note that in this case optional user oscillator U13 can't be used.

4.5 J1 Pin-out

J1 pin	Net	Type	FPGA pin	Net Length	J1 pin	Net	Type	FPGA pin	Net Length
1	3.3V	POW	-	-	2	GND	GND	-	-
3	3.3V	POW	-	-	4	PHY_MDI0_P	PHY	-	-
5	3.3V	POW	-	-	6	PHY_MDI0_N	PHY	-	-
7	3.3V	POW	-	-	8	GND	GND	-	-
9	3.3V	POW	-	-	10	PHY_MDI1_P	PHY	-	-
11	3.3V	POW	-	-	12	PHY_MDI1_N	PHY	-	-
13	3.3V	POW	-	-	14	PHY_AVDD	PHY	-	-
15	3.3V	POW	-	-	16	PHY_MDI2_P	PHY	-	-
17	PHY_L10	PHY	-	-	18	PHY_MDI2_N	PHY	-	-
19	PHY_L100	PHY	-	-	20	GND	GND	-	-
21	PHY_L1000	PHY	-	-	22	PHY_MDI3_P	PHY	-	-
23	PHY_DUP	PHY	-	-	24	PHY_MDI3_N	PHY	-	-
25	PHY_LED_TX	PHY	-	-	26	GND	GND	-	-
27	PHY_LED_RX	PHY	-	-	28	EN	TE	-	-
29	GND	GND	-	-	30	INIT	CONFIG	T6	-
31	B2B_B2_L57_N	DIO	AB4	8.66mm	32	B2B_B2_L32_N	SIO	AB11	8.12mm
33	B2B_B2_L57_P	DIO	AA4	9.84mm	34	GND	GND	-	-
35	B2B_B2_L49_N	DIO	AB6	8.66mm	36	B2B_B2_L60_P	DIO	T7	9.96mm
37	B2B_B2_L49_P	DIO	AA6	9.58mm	38	B2B_B2_L60_N	DIO	R7	11.16mm
39	2.5V	POW	-	-	40	B2B_B2_L59_N	DIO	R8	11.42mm
41	1.2V	POW	-	-	42	B2B_B2_L59_P	DIO	R9	11.36mm
43	1.2V	POW	-	-	44	GND	GND	-	-
45	B2B_B2_L48_N	DIO	AB7	9.98mm	46	B2B_B2_L44_N	DIO	Y10	11.34mm
47	B2B_B2_L48_P	DIO	Y7	10.98mm	48	B2B_B2_L44_P	DIO	W10	10.21mm
49	B2B_B2_L45_N	DIO	AB8	10.60mm	50	B2B_B2_L42_N	DIO	W11	7.52mm
51	B2B_B2_L45_P	DIO	AA8	11.053mm	52	B2B_B2_L42_P	DIO	V11	8.36mm
53	GND	GND	-	-	54	GND	GND	-	-
55	B2B_B2_L43_N	DIO	AB9	13.75mm	56	B2B_B2_L18_P	DIO	V13	7.94mm
57	B2B_B2_L43_P	DIO	Y9	12.97mm	58	B2B_B2_L18_N	DIO	W13	6.96mm
59	B2B_B2_L41_N	DIO	AB10, AB13	10.33mm	60	B2B_B2_L8_N	DIO	U16	9.92mm
61	B2B_B2_L41_P	DIO	AA10, Y13	11.01mm	62	B2B_B2_L8_P	DIO	U17	9.94mm
63	GND	GND	-	-	64	GND	GND	-	-
65	B2B_B2_L21_P	DIO	Y15	13.12mm	66	B2B_B2_L11_P	DIO	V17	8.31mm
67	B2B_B2_L21_N	DIO	AB15	12.37mm	68	B2B_B2_L11_N	DIO	W17	7.29mm
69	B2B_B2_L15_P	DIO	Y17	14.20mm	70	B2B_B2_L6_P	DIO	W18	7.40mm
71	B2B_B2_L15_N	DIO	AB17	13.77mm	72	B2B_B2_L6_N	DIO	Y18	6.94mm
73	GND	GND	-	-	74	GND	GND	-	-
75	B2B_B2_L31_N	SIO	AB12	12.30mm	76	B2B_B2_L5_P	DIO	Y19	6.18mm

J2 pin	Net	Type	FPGA pin	Net Length	J2 pin	Net	Type	FPGA pin	Net Length
59	GND	GND	-	-	60	GND	GND	-	-
61	B2B_B0_L62_P	DIO	D15	7.44mm	62	B2B_B0_L38_N	DIO	A13	8.38mm
63	B2B_B0_L62_N	DIO	C16	6.95mm	64	B2B_B0_L38_P	DIO	C13	9.87mm
65	B2B_B0_L66_P	DIO	E16	8.07mm	66	B2B_B0_L50_N	DIO	A14	7.66mm
67	B2B_B0_L66_N	DIO	D17	6.96mm	68	B2B_B0_L50_P	DIO	B14	8.87mm
69	GND	GND	-	-	70	GND	GND	-	-
71	B2B_B1_L10_P	DIO	F16	9.56mm	72	B2B_B0_L51_N	DIO	A15	10.22mm
73	B2B_B1_L10_N	DIO	F17	8.85mm	74	B2B_B0_L51_P	DIO	C15	10.67mm
75	B2B_B1_L9_P	DIO	G16	10.59mm	76	B2B_B0_L63_N	DIO	A16	7.95mm
77	B2B_B1_L9_N	DIO	G17	10.23mm	78	B2B_B0_L63_P	DIO	B16	9.12mm
79	GND	GND	-	-	80	GND	GND	-	-
81	B2B_B1_L21_N	DIO	J16	13.22mm	82	B2B_B0_L64_N	DIO	A17	9.55mm
83	B2B_B1_L21_P	DIO	K16	14.41mm	84	B2B_B0_L64_P	DIO	C17	10.25mm
85	B2B_B1_L61_P	DIO	L17	14.89mm	86	B2B_B0_L65_N	DIO	A18	8.51mm
87	B2B_B1_L61_N	DIO	K18	13.59mm	88	B2B_B0_L65_P	DIO	B18	9.29mm
89	GND	GND	-	-	90	GND	GND	-	-
91	VCCAUX	POW	-	-	92	B2B_B1_L20_P	DIO	A20	8.02mm
93	TMS	JTAG	C18	-	94	B2B_B1_L20_N	DIO	A21	7.82mm
95	TDI	JTAG	E18	-	96	B2B_B1_L19_P	DIO	B21	9.63mm
97	TDO	JTAG	A19	-	98	B2B_B1_L19_N	DIO	B22	9.06mm
99	TCK	JTAG	G15	-	100	B2B_B1_L59	SIO	P19	27.19mm

Table 12: J2 pin-out

4.7 Signal Integrity Considerations

Traces of differential signals pairs are routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length[5]. For applications where traces length has to be matched or timing differences have to be compensated, Table 11 and Table 12 list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 100 ohm. Single ended traces are routed with 60 ohm impedance.

An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.

5 Module revisions and assembly variants

Module revision coded by 4 FPGA BR[3:0] pins, which can be read by FPGA firmware. All these pins should be configures to have internal PULLUP.

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[5] Difference in signal lines length is negligible for used signal frequency.

Signal FPGA pin	BR3 R19	BR2 P18	BR1 N16	BR0 P17
Revision 01	1	1	1	1
Revision 02	1	1	1	0

Table 13: Board revisions pin coding

Main differences between 01 and 02 revisions:

- More powerful regulators for 1.2V and 1.5V rails
- VCCAUX separated from 2.5V power rail
- 128Mbit SPI Flash
- Additional secure 1Kbit EEPROM
- Optional B2B connection to bank 2 differential clock input

Module assembly variants coded by 4 zero ohm resistors, connected to FPGA AV[3:0] pins. All these pins should be configures to have internal PULLUP.

Signal FPGA pin	AV3 M18	AV2 M17	AV1 V20	AV0 U19	Speed grade	SDRAM	Temp grade
TE0600-02[V|B]	0	0	0	0	2	2x128MBit	C
TE0600-02[V|B]I	0	0	0	1	2	2x128MBit	I
TE0600-02[V|B]F	0	0	1	0	3	2x128MBit	C
TE0600-02[V|B]IF	0	0	1	1	3	2x128MBit	I
TE0600-02[V|B]MF	0	1	0	0	3	2x512MBit	C

Table 14: Assembly variants pin coding

http://www.xilinx.com/support/documentation/user_guides/ug381.pdf

6.4 Design and Development Tools

- Xilinx ISE Design Suite
  http://www.xilinx.com/ISE/
  http://www.xilinx.com/tools/designtools.htm
- Xilinx ISE Design Suite (version archive)
  http://www.xilinx.com/download/
  http://www.xilinx.com/support/download/
- Xilinx ISE WebPACK
  http://www.xilinx.com/tools/webpack.htm
  http://www.xilinx.com/webpack/

6.5 Design Resources

- Trenz Electronic GigaBee Design Resources
  http://www.trenz-electronic.de/download/d0/Trenz_Electronic/d1/TE0600-GigaBee_series.html
- Trenz Electronic GigaBee Reference Designs
  https://github.com/Trenz-Electronic/
  https://github.com/Trenz-Electronic/TE-EDK-IP/
  https://github.com/Trenz-Electronic/TE060X-GigaBee-Reference-Designs/

6.6 Tutorials

- Xilinx UG695: ISE In-Depth Tutorial
  Chapter 8: Configuration Using iMPACT
  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/ise_tutorial_ug695.pdf

7 Glossary of Abbreviations and Acronyms

STOP	A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.
⚠	A CAUTION notice denotes a risk. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in a fault. (undesired condition that can lead to an error) Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.
API	application programming interface
B2B	board-to-board
DSP	digital signal processing; digital signal processor
EDK	Embedded Development Kit
IOB	input / output blocks; I/O blocks
IP	intellectual property
ISP	In-System Programmability
OTP	one-time programmable
PB	push button
SDK	Software Development Kit
TE	Trenz Electronic
XPS	Xilinx Platform Studio

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Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol

Document Change History

ver.	date	author	description
0.01	2011-10-01	AIK	Release.
0.02	2011-10-05	AIK	Added B2B pin-out section.
0.03	2011-10-06	AIK	Reformatted pin-out tables. Added eFUSE programming section.
0.04	2011-10-06	AIK	Added board photos. Additions to eFUSE section.
0.05	2011-10-06	AIK	Removed net length information for nets which can't be measured right.
0.06	2011-10-06	AIK	Added power consumption section.
0.07	2011-10-08	AIK	Little fixes after FDR audit.
0.08	2011-10-12	AIK	Fix in eFUSE section.
0.09	2011-11-11	AIK	Added pin numbering description for B2B connectors
0.10	2012-01-20	AIK	Added pin compatibility note and manual reference.
0.11	2012-04-12	AIK	Added FPGA banks VCCIO voltages table.
1.00	2012-04-17	FDR	Updated documentation link. Replaced obsolete ElDesI and RedMine links with current GitHub links. Updated dating convention.
1.01	2012-05-18	AIK	Corrected cross-reference in section 3.2. Corrected LED description.
1.02	2012-06-18	FDR	Removed junction temperature limits under connector current ratings.
1.03	2012-07-18	AIK	Added table with B2B signals summary per FPGA bank
2.01	2012-10-30	AIK	Fork to 01 and 02 board revisions
2.01	2012-11-06	AIK	Fixed bank 1 power options
2.02	2012-11-21	AIK	Updated module diagram
2.03	2012-11-30	AIK	Added Ethernet disable note
2.04	2012-12-19	AIK	Fixed SPI Flash size on block diagram
2.05	2013-01-21	AIK	Added PHY reset note
2.06	2013-03-13	AIK	Connectors current chapter moved to separate document
2.07	2013-03-13	AIK	Changed Bank 1 power supply description and VCCIO0 sources description