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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Spartan-6 LX-150
Co-Processor	-
Speed	125MHz
Flash Size	16MB
RAM Size	1GB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0600-02imvf

Table of Contents

1 Technical Specifications

1.1 Components

- Xilinx Spartan-6 LX FPGA:
  - XC6SLX**45**-2FGG484**C** = 43 K logic cells, commercial grade
    XC6SLX**45**-2FGG484**I** = 43 K logic cells, industrial grade
  - XC6SLX**100**-2FGG484**C** = 101 K logic cells, commercial grade
    XC6SLX**100**-2FGG484**I** = 101 K logic cells, industrial grade
  - XC6SLX**150**-2FGG484**C** = 147 K logic cells, commercial grade
    XC6SLX**150**-2FGG484**I** = 147 K logic cells, industrial grade
- 10/100/1000 Gigabit Ethernet transceiver (physical layer)
  Marvell Semiconductor 88E1111
- 2 × independent 16-bit-wide (data-bus) 1 Gigabit (128 megabyte) or 4 Gigabit (512 megabyte) DDR3 SDRAM
- 128 megabit (16 megabyte) serial Flash memory with dual/quad SPI interface
- 48-bit node address chip
  Maxim Integrated Products DS2502-E48
- 1Kb Protected 1-Wire EEPROM with SHA-1 Engine

  Maxim Embedded Security Products DS2432
- 2 x fine-pitch (0.5 mm) 100-pin high-speed (up to 10.0 GHz / 20 Gbps) hermaphroditic strips
  LSHM-150-04.0-L-DV-A-S-K-TR
- Up to 52 differential FPGA input/output pins available on B2B strips
- Up to 109 single-ended (+ 1 dual-purpose) FPGA input/output pins available on B2B strips
- Ethernet (PHY), JTAG and SPI pins available on B2B strips
- 4.0 A high-efficiency DC-DC switching regulator for power rail 1.2V
- 1.5 A high-efficiency DC-DC switching regulator for power rail 1.5V
- 2 x 800 mA DC-DC linear regulator for power rails 2.5V and VCCAUX
- Processor supervisory circuits with power-fail and watchdog
  Texas Instruments TPS3705-33
- 125 MHz clock signal (system + user)
- Footprint for custom single-ended oscillator (option)
- 1 x LED (user)
- Power supply voltage: 3.3 V
- Power supply source: board-to-board interconnect (e.g. carrier board)
- Dimensions: 50 mm × 40 mm (20 cm^2)
- Minimum module height: 8 mm (without connectors)

- Maximum height on carrier board surface: ≈ 13 mm (standard connectors)
- Minimum height on carrier board surface: ≈ 5 mm (standard connectors)
- Weight: 17.2 ± 0.1 g
- Temperature grades:
- commercial (C-type FPGA device)
- industrial (I-type FPGA device)

1.2 Dimensions

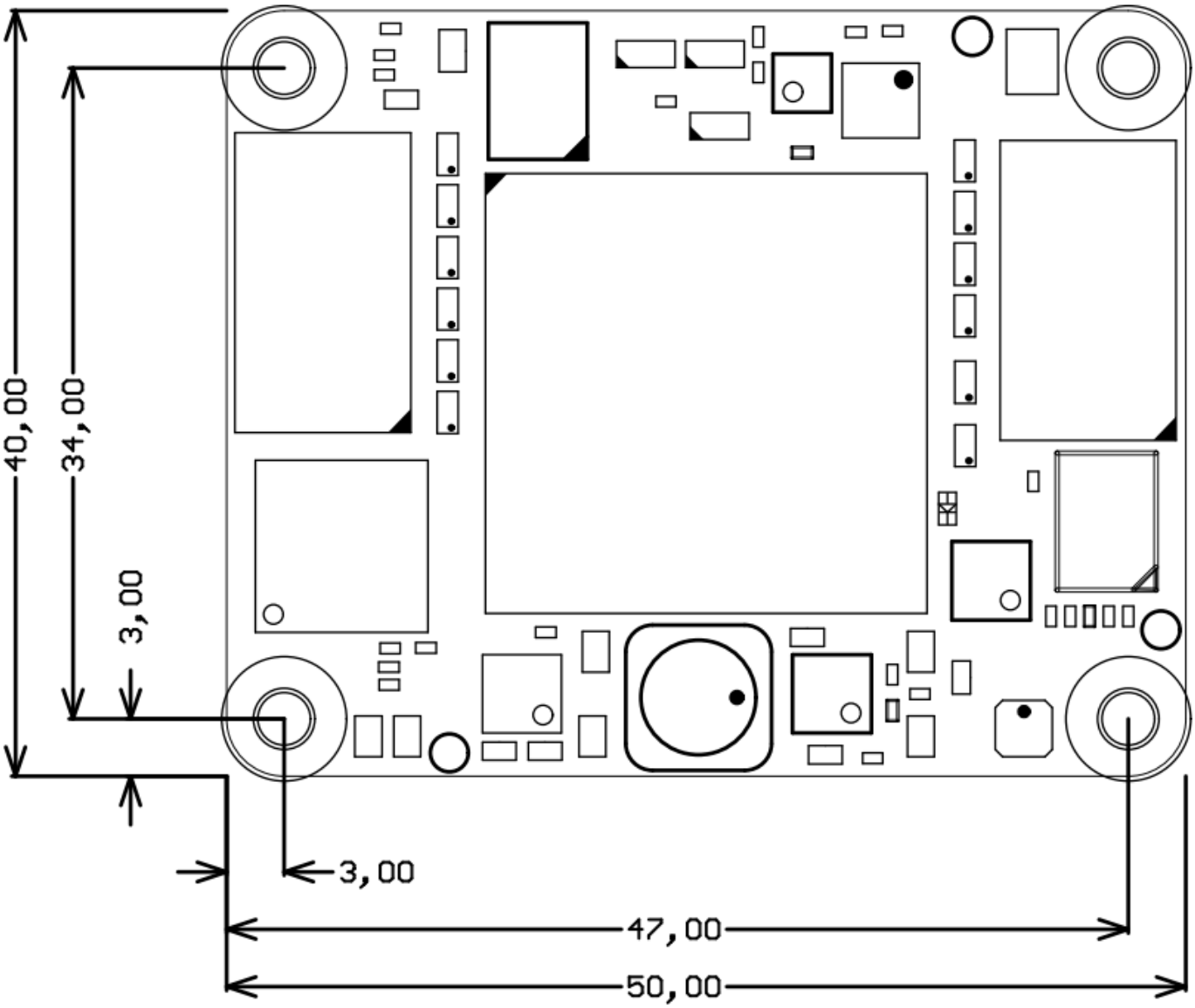

Figure 3: GigaBee board dimensions (top view)

GigaBee XC6SLX can reach a minimum vertical height of about 8 mm, if B2B

connectors are not assembled. The maximum component height on the module board on the top side is about 3.5 mm. The maximum component height on the module board on the bottom side is about 3.0 mm.

The typical minimum and maximum height from the carrier board surface, of a GigaBee XC6SLX when it mounted on a carrier board, is respectively about 5.0 mm and about 13 mm.

GigaBee XC6SLX has 4 mounting holes, one in each corner. The module can be fixed by screwing M3 screws (ISO 262) onto a carrier board through those mounting holes.

GigaBee XC6SLX weighs between 17.1 and 17.3 g with standard connectors.

1.3 Power Consumption

Power consumption of GigaBee XC6SLX modules highly depend on the FPGA design implemented. Some typical power consumptions are provided in Table 1 for the following reference systems:

- Boards – GigaBee XC6SLX 45/100/150
- Base board – TE0603-02
- Power supply – 5 V from baseboard
- Connected Gigabit Ethernet cable

FPGA type	Unconfigured	Configured with Web-server reference design
LX45	0.15 A	0.6 A
LX100	0.17 A	0.5 A
LX150	0.2 A	0.5 A

Table 1: Power consumption

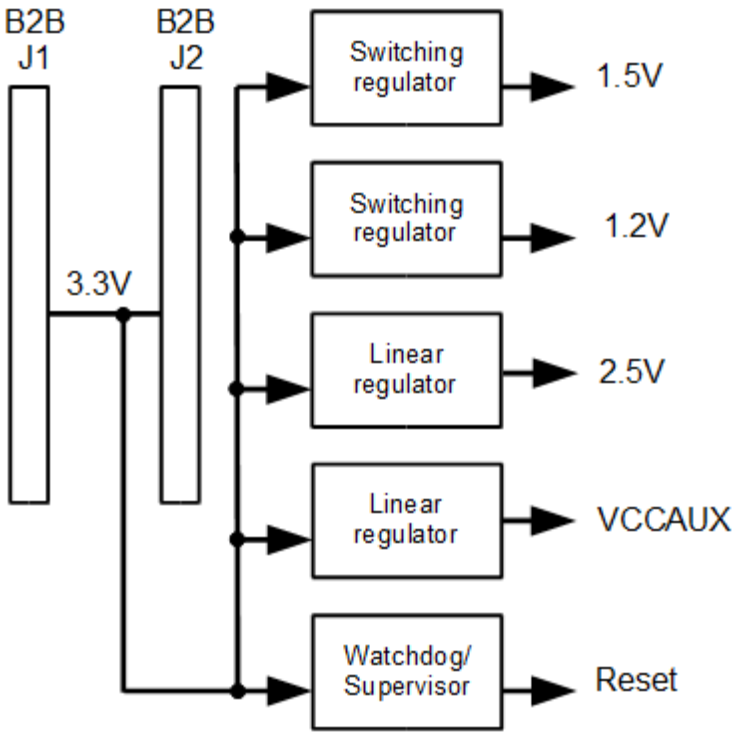

Figure 5: Power supply diagram

2.2.1 Power Supply Sources

GigaBee XC6SLX board must be powered at least in one of the following two ways:

- through B2B connector J1 (pins 1, 3, 5, 7, 9, 11, 13, 15),
- through B2B connector J2 (pins 2, 4, 6, 8, 10, 12).

We recommend to supply the module with all these 14 pins. When one or more of these pins are not power supplied, it or they can be used as power source for user applications.

Please make sure that your logic design does not draw more RMS current per pin than specified in section 2.4 Board-to-board Connectors.

2.2.2 FPGA banks VCCIO power supply

FPGA VCCIO power options shown in Table 2. Default values for configurable voltages shown in braces.

Bank	Supply voltage
B0	VCCIO 0 (3.3 V)
B1	VCCIO 1 (1.5 V)
B2	3.3 V
B3	1.5 V

Table 2: FPGA banks VCCIO power supply

Bank 0 power supply VCCIO 0 can be configured by user to 3.3 V, 2.5 V or

After this delay, the /RESET line is reset (high) and the FPGA configuration can start. When the supply rail voltage drops below the threshold voltage, the /RESET line becomes active (low) again and stays active (low) as long as the rail voltage remains below the threshold voltage (2.93 volt). Once the rail voltage raises again and remains over the threshold voltage for more than the typical delay time t_d of 200 ms, the /RESET line returns to the inactive state (high) to allow a new system start-up.

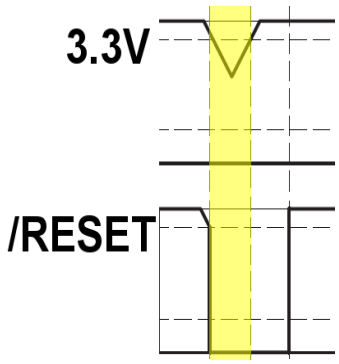

Figure 8: Reset on power drop

2.3.2 Power Fail

GigaBee XC6SLX integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply 3.3 V. When the voltage of the PFI (power-fail comparator input, input pin 16 of connector J2) line drops below 1.25 volt, the /PFO (power-fail comparator output, FPGA pin A2, label IO_L83P_3) line becomes active (low). The user application can sense this line to take action. To set a power fail threshold higher than 1.25 volt, the user can implement a simple resistive voltage divider on the carrier board.

2.4 Board-to-board Connectors

GigaBee XC6SLX mounts two Samtec Razor Beam LSHM connectors (J1 and J2) on the bottom side.

Each connector features the following characteristics:

- rows per connector: 2
- contacts per row: 50
- contacts per connector: 100
- connector gender: hermaphrodite
- pitch: 0.50 mm = 19.7 mil = .0197”
- mated height: min. 5.0 mm | typ. 8.0 mm | max. 12.0 mm
- mating force: min. 39 N | typ. 59 N | max. 62 N
- un-mating force: min. 49 N | typ. 73 N | max. 74 N

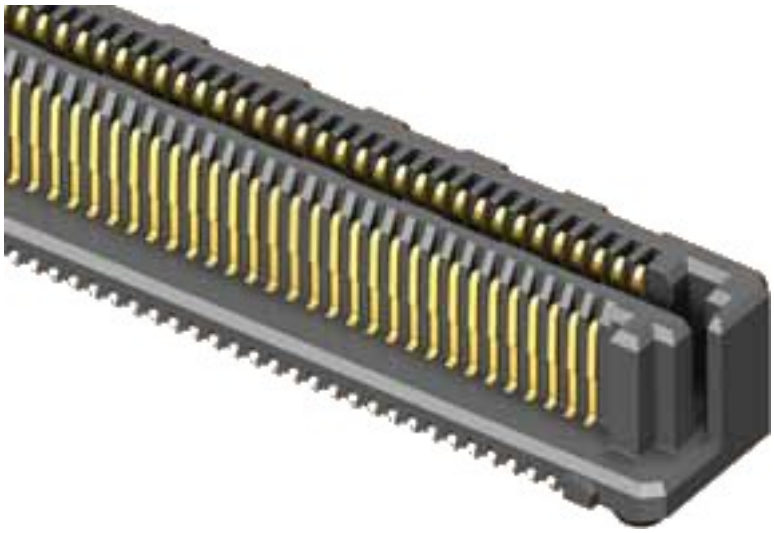

Figure 9: Samtec Razor Beam LSHM connector

The overall number of connector contacts on the GigaBee XC6SLX is 200.

Samtec Razor Beam LSHM is a high-speed interconnect system with very fine pitch (50 mil) and low profile design. Razor Beam connectors are well suited for high speed applications with performance up to 11.5 GHz (23 Gb/s) at -3 dB insertion loss. Razor Beam contacts are ideal for high speed and rugged applications featuring undercut retention notches that increase the withdrawal force and provide an audible click when the contacts engage. In addition, the self-mating (hermaphroditic) design can help reduce inventory costs. The LSHM Series features also optional shielding for EMI protection (default on GigaBee XC6SLX).

Samtec Razor Beam LSHM connectors are keyed. On the bottom side of the GigaBee XSL6, the connectors are assembled in such a way to prevent the module to be reverse mounted on carrier boards.

Samtec Razor Beam LSHM are available in different lead styles, see Table 4 for details.

lead style	A [mm]	B [mm]
-02.5	3.95	1.00
-03.0	4.45	1.50
-04.0	5.45	2.50
-06.0	7.45	4.50

Table 4: Samtec Razor Beam LSHM lead styles

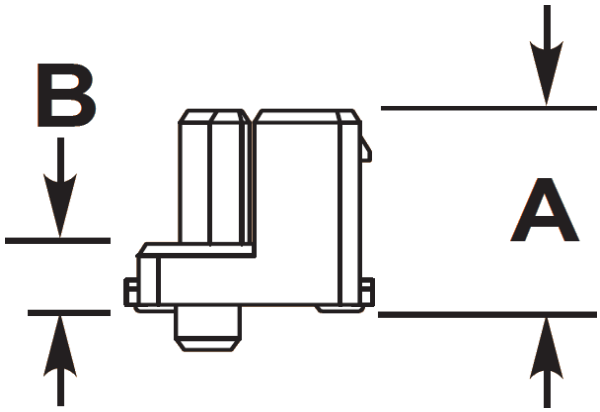

Figure 10: A and B features of Samtec Razor Beam LSHM series

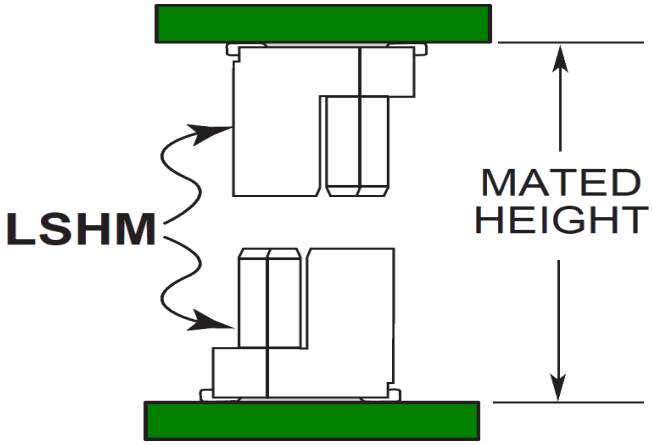

Figure 11: Definition of mated height for Samtec Razor Beam LSHM series.

The standard connector mounted on the GigaBee XC6SLX is Samtec Razor Beam LSHM-150-04.0-L-DV-A-S-K-TR (lead style: –04.0, tail option: vertical, shield option: with shield).

Trenz Electronic recommends the same part as mating connector, due to its self-mating capability.

The Samtec Razor Beam LSHM series offers a variety of mated heights form 5.0 mm to 12.0 mm. Two mated standard GigaBee XC6SLX connectors have a typical mated height of 8.0 mm. Processing conditions will affect the following heights.

standard connector lead style	mating connector lead style	mated height [mm]	min. height from carrier board [mm]	max. height on carrier board [mm]
–04.0	–02.5	6.5	≈ 3.5	≈ 11.5
–04.0	–03.0	7.0	≈ 4.0	≈ 12.0
–04.0	**–04.0**	**8.0**	**≈ 5.0**	**≈ 13.0**
–04.0	–06.0	10.0	≈ 7.0	≈ 15.0

Table 5: Samtec Razor Beam LSHM mated heights

Ordering codes for connectors J1 and J2 used in GigaBee XC6SLX board, and their mating connectors are given in Table 6.

lead style	gender	Samtec	Trenz Electronic
-02.5	hermaphroditic	LSHM-150-02.5-L-DV-A-S-K-TR	23836
-03.0	hermaphroditic	LSHM-150-03.0-L-DV-A-S-K-TR	23837
-04.0	hermaphroditic	LSHM-150-04.0-L-DV-A-S-K-TR	23838
-06.0	hermaphroditic	LSHM-150-06.0-L-DV-A-S-K-TR	23839

Table 6: Ordered codes of recommended B2B connectors

2.4.1 Connector Speed Rating

Samtec provides speed rating data for the Samtec Razor Beam LSHM connector system. The data presented in Table 7 are applicable only to the maximum and minimum mated heights. The speed rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signalling environment.

mated height	5 mm	12 mm
single-ended signalling	11.5 GHz 23.0 Gb/s	7.5 GHz 15.0 Gb/s
differential pair signalling	7.0 GHz 14.0 Gb/s	6.5 GHz 13.0 Gb/s

Table 7: Connectors speed rating

More details can be found in the Samtec Razor Beam LSHM series overview (“High Speed Characterization Reports”).

2.5 EPROM

GigaBee XC6SLX board contains a Maxim DS2502-E48 node address chip with factory-programmed valid MAC-48 address and 768 bits of OTP-EPROM memory for user data.

Address chip provide convenient data access through 1-Wire interface up to 16.3 kbps (FPGA pin T11).

More information can be found in the Maxim DS2502-E48 product overwiew.

Additional 1Kb protected 1-Wire EEPROM with SHA-1 engine DS2432 accessible via the same line.

More information can be found at the Maxim DS2432 product page.

2.6 DDR3 SDRAM Memory

The board contains two 1 Gb (128 MB) or 4 Gb (512 MB) DDR3 SDRAM chips. Data width of each chip is 16 bit. DDR3 memory connected to FPGA bank 1 and FPGA bank 3. Spartan-6 Memory controller Blocks operations can be merged to implement effective 32-bit memory interface. Refer Xilinx XAPP496 for detailed information.

For correct operation of the Marvell PHY it is required that PHY Reset pin sees valid low level each time power is applied and also during any brownout situations where system Power is removed for short time, but some pins are not at valid logic levels.

Solutions:

1) if GbE PHY is not used PHY reset pin can be tied off to GND
2) if PLL is used from PHY clock, then PLL "locked" output can be used to reset PHY - as long PLL is not locked, it will keep PHY in reset
3) Reset pulse generation circuit clocked from FPGA internal configuration clock, this circuit can force PHY reset pin to low when external clock from PHY is not available
4) any custom Reset circuit that is guaranteed to drive PHY reset to low level at least once after FPGA configuration when PHY clock is not running.
5) any user logic that is guaranteed to drive PHY reset low after FPGA configuration (without using PHY clock).

Explanation: Marvell PHY samples the MODE pins ONLY when it sees low level on PHY reset input, it does not sample those pins during short power off situations (if the reset pin holds high level because of pin capacitance and high impedance of the pins)! So it is possible that the PHY mode is reset, but the mode pins are not sampled again - this yields in mode setting where 125MHz reference clock from PHY is not available.

2.9 Oscillators

The module has one 25 MHz oscillator for Ethernet PHY (U9). Ethernet PHY provides clock multiplication and resulting 125 MHz clock acts as a system and user clock for the FPGA (FPGA input pin AA12).

Note: For correct generation start, PHY should receive reset pulse. Recommended way to do it it's to connect PHY reset signal (ETHERNET_PHY_RST_N) to LOCKED output of corresponding DCM (DCM which use 125 MHz from PHY).

The module also provides the footprint for custom 3.3 V single-ended oscillator (U12) which can be installed as an option (FPGA input pin Y13).

2.10 User LED

The module contains one user active-low LED connected to FPGA output pin T20. To access more LEDs, use a carrier board and drive FPGA signals connected to B2B connectors. As LED connected to FPGA bank with configurable VCCIO to light LED FPGA pin should in '0' (low) state. To disable LED FPGA pin should be in 'Z' (High impedance).

2.11 Watchdog

GigaBee XS6LX has a watchdog timer that is periodically triggered by a positive or negative transition of the WDI (watchdog input) line (FPGA pin V9). When the supervising system fails to re-trigger the watchdog circuit within the time-out interval (min 1.1 s, typ 1.6 s, max 2.3 s), the /WDO (watchdog output) line becomes active (low). This event also re-initializes the watchdog timer.

If zero-resistors R2 is not assembled, the watchdog is disabled (alternate assembly).

If zero-resistors R2 is assembled, the watchdog can be enabled (standard assembly). In this case there is still two options:

To **enable** the watchdog, after module power-up, drive the WDI signal to generate at least one transition (no matter positive or negative).

To keep watchdog **disabled**, set WDI FPGA signal output to high-impedance. One way to reach this goal is to leave FPGA pin V9 (label IO_L50N_2) undeclared in user constrains file (UCF) and set “unused IOB pins” to “float” in the Xilinx Project Navigator options, see Fig. 12.

(Project properties > Configuration options > Unused IOB Pins > Float).

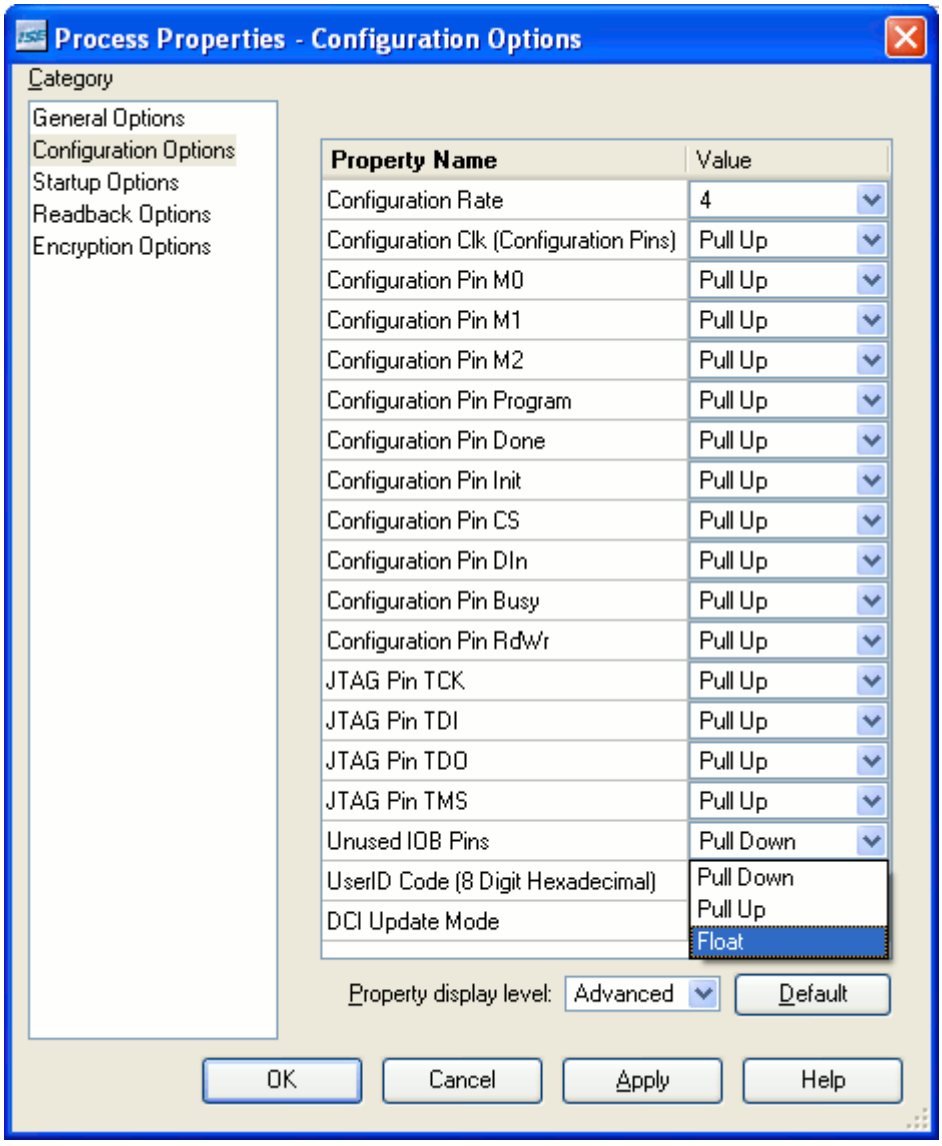

Figure 12: Unused IOB Pins option selection

In the standard assembly, the /WDO (watchdog output) line is left unconnected[3] and the only possibility to reset the module is by driving the /MR (master reset) line active (low) through pin 18 of connector J2.

In the alternate assembly, the /WDO (watchdog output) line is connected through zero-resistor R3 to /MR (master reset) line.

If alternate assembly is used, pin 18 of connector J2 must be left unconnected.

3 Configuration Options

The FPGA on GigaBee XC6SLX board can be configured by means of the following devices:

- Xilinx download cable (JTAG)
- SPI Flash memory

3.1 JTAG Configuration

The FPGA can be configured through the JTAG interface. JTAG signals are connected to B2B connector J2. When GigaBee XC6SLX board is used with the TE0603 carrier board, the JTAG interface can be accessed via connectors J5 and J6 on the carrier board.

3.2 Flash Configuration

Default configuration option for FPGA is “Master Serial/SPI”. The bit-stream for the FPGA is stored in a serial Flash chip (U11). See chapter 2.7 Flash Memory for additional information.

3.3 eFUSE Programming

eFUSE programming feature is not directly supported by GigaBee XC6SLX modules, but it is possible to use it. To program eFUSE, please follow the steps below:

- Connect VCCAUX to 3.3V power rail.

  On TE0603 it can be done by connecting J5 pin 2 or J6 “VREF” (VCCAUX) to J1 any pin from 1,2,3,4 (3.3V). See Figure 13.

- Program eFUSE using JTAG cable and iMPACT software.
- Remove power supply connections to VCCAUX

3 Resistor R3 is not populated.

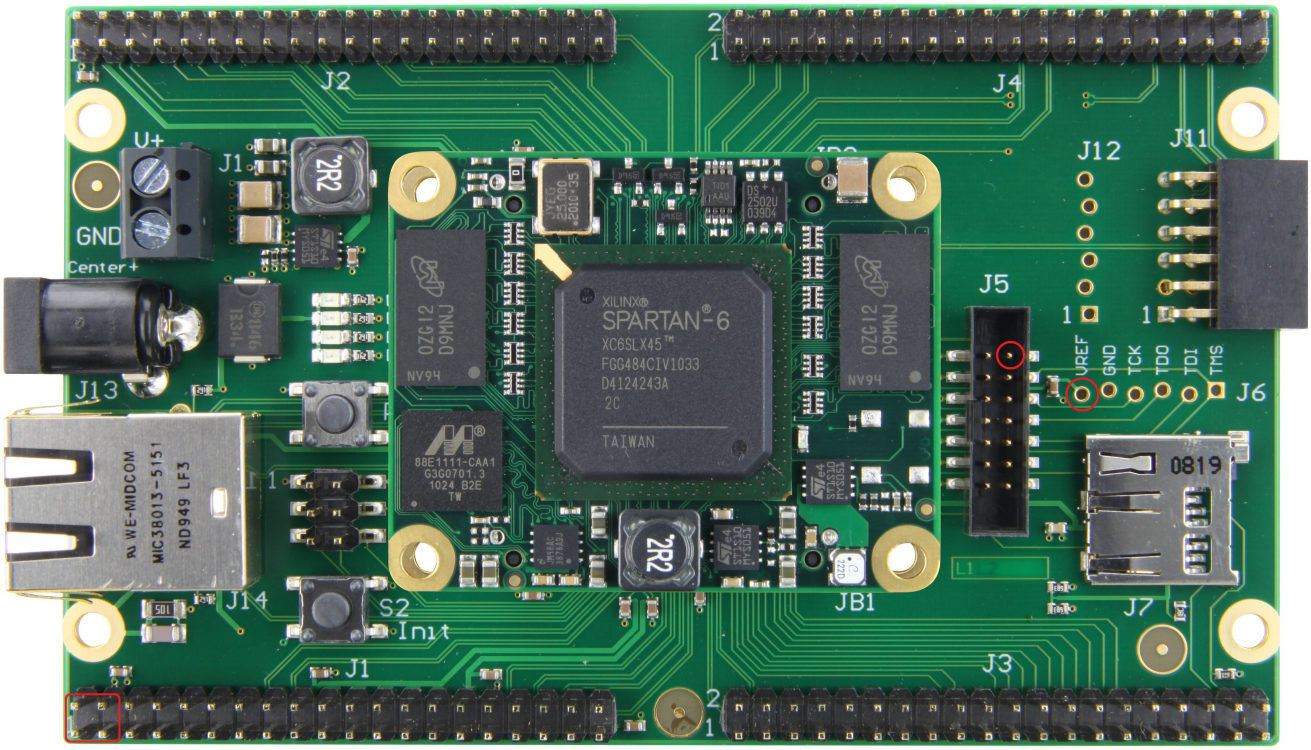

Figure 13: eFUSE Powering

4 B2B Connectors Pin Descriptions

This section describes how the various pins on B2B connectors J1 and J2 connects to TE0600 on-board components. There are five main signal types connected to B2B connectors:

- FPGA users signals;
- FPGA system signals;
- Power signals;
- Ethernet PHY signals;
- Other system signals.

FPGA Bank	Single-ended	Differential	Total	VCCIO
Bank 0	1	22	45	VCCIO 0 (3.3 V)
Bank 1	1	6	13	VCCIO 1 (1.5 V)
Bank 2	3	21	45	3.3 V
Bank 3	0	3	6	1.5 V
	5	52	109	

Table 9: B2B signals count

4.1 Pin Labelling

FPGA user signals connected to B2B connectors are characterized by the "B2B_Bx_Lyy_p" naming convention, where:

- B2B defines a "FPGA to B2B" signal type;
- Bx defines the FPGA bank (x = bank number);
- Lyy defines a differential pair or signal number (yy = pair number);
- p defines a differential signal polarity (P = positive, N = negative); single ended signals do not have this field.

Ethernet PHY signals use "PHY_name" naming conversions where "PHY" defines signal type "PHY to B2B" and "name" is PHY signal name.

Remaining signals use custom names.

4.2 Pin Numbering

Note that GigaBee XC6SLX have hermaphroditic B2B connectors. A feature of hermaphroditic connector numbering is that connected signal numbers don't match. Odd signals on module connect to even signals on baseboard. For example module signal 1 to baseboard signal 2, module signal 2 to baseboard signal 1, module signal 3 to baseboard signal 4 and so on.

4.3 Pin Types

Most pins of B2B connectors J1 and J2 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 8 different functional types of pins on the TE0600, as outlined in Table 10. In pin-out tables Table 11 and Table 12, the individual pins are colour-coded according to pin type as in Table 10.

type colour code	description
DIO[4]	Unrestricted, general-purpose differential user-I/O pin.
SIO	Unrestricted, general-purpose user-I/O pin.
CONFIG	Dedicated configuration signals.
PWRMGMT	Control and status signals for the power-saving Suspend mode.
JTAG	Dedicated JTAG signals.
GND	Dedicated ground pin. All must be connected.
TE	Trenz Electronic specific pin type. See the description of each pin in the user manual for additional information on the corresponding signals.
POW	Power signals.
SPI	SPI signals.
PHY	Ethernet PHY signals.

Table 10: TE0600 pin types

Note that some of Spartan-6 I/O types are partially compatible, so pins of compatible types can be used as inputs for signal of other type. For example pins from FPGA bank with 1.5V VCCO (IOSTANDARD = LVCMOS15) can be used as inputs for 1.2V, 1.8V, 2.5V and 3.3V signals.

See “Spartan-6 FPGA SelectIO Resources” page 38 for detailed information.

4 DIO pins can be used as SIO.

J2 pin	Net	Type	FPGA pin	Net Length	J2 pin	Net	Type	FPGA pin	Net Length
59	GND	GND	-	-	60	GND	GND	-	-
61	B2B_B0_L62_P	DIO	D15	7.44mm	62	B2B_B0_L38_N	DIO	A13	8.38mm
63	B2B_B0_L62_N	DIO	C16	6.95mm	64	B2B_B0_L38_P	DIO	C13	9.87mm
65	B2B_B0_L66_P	DIO	E16	8.07mm	66	B2B_B0_L50_N	DIO	A14	7.66mm
67	B2B_B0_L66_N	DIO	D17	6.96mm	68	B2B_B0_L50_P	DIO	B14	8.87mm
69	GND	GND	-	-	70	GND	GND	-	-
71	B2B_B1_L10_P	DIO	F16	9.56mm	72	B2B_B0_L51_N	DIO	A15	10.22mm
73	B2B_B1_L10_N	DIO	F17	8.85mm	74	B2B_B0_L51_P	DIO	C15	10.67mm
75	B2B_B1_L9_P	DIO	G16	10.59mm	76	B2B_B0_L63_N	DIO	A16	7.95mm
77	B2B_B1_L9_N	DIO	G17	10.23mm	78	B2B_B0_L63_P	DIO	B16	9.12mm
79	GND	GND	-	-	80	GND	GND	-	-
81	B2B_B1_L21_N	DIO	J16	13.22mm	82	B2B_B0_L64_N	DIO	A17	9.55mm
83	B2B_B1_L21_P	DIO	K16	14.41mm	84	B2B_B0_L64_P	DIO	C17	10.25mm
85	B2B_B1_L61_P	DIO	L17	14.89mm	86	B2B_B0_L65_N	DIO	A18	8.51mm
87	B2B_B1_L61_N	DIO	K18	13.59mm	88	B2B_B0_L65_P	DIO	B18	9.29mm
89	GND	GND	-	-	90	GND	GND	-	-
91	VCCAUX	POW	-	-	92	B2B_B1_L20_P	DIO	A20	8.02mm
93	TMS	JTAG	C18	-	94	B2B_B1_L20_N	DIO	A21	7.82mm
95	TDI	JTAG	E18	-	96	B2B_B1_L19_P	DIO	B21	9.63mm
97	TDO	JTAG	A19	-	98	B2B_B1_L19_N	DIO	B22	9.06mm
99	TCK	JTAG	G15	-	100	B2B_B1_L59	SIO	P19	27.19mm

Table 12: J2 pin-out

4.7 Signal Integrity Considerations

Traces of differential signals pairs are routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length[5]. For applications where traces length has to be matched or timing differences have to be compensated, Table 11 and Table 12 list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 100 ohm. Single ended traces are routed with 60 ohm impedance.

An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.

5 Module revisions and assembly variants

Module revision coded by 4 FPGA BR[3:0] pins, which can be read by FPGA firmware. All these pins should be configures to have internal PULLUP.

5 Difference in signal lines length is negligible for used signal frequency.

6 Related Materials and References

The following documents provide supplementary information useful with this user manual.

6.1 Data Sheets

- Xilinx DS160: Spartan-6 Family Overview
  This overview outlines the features and product selection of the Spartan®-6 family.
  http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf
- Xilinx DS162: Spartan-6 FPGA Data Sheet: DC and Switching Characteristics
  This data sheet contains the DC and switching characteristic specifications for the Spartan®-6 family.
  http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf
- Samtec Razor Beam LSHM series overview.
  http://www.samtec.com/LSHM
- Maxim DS2502-E48 product overview.

  http://www.maxim-ic.com/datasheet/index.mvp/id/3748
- Winbond W25Q128BV product overview.

  http://www.winbond.com/hq/enu/ProductAndSales/ProductLines/FlashMemory/SerialFlash/W25Q128BV.htm
- Maxim DS2432 product page.

  http://www.maximintegrated.com/datasheet/index.mvp/id/2914

6.2 Documentation Archives

- Xilinx Spartan-6 Documentation
  http://www.xilinx.com/support/documentation/spartan-6.htm
- Xilinx Documentation
  http://www.xilinx.com/documentation/
  http://www.xilinx.com/support/documentation/
- Trenz Electronic GigaBee Series Documentation
  http://docs.trenz-electronic.de/Trenz_Electronic/products/TE0600-GigaBee_series/

6.3 User Guides

- Xilinx UG380: Spartan-6 FPGA Configuration User Guide
  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.
  http://www.xilinx.com/support/documentation/user_guides/ug380.pdf
- Xilinx UG381: Spartan-6 FPGA SelectIO Resources

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Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol

consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Document Change History

ver.	date	author	description
0.01	2011-10-01	AIK	Release.
0.02	2011-10-05	AIK	Added B2B pin-out section.
0.03	2011-10-06	AIK	Reformatted pin-out tables. Added eFUSE programming section.
0.04	2011-10-06	AIK	Added board photos. Additions to eFUSE section.
0.05	2011-10-06	AIK	Removed net length information for nets which can't be measured right.
0.06	2011-10-06	AIK	Added power consumption section.
0.07	2011-10-08	AIK	Little fixes after FDR audit.
0.08	2011-10-12	AIK	Fix in eFUSE section.
0.09	2011-11-11	AIK	Added pin numbering description for B2B connectors
0.10	2012-01-20	AIK	Added pin compatibility note and manual reference.
0.11	2012-04-12	AIK	Added FPGA banks VCCIO voltages table.
1.00	2012-04-17	FDR	Updated documentation link. Replaced obsolete ElDesI and RedMine links with current GitHub links. Updated dating convention.
1.01	2012-05-18	AIK	Corrected cross-reference in section 3.2. Corrected LED description.
1.02	2012-06-18	FDR	Removed junction temperature limits under connector current ratings.
1.03	2012-07-18	AIK	Added table with B2B signals summary per FPGA bank
2.01	2012-10-30	AIK	Fork to 01 and 02 board revisions
2.01	2012-11-06	AIK	Fixed bank 1 power options
2.02	2012-11-21	AIK	Updated module diagram
2.03	2012-11-30	AIK	Added Ethernet disable note
2.04	2012-12-19	AIK	Fixed SPI Flash size on block diagram
2.05	2013-01-21	AIK	Added PHY reset note
2.06	2013-03-13	AIK	Connectors current chapter moved to separate document
2.07	2013-03-13	AIK	Changed Bank 1 power supply description and VCCIO0 sources description