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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Spartan-6 LX-45
Co-Processor	-
Speed	125MHz
Flash Size	16MB
RAM Size	256MB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0600-02in

Key Features

- Industrial-grade Xilinx Spartan-6 LX FPGA micromodule (LX45 / LX100 / LX150)
- 10/100/1000 tri-speed Gigabit Ethernet transceiver (PHY)
- 2 x 16-bit-wide 1 Gb (128 MB) or 4Gb (512 MB) DDR3 SDRAM
- 128Mb (16 MB) SPI Flash memory (for configuration and operation) accessible through:
- 1Kb Protected 1-Wire EEPROM with SHA-1 Engine
- JTAG port (SPI indirect)
- FPGA configuration through:
  - B2B connector
  - JTAG port
  - SPI Flash memory
- Plug-on module with 2 × 100-pin high-speed hermaphroditic strips
- Up to 52 differential, up to 109 single-ended (+ 1 dual-purpose) FPGA I/O pins available on B2B strips
- 4.0 A x 1.2 V power rail
- 1.5 A x 1.5 V power rail
- 125 MHz reference clock signal
- Single-ended custom oscillator (option)
- eFUSE bit-stream encryption (LX100 or larger)
- 1 user LED
- Evenly-spread supply pins for good signal integrity
- Other assembly options for cost or performance optimization available upon request.

Table of Contents

1 Technical Specifications

1.1 Components

- Xilinx Spartan-6 LX FPGA:
  - XC6SLX**45**-2FGG484**C** = 43 K logic cells, commercial grade
    XC6SLX**45**-2FGG484**I** = 43 K logic cells, industrial grade
  - XC6SLX**100**-2FGG484**C** = 101 K logic cells, commercial grade
    XC6SLX**100**-2FGG484**I** = 101 K logic cells, industrial grade
  - XC6SLX**150**-2FGG484**C** = 147 K logic cells, commercial grade
    XC6SLX**150**-2FGG484**I** = 147 K logic cells, industrial grade
- 10/100/1000 Gigabit Ethernet transceiver (physical layer)
  Marvell Semiconductor 88E1111
- 2 × independent 16-bit-wide (data-bus) 1 Gigabit (128 megabyte) or 4 Gigabit (512 megabyte) DDR3 SDRAM
- 128 megabit (16 megabyte) serial Flash memory with dual/quad SPI interface
- 48-bit node address chip
  Maxim Integrated Products DS2502-E48
- 1Kb Protected 1-Wire EEPROM with SHA-1 Engine

  Maxim Embedded Security Products DS2432
- 2 x fine-pitch (0.5 mm) 100-pin high-speed (up to 10.0 GHz / 20 Gbps) hermaphroditic strips
  LSHM-150-04.0-L-DV-A-S-K-TR
- Up to 52 differential FPGA input/output pins available on B2B strips
- Up to 109 single-ended (+ 1 dual-purpose) FPGA input/output pins available on B2B strips
- Ethernet (PHY), JTAG and SPI pins available on B2B strips
- 4.0 A high-efficiency DC-DC switching regulator for power rail 1.2V
- 1.5 A high-efficiency DC-DC switching regulator for power rail 1.5V
- 2 x 800 mA DC-DC linear regulator for power rails 2.5V and VCCAUX
- Processor supervisory circuits with power-fail and watchdog
  Texas Instruments TPS3705-33
- 125 MHz clock signal (system + user)
- Footprint for custom single-ended oscillator (option)
- 1 x LED (user)
- Power supply voltage: 3.3 V
- Power supply source: board-to-board interconnect (e.g. carrier board)
- Dimensions: 50 mm × 40 mm (20 cm^2)
- Minimum module height: 8 mm (without connectors)

- Maximum height on carrier board surface: ≈ 13 mm (standard connectors)
- Minimum height on carrier board surface: ≈ 5 mm (standard connectors)
- Weight: 17.2 ± 0.1 g
- Temperature grades:
- commercial (C-type FPGA device)
- industrial (I-type FPGA device)

1.2 Dimensions

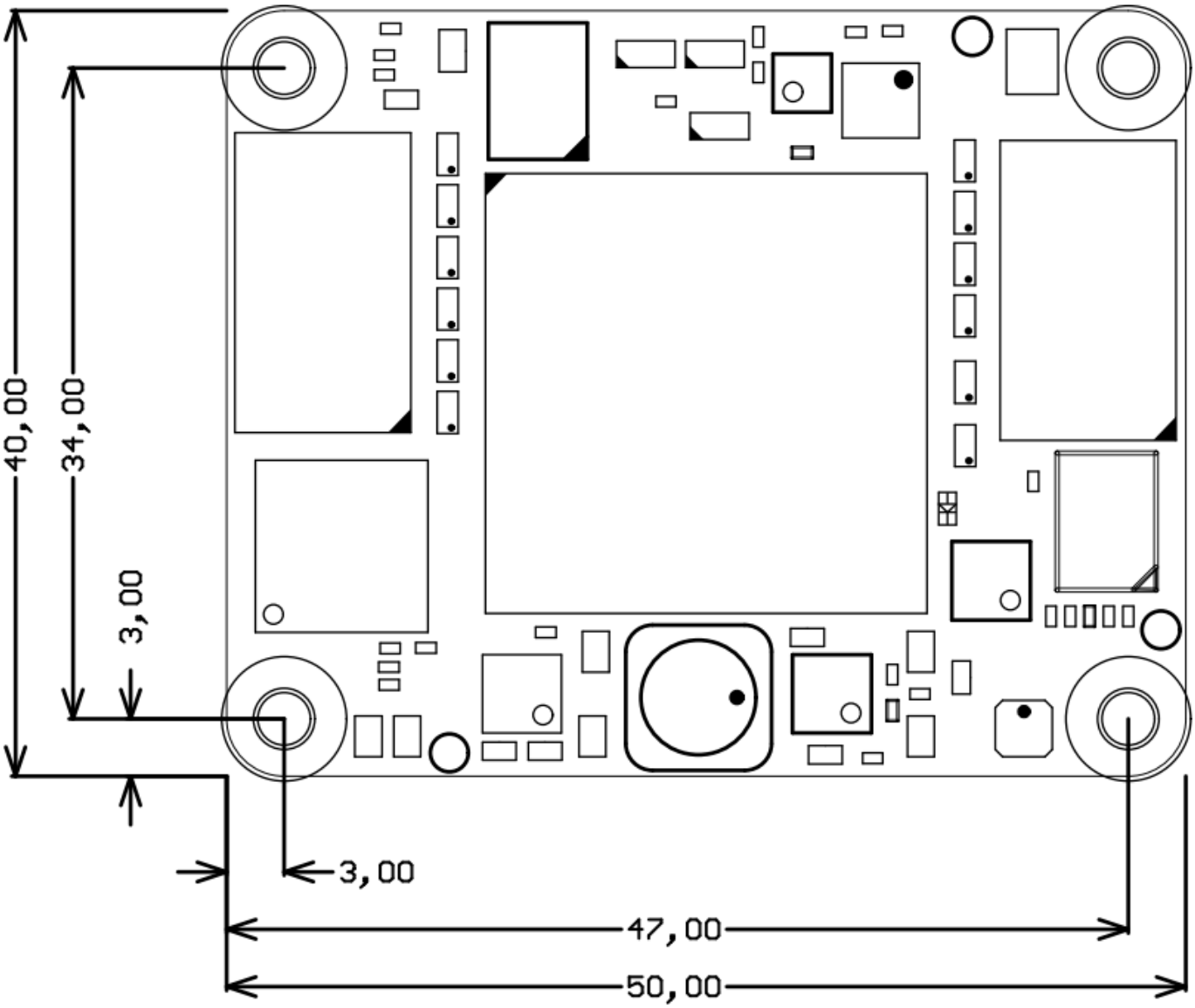

Figure 3: GigaBee board dimensions (top view)

GigaBee XC6SLX can reach a minimum vertical height of about 8 mm, if B2B

2 Detailed Description

2.1 Block Diagram

Figure 4 shows a block diagram of the GigaBee XC6SLX board.

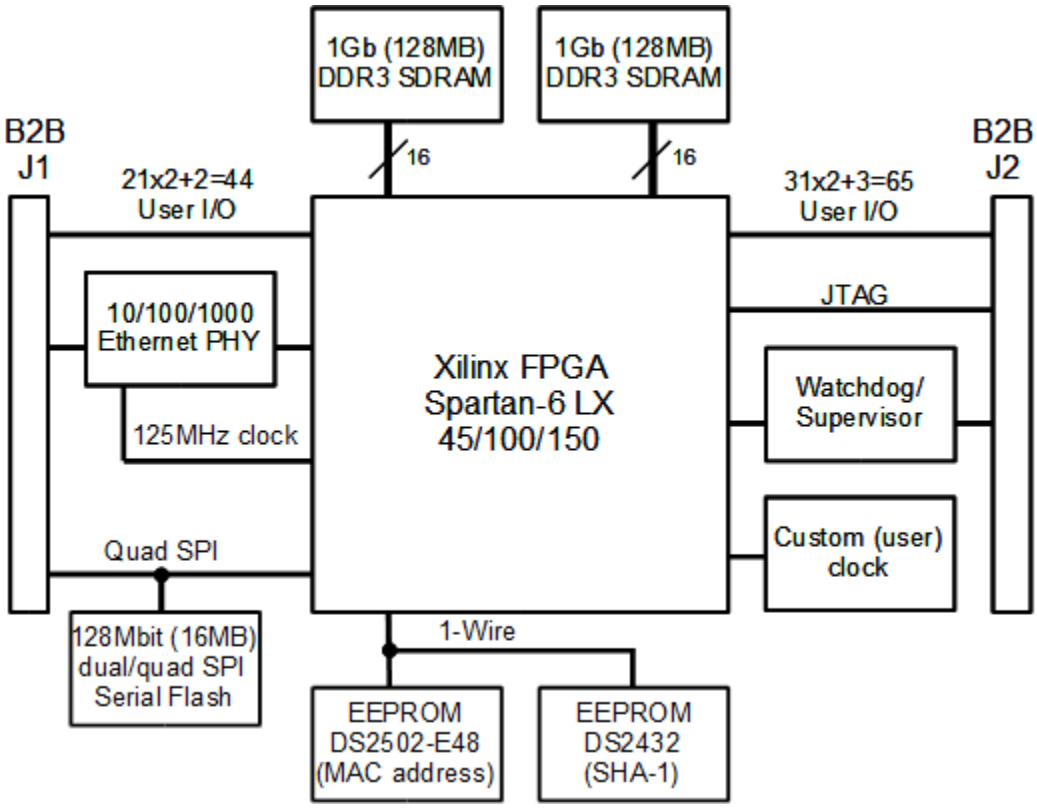

Figure 4: TE0600-02 Block Diagram

2.2 Power Supply

The nominal supply voltage of the GigaBee XC6SLX is 3.3 volt. The minimum supply voltage is 3.0 volt. The maximum supply voltage is 3.45 volt.

Supply voltages beyond the range might affect to device reliability, or even cause permanent damage of the device!

Board power supply diagram is shown in Figure 5.

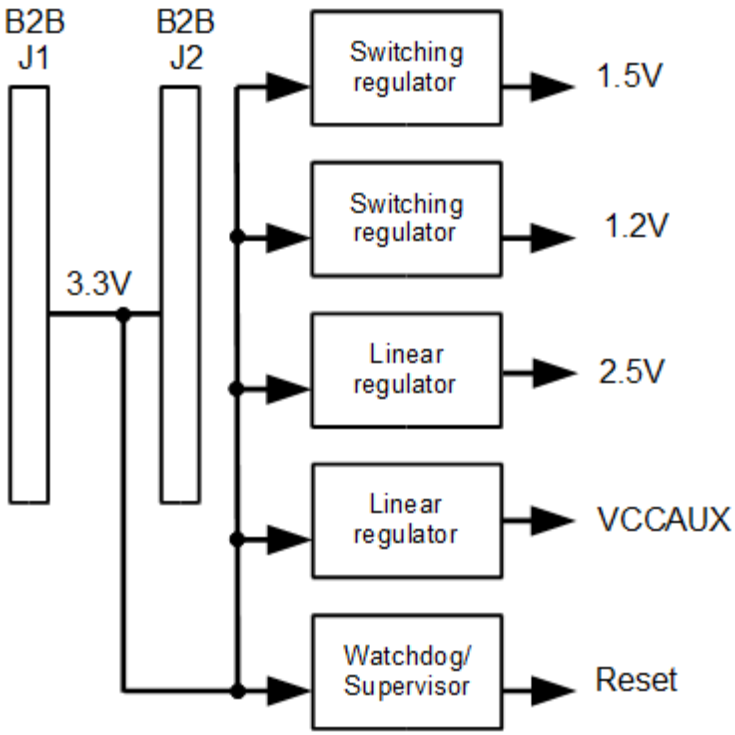

Figure 5: Power supply diagram

2.2.1 Power Supply Sources

GigaBee XC6SLX board must be powered at least in one of the following two ways:

- through B2B connector J1 (pins 1, 3, 5, 7, 9, 11, 13, 15),
- through B2B connector J2 (pins 2, 4, 6, 8, 10, 12).

We recommend to supply the module with all these 14 pins. When one or more of these pins are not power supplied, it or they can be used as power source for user applications.

Please make sure that your logic design does not draw more RMS current per pin than specified in section 2.4 Board-to-board Connectors.

2.2.2 FPGA banks VCCIO power supply

FPGA VCCIO power options shown in Table 2. Default values for configurable voltages shown in braces.

Bank	Supply voltage
B0	VCCIO 0 (3.3 V)
B1	VCCIO 1 (1.5 V)
B2	3.3 V
B3	1.5 V

Table 2: FPGA banks VCCIO power supply

Bank 0 power supply VCCIO 0 can be configured by user to 3.3 V, 2.5 V or

- J2 connector (option: if zero-resistor R80 **is** populated and zero-resistor R79 is **not** populated).

2.2.3.5 VCCAUX Power Rail

It is converted from the 3.3V rail by a linear voltage regulator and can provide up to 0.8 A to:

- FPGA auxiliary circuits;
- J2 connector.

2.2.3.6 VCCIO0 Power Rail

There are 4 options to supply this rail:

- from 3.3 V power rail (if zero-resistor R79 **is** populated[2] and R80 is **not**);
- from 2.5 V power rail (if zero-resistor R80 **is** populated and R79 is **not**);
- from 1.5 V power rail (if zero-resistors R79 and R80 are **not** populated and VCCIO0 connected to 1.5 V power rail);
- from an external power source through J2 B2B connector (pins 1, 3, 5, 7, 9) (if R79 and R80 are **not** populated)

It supplies:

- FPGA bank 0 $V_{CCO.}$

Figure 6 show simplified schematic of power options. Dashed resistors are not populated by default.

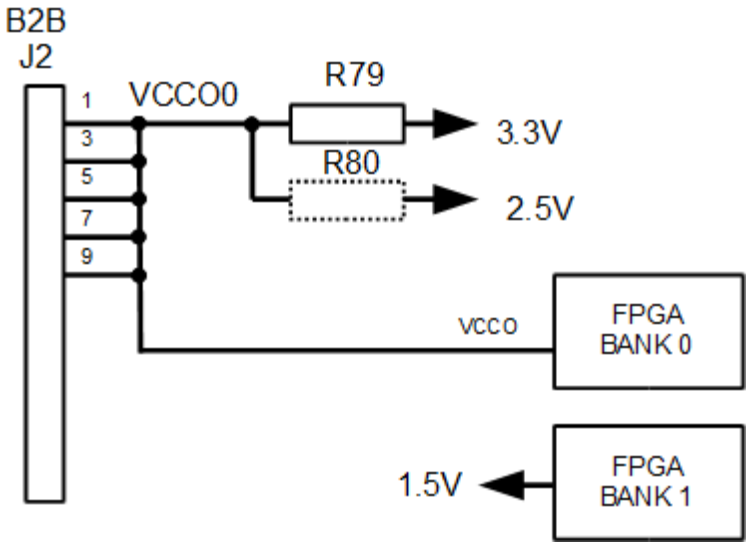

Figure 6: Power options diagram

2 Default assembling for VCCIO0 rail

Table 3 summarizes power rails information.

power-rail name	nominal voltage(V)	maximum current (A)	power source	system supply	user supply
3.3V	3.3	2.4 (3.3 option)	J1, J2	module	J1 (≤1.2 A) J2 (≤1.2 A, ≤2.1 option)
2.5V	2.5	0.8	3.3V ▸ linear	Ethernet	J1 (≤0.3 A) J2 (option)
1.5V	1.5	1.5	3.3V ▸ switch.	DDR3 SDRAM VCCO (1+3)	J1 (≤0.3 A)
1.2V	1.2	4.0	3.3V ▸ switch.	VCCINT Ethernet	J1 (≤0.6 A)
VCCAUX	2.5	0.8	3.3V ▸ linear	FPGA	J2 (≤0.3 A)
VCCCIO0	1.2, 1.5, 1.8, 2.5, 3.3	0.9	J2	VCCO (0)	J2 (≤0.9 A)

Table 3: On-board power rails summary

2.3 Power Supervision

2.3.1 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the supply rail remains below the threshold voltage (2.93 volt). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset prior to a regular system start-up. The typical delay time t_d of 200 ms starts after the supply rail has risen above the threshold voltage.

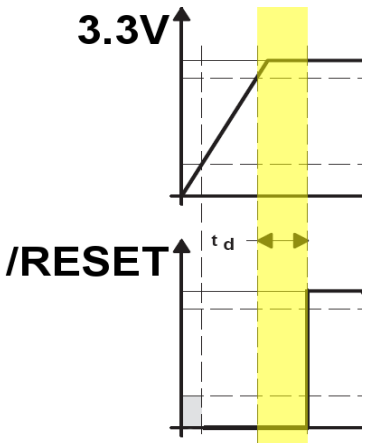

Figure 7: Reset on power-on

After this delay, the /RESET line is reset (high) and the FPGA configuration can start. When the supply rail voltage drops below the threshold voltage, the /RESET line becomes active (low) again and stays active (low) as long as the rail voltage remains below the threshold voltage (2.93 volt). Once the rail voltage raises again and remains over the threshold voltage for more than the typical delay time t_d of 200 ms, the /RESET line returns to the inactive state (high) to allow a new system start-up.

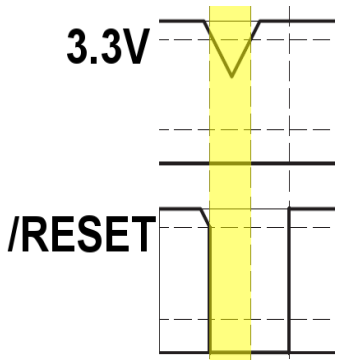

Figure 8: Reset on power drop

2.3.2 Power Fail

GigaBee XC6SLX integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply 3.3 V. When the voltage of the PFI (power-fail comparator input, input pin 16 of connector J2) line drops below 1.25 volt, the /PFO (power-fail comparator output, FPGA pin A2, label IO_L83P_3) line becomes active (low). The user application can sense this line to take action. To set a power fail threshold higher than 1.25 volt, the user can implement a simple resistive voltage divider on the carrier board.

2.4 Board-to-board Connectors

GigaBee XC6SLX mounts two Samtec Razor Beam LSHM connectors (J1 and J2) on the bottom side.

Each connector features the following characteristics:

- rows per connector: 2
- contacts per row: 50
- contacts per connector: 100
- connector gender: hermaphrodite
- pitch: 0.50 mm = 19.7 mil = .0197”
- mated height: min. 5.0 mm | typ. 8.0 mm | max. 12.0 mm
- mating force: min. 39 N | typ. 59 N | max. 62 N
- un-mating force: min. 49 N | typ. 73 N | max. 74 N

For correct operation of the Marvell PHY it is required that PHY Reset pin sees valid low level each time power is applied and also during any brownout situations where system Power is removed for short time, but some pins are not at valid logic levels.

Solutions:

1) if GbE PHY is not used PHY reset pin can be tied off to GND
2) if PLL is used from PHY clock, then PLL "locked" output can be used to reset PHY - as long PLL is not locked, it will keep PHY in reset
3) Reset pulse generation circuit clocked from FPGA internal configuration clock, this circuit can force PHY reset pin to low when external clock from PHY is not available
4) any custom Reset circuit that is guaranteed to drive PHY reset to low level at least once after FPGA configuration when PHY clock is not running.
5) any user logic that is guaranteed to drive PHY reset low after FPGA configuration (without using PHY clock).

Explanation: Marvell PHY samples the MODE pins ONLY when it sees low level on PHY reset input, it does not sample those pins during short power off situations (if the reset pin holds high level because of pin capacitance and high impedance of the pins)! So it is possible that the PHY mode is reset, but the mode pins are not sampled again - this yields in mode setting where 125MHz reference clock from PHY is not available.

2.9 Oscillators

The module has one 25 MHz oscillator for Ethernet PHY (U9). Ethernet PHY provides clock multiplication and resulting 125 MHz clock acts as a system and user clock for the FPGA (FPGA input pin AA12).

Note: For correct generation start, PHY should receive reset pulse. Recommended way to do it it's to connect PHY reset signal (ETHERNET_PHY_RST_N) to LOCKED output of corresponding DCM (DCM which use 125 MHz from PHY).

The module also provides the footprint for custom 3.3 V single-ended oscillator (U12) which can be installed as an option (FPGA input pin Y13).

2.10 User LED

The module contains one user active-low LED connected to FPGA output pin T20. To access more LEDs, use a carrier board and drive FPGA signals connected to B2B connectors. As LED connected to FPGA bank with configurable VCCIO to light LED FPGA pin should in '0' (low) state. To disable LED FPGA pin should be in 'Z' (High impedance).

2.11 Watchdog

GigaBee XS6LX has a watchdog timer that is periodically triggered by a positive or negative transition of the WDI (watchdog input) line (FPGA pin V9). When the supervising system fails to re-trigger the watchdog circuit within the time-out interval (min 1.1 s, typ 1.6 s, max 2.3 s), the /WDO (watchdog output) line becomes active (low). This event also re-initializes the watchdog timer.

If zero-resistors R2 is not assembled, the watchdog is disabled (alternate assembly).

If zero-resistors R2 is assembled, the watchdog can be enabled (standard assembly). In this case there is still two options:

To **enable** the watchdog, after module power-up, drive the WDI signal to generate at least one transition (no matter positive or negative).

To keep watchdog **disabled**, set WDI FPGA signal output to high-impedance. One way to reach this goal is to leave FPGA pin V9 (label IO_L50N_2) undeclared in user constrains file (UCF) and set “unused IOB pins” to “float” in the Xilinx Project Navigator options, see Fig. 12.

(Project properties > Configuration options > Unused IOB Pins > Float).

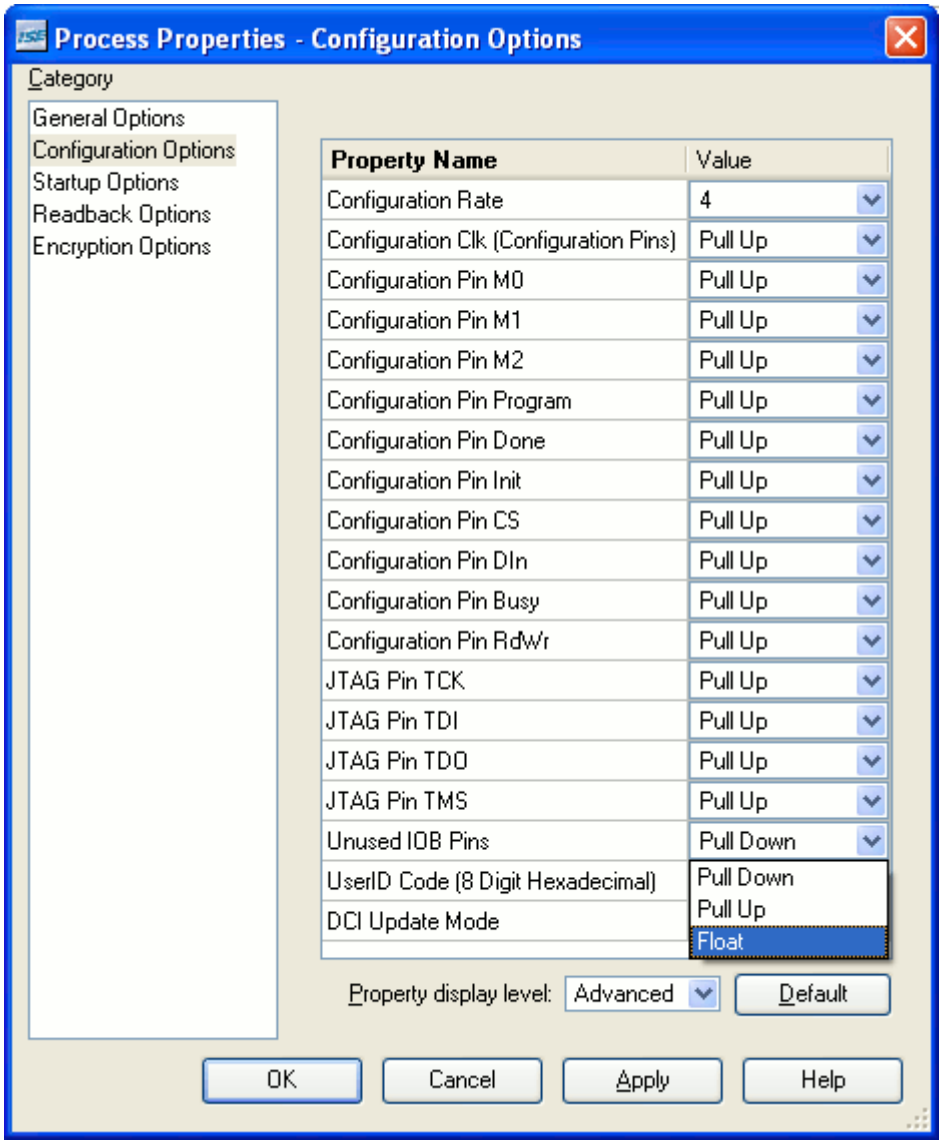

Figure 12: Unused IOB Pins option selection

In the standard assembly, the /WDO (watchdog output) line is left unconnected[3] and the only possibility to reset the module is by driving the /MR (master reset) line active (low) through pin 18 of connector J2.

In the alternate assembly, the /WDO (watchdog output) line is connected through zero-resistor R3 to /MR (master reset) line.

If alternate assembly is used, pin 18 of connector J2 must be left unconnected.

3 Configuration Options

The FPGA on GigaBee XC6SLX board can be configured by means of the following devices:

- Xilinx download cable (JTAG)
- SPI Flash memory

3.1 JTAG Configuration

The FPGA can be configured through the JTAG interface. JTAG signals are connected to B2B connector J2. When GigaBee XC6SLX board is used with the TE0603 carrier board, the JTAG interface can be accessed via connectors J5 and J6 on the carrier board.

3.2 Flash Configuration

Default configuration option for FPGA is “Master Serial/SPI”. The bit-stream for the FPGA is stored in a serial Flash chip (U11). See chapter 2.7 Flash Memory for additional information.

3.3 eFUSE Programming

eFUSE programming feature is not directly supported by GigaBee XC6SLX modules, but it is possible to use it. To program eFUSE, please follow the steps below:

- Connect VCCAUX to 3.3V power rail.

  On TE0603 it can be done by connecting J5 pin 2 or J6 “VREF” (VCCAUX) to J1 any pin from 1,2,3,4 (3.3V). See Figure 13.

- Program eFUSE using JTAG cable and iMPACT software.
- Remove power supply connections to VCCAUX

3 Resistor R3 is not populated.

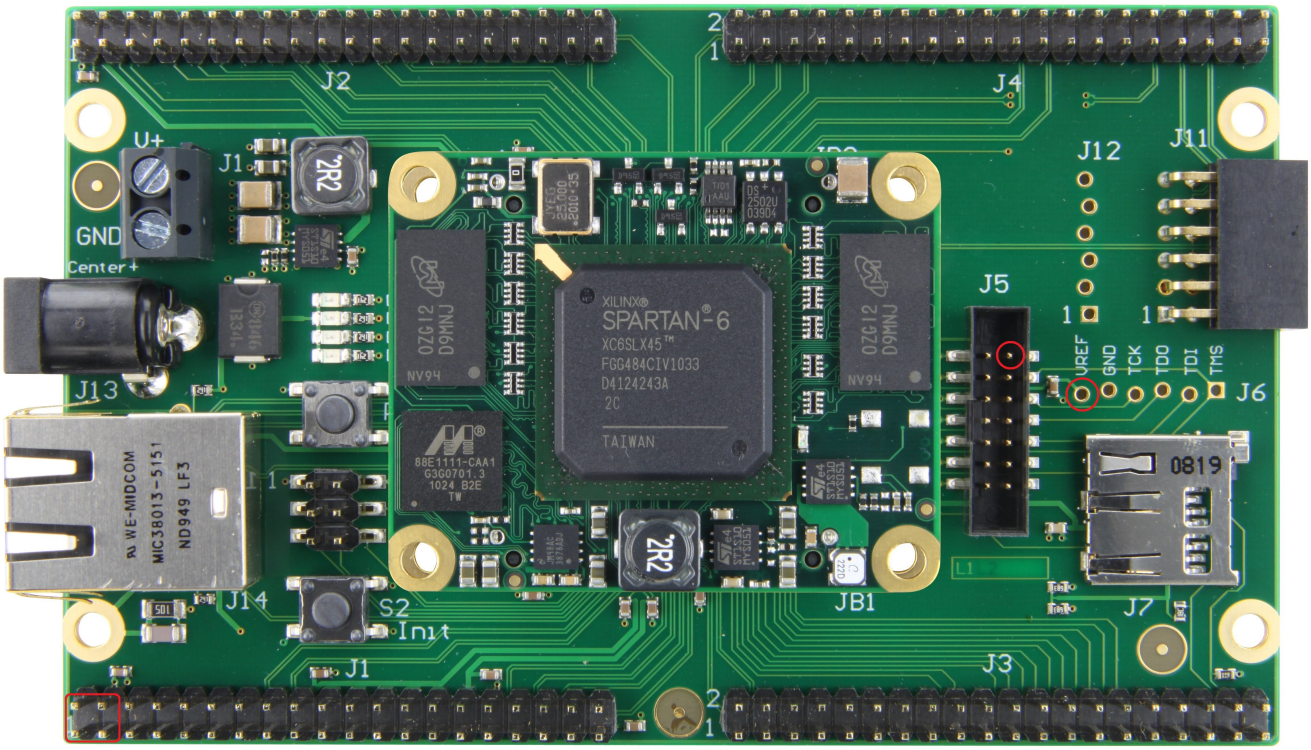

Figure 13: eFUSE Powering

4 B2B Connectors Pin Descriptions

This section describes how the various pins on B2B connectors J1 and J2 connects to TE0600 on-board components. There are five main signal types connected to B2B connectors:

- FPGA users signals;
- FPGA system signals;
- Power signals;
- Ethernet PHY signals;
- Other system signals.

FPGA Bank	Single-ended	Differential	Total	VCCIO
Bank 0	1	22	45	VCCIO 0 (3.3 V)
Bank 1	1	6	13	VCCIO 1 (1.5 V)
Bank 2	3	21	45	3.3 V
Bank 3	0	3	6	1.5 V
	5	52	109	

Table 9: B2B signals count

4.4 External Bank 2 differential clock connection

TE0600-02 module have optional connection to FPGA bank 2 differential clock input pins. To provide connection from B2B_B2_L41_P signal to Y13 FPGA pin, zero-resistor R69 should be soldered. To provide connection B2B_B2_L41_N signal to AB13 FPGA pin, zero-resistor R81 should be soldered. Note that in this case optional user oscillator U13 can't be used.

4.5 J1 Pin-out

J1 pin	Net	Type	FPGA pin	Net Length	J1 pin	Net	Type	FPGA pin	Net Length
1	3.3V	POW	-	-	2	GND	GND	-	-
3	3.3V	POW	-	-	4	PHY_MDI0_P	PHY	-	-
5	3.3V	POW	-	-	6	PHY_MDI0_N	PHY	-	-
7	3.3V	POW	-	-	8	GND	GND	-	-
9	3.3V	POW	-	-	10	PHY_MDI1_P	PHY	-	-
11	3.3V	POW	-	-	12	PHY_MDI1_N	PHY	-	-
13	3.3V	POW	-	-	14	PHY_AVDD	PHY	-	-
15	3.3V	POW	-	-	16	PHY_MDI2_P	PHY	-	-
17	PHY_L10	PHY	-	-	18	PHY_MDI2_N	PHY	-	-
19	PHY_L100	PHY	-	-	20	GND	GND	-	-
21	PHY_L1000	PHY	-	-	22	PHY_MDI3_P	PHY	-	-
23	PHY_DUP	PHY	-	-	24	PHY_MDI3_N	PHY	-	-
25	PHY_LED_TX	PHY	-	-	26	GND	GND	-	-
27	PHY_LED_RX	PHY	-	-	28	EN	TE	-	-
29	GND	GND	-	-	30	INIT	CONFIG	T6	-
31	B2B_B2_L57_N	DIO	AB4	8.66mm	32	B2B_B2_L32_N	SIO	AB11	8.12mm
33	B2B_B2_L57_P	DIO	AA4	9.84mm	34	GND	GND	-	-
35	B2B_B2_L49_N	DIO	AB6	8.66mm	36	B2B_B2_L60_P	DIO	T7	9.96mm
37	B2B_B2_L49_P	DIO	AA6	9.58mm	38	B2B_B2_L60_N	DIO	R7	11.16mm
39	2.5V	POW	-	-	40	B2B_B2_L59_N	DIO	R8	11.42mm
41	1.2V	POW	-	-	42	B2B_B2_L59_P	DIO	R9	11.36mm
43	1.2V	POW	-	-	44	GND	GND	-	-
45	B2B_B2_L48_N	DIO	AB7	9.98mm	46	B2B_B2_L44_N	DIO	Y10	11.34mm
47	B2B_B2_L48_P	DIO	Y7	10.98mm	48	B2B_B2_L44_P	DIO	W10	10.21mm
49	B2B_B2_L45_N	DIO	AB8	10.60mm	50	B2B_B2_L42_N	DIO	W11	7.52mm
51	B2B_B2_L45_P	DIO	AA8	11.053mm	52	B2B_B2_L42_P	DIO	V11	8.36mm
53	GND	GND	-	-	54	GND	GND	-	-
55	B2B_B2_L43_N	DIO	AB9	13.75mm	56	B2B_B2_L18_P	DIO	V13	7.94mm
57	B2B_B2_L43_P	DIO	Y9	12.97mm	58	B2B_B2_L18_N	DIO	W13	6.96mm
59	B2B_B2_L41_N	DIO	AB10, AB13	10.33mm	60	B2B_B2_L8_N	DIO	U16	9.92mm
61	B2B_B2_L41_P	DIO	AA10, Y13	11.01mm	62	B2B_B2_L8_P	DIO	U17	9.94mm
63	GND	GND	-	-	64	GND	GND	-	-
65	B2B_B2_L21_P	DIO	Y15	13.12mm	66	B2B_B2_L11_P	DIO	V17	8.31mm
67	B2B_B2_L21_N	DIO	AB15	12.37mm	68	B2B_B2_L11_N	DIO	W17	7.29mm
69	B2B_B2_L15_P	DIO	Y17	14.20mm	70	B2B_B2_L6_P	DIO	W18	7.40mm
71	B2B_B2_L15_N	DIO	AB17	13.77mm	72	B2B_B2_L6_N	DIO	Y18	6.94mm
73	GND	GND	-	-	74	GND	GND	-	-
75	B2B_B2_L31_N	SIO	AB12	12.30mm	76	B2B_B2_L5_P	DIO	Y19	6.18mm

J2 pin	Net	Type	FPGA pin	Net Length	J2 pin	Net	Type	FPGA pin	Net Length
59	GND	GND	-	-	60	GND	GND	-	-
61	B2B_B0_L62_P	DIO	D15	7.44mm	62	B2B_B0_L38_N	DIO	A13	8.38mm
63	B2B_B0_L62_N	DIO	C16	6.95mm	64	B2B_B0_L38_P	DIO	C13	9.87mm
65	B2B_B0_L66_P	DIO	E16	8.07mm	66	B2B_B0_L50_N	DIO	A14	7.66mm
67	B2B_B0_L66_N	DIO	D17	6.96mm	68	B2B_B0_L50_P	DIO	B14	8.87mm
69	GND	GND	-	-	70	GND	GND	-	-
71	B2B_B1_L10_P	DIO	F16	9.56mm	72	B2B_B0_L51_N	DIO	A15	10.22mm
73	B2B_B1_L10_N	DIO	F17	8.85mm	74	B2B_B0_L51_P	DIO	C15	10.67mm
75	B2B_B1_L9_P	DIO	G16	10.59mm	76	B2B_B0_L63_N	DIO	A16	7.95mm
77	B2B_B1_L9_N	DIO	G17	10.23mm	78	B2B_B0_L63_P	DIO	B16	9.12mm
79	GND	GND	-	-	80	GND	GND	-	-
81	B2B_B1_L21_N	DIO	J16	13.22mm	82	B2B_B0_L64_N	DIO	A17	9.55mm
83	B2B_B1_L21_P	DIO	K16	14.41mm	84	B2B_B0_L64_P	DIO	C17	10.25mm
85	B2B_B1_L61_P	DIO	L17	14.89mm	86	B2B_B0_L65_N	DIO	A18	8.51mm
87	B2B_B1_L61_N	DIO	K18	13.59mm	88	B2B_B0_L65_P	DIO	B18	9.29mm
89	GND	GND	-	-	90	GND	GND	-	-
91	VCCAUX	POW	-	-	92	B2B_B1_L20_P	DIO	A20	8.02mm
93	TMS	JTAG	C18	-	94	B2B_B1_L20_N	DIO	A21	7.82mm
95	TDI	JTAG	E18	-	96	B2B_B1_L19_P	DIO	B21	9.63mm
97	TDO	JTAG	A19	-	98	B2B_B1_L19_N	DIO	B22	9.06mm
99	TCK	JTAG	G15	-	100	B2B_B1_L59	SIO	P19	27.19mm

Table 12: J2 pin-out

4.7 Signal Integrity Considerations

Traces of differential signals pairs are routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length[5]. For applications where traces length has to be matched or timing differences have to be compensated, Table 11 and Table 12 list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 100 ohm. Single ended traces are routed with 60 ohm impedance.

An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.

5 Module revisions and assembly variants

Module revision coded by 4 FPGA BR[3:0] pins, which can be read by FPGA firmware. All these pins should be configures to have internal PULLUP.

5 Difference in signal lines length is negligible for used signal frequency.

6 Related Materials and References

The following documents provide supplementary information useful with this user manual.

6.1 Data Sheets

- Xilinx DS160: Spartan-6 Family Overview
  This overview outlines the features and product selection of the Spartan®-6 family.
  http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf
- Xilinx DS162: Spartan-6 FPGA Data Sheet: DC and Switching Characteristics
  This data sheet contains the DC and switching characteristic specifications for the Spartan®-6 family.
  http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf
- Samtec Razor Beam LSHM series overview.
  http://www.samtec.com/LSHM
- Maxim DS2502-E48 product overview.

  http://www.maxim-ic.com/datasheet/index.mvp/id/3748
- Winbond W25Q128BV product overview.

  http://www.winbond.com/hq/enu/ProductAndSales/ProductLines/FlashMemory/SerialFlash/W25Q128BV.htm
- Maxim DS2432 product page.

  http://www.maximintegrated.com/datasheet/index.mvp/id/2914

6.2 Documentation Archives

- Xilinx Spartan-6 Documentation
  http://www.xilinx.com/support/documentation/spartan-6.htm
- Xilinx Documentation
  http://www.xilinx.com/documentation/
  http://www.xilinx.com/support/documentation/
- Trenz Electronic GigaBee Series Documentation
  http://docs.trenz-electronic.de/Trenz_Electronic/products/TE0600-GigaBee_series/

6.3 User Guides

- Xilinx UG380: Spartan-6 FPGA Configuration User Guide
  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.
  http://www.xilinx.com/support/documentation/user_guides/ug380.pdf
- Xilinx UG381: Spartan-6 FPGA SelectIO Resources

7 Glossary of Abbreviations and Acronyms

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

A CAUTION notice denotes a risk. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in a fault. (undesired condition that can lead to an error) Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

API	application programming interface
B2B	board-to-board
DSP	digital signal processing; digital signal processor
EDK	Embedded Development Kit
IOB	input / output blocks; I/O blocks
IP	intellectual property
ISP	In-System Programmability
OTP	one-time programmable
PB	push button
SDK	Software Development Kit
TE	Trenz Electronic
XPS	Xilinx Platform Studio

9 Environmental protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

9.1 REACH (Registration, Evaluation, Authorisation and Restriction of Chemicals) compliance statement

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet.

According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products.

Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

9.2 RoHS (Restriction of Hazardous Substances) compliance statement

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

9.3 WEEE (Waste Electrical and Electronic Equipment)

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment.

Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol

consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.