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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Spartan-6 LX-150
Co-Processor	-
Speed	125MHz
Flash Size	16MB
RAM Size	256MB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0600-02ivf

Key Features

- Industrial-grade Xilinx Spartan-6 LX FPGA micromodule (LX45 / LX100 / LX150)
- 10/100/1000 tri-speed Gigabit Ethernet transceiver (PHY)
- 2 x 16-bit-wide 1 Gb (128 MB) or 4Gb (512 MB) DDR3 SDRAM
- 128Mb (16 MB) SPI Flash memory (for configuration and operation) accessible through:
- 1Kb Protected 1-Wire EEPROM with SHA-1 Engine
- JTAG port (SPI indirect)
- FPGA configuration through:
  - B2B connector
  - JTAG port
  - SPI Flash memory
- Plug-on module with 2 × 100-pin high-speed hermaphroditic strips
- Up to 52 differential, up to 109 single-ended (+ 1 dual-purpose) FPGA I/O pins available on B2B strips
- 4.0 A x 1.2 V power rail
- 1.5 A x 1.5 V power rail
- 125 MHz reference clock signal
- Single-ended custom oscillator (option)
- eFUSE bit-stream encryption (LX100 or larger)
- 1 user LED
- Evenly-spread supply pins for good signal integrity
- Other assembly options for cost or performance optimization available upon request.

Table of Contents

1 Technical Specifications

1.1 Components

- Xilinx Spartan-6 LX FPGA:
  - XC6SLX**45**-2FGG484**C** = 43 K logic cells, commercial grade
    XC6SLX**45**-2FGG484**I** = 43 K logic cells, industrial grade
  - XC6SLX**100**-2FGG484**C** = 101 K logic cells, commercial grade
    XC6SLX**100**-2FGG484**I** = 101 K logic cells, industrial grade
  - XC6SLX**150**-2FGG484**C** = 147 K logic cells, commercial grade
    XC6SLX**150**-2FGG484**I** = 147 K logic cells, industrial grade
- 10/100/1000 Gigabit Ethernet transceiver (physical layer)
  Marvell Semiconductor 88E1111
- 2 × independent 16-bit-wide (data-bus) 1 Gigabit (128 megabyte) or 4 Gigabit (512 megabyte) DDR3 SDRAM
- 128 megabit (16 megabyte) serial Flash memory with dual/quad SPI interface
- 48-bit node address chip
  Maxim Integrated Products DS2502-E48
- 1Kb Protected 1-Wire EEPROM with SHA-1 Engine

  Maxim Embedded Security Products DS2432
- 2 x fine-pitch (0.5 mm) 100-pin high-speed (up to 10.0 GHz / 20 Gbps) hermaphroditic strips
  LSHM-150-04.0-L-DV-A-S-K-TR
- Up to 52 differential FPGA input/output pins available on B2B strips
- Up to 109 single-ended (+ 1 dual-purpose) FPGA input/output pins available on B2B strips
- Ethernet (PHY), JTAG and SPI pins available on B2B strips
- 4.0 A high-efficiency DC-DC switching regulator for power rail 1.2V
- 1.5 A high-efficiency DC-DC switching regulator for power rail 1.5V
- 2 x 800 mA DC-DC linear regulator for power rails 2.5V and VCCAUX
- Processor supervisory circuits with power-fail and watchdog
  Texas Instruments TPS3705-33
- 125 MHz clock signal (system + user)
- Footprint for custom single-ended oscillator (option)
- 1 x LED (user)
- Power supply voltage: 3.3 V
- Power supply source: board-to-board interconnect (e.g. carrier board)
- Dimensions: 50 mm × 40 mm (20 cm^2)
- Minimum module height: 8 mm (without connectors)

- Maximum height on carrier board surface: ≈ 13 mm (standard connectors)
- Minimum height on carrier board surface: ≈ 5 mm (standard connectors)
- Weight: 17.2 ± 0.1 g
- Temperature grades:
- commercial (C-type FPGA device)
- industrial (I-type FPGA device)

1.2 Dimensions

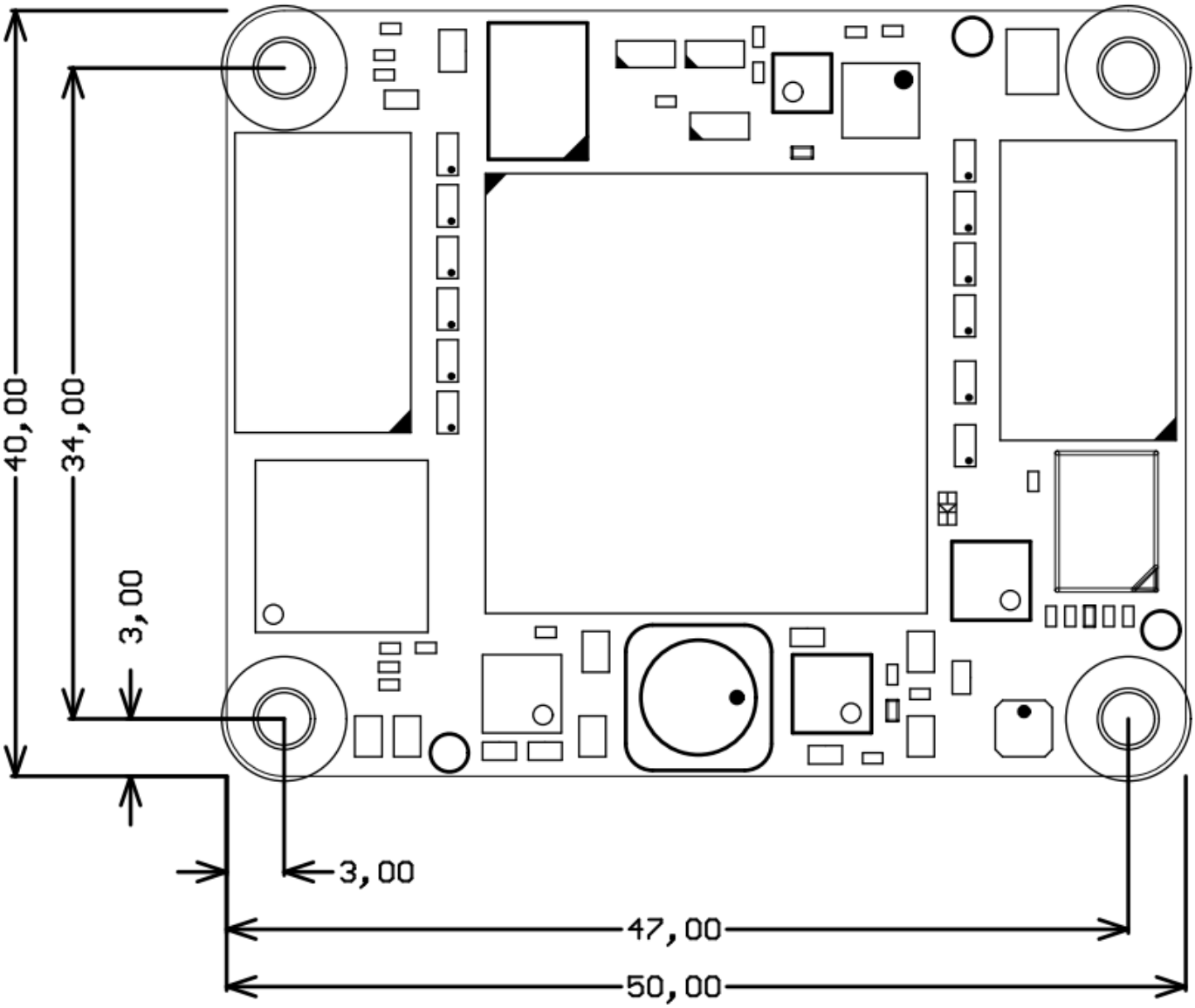

Figure 3: GigaBee board dimensions (top view)

GigaBee XC6SLX can reach a minimum vertical height of about 8 mm, if B2B

connectors are not assembled. The maximum component height on the module board on the top side is about 3.5 mm. The maximum component height on the module board on the bottom side is about 3.0 mm.

The typical minimum and maximum height from the carrier board surface, of a GigaBee XC6SLX when it mounted on a carrier board, is respectively about 5.0 mm and about 13 mm.

GigaBee XC6SLX has 4 mounting holes, one in each corner. The module can be fixed by screwing M3 screws (ISO 262) onto a carrier board through those mounting holes.

GigaBee XC6SLX weighs between 17.1 and 17.3 g with standard connectors.

1.3 Power Consumption

Power consumption of GigaBee XC6SLX modules highly depend on the FPGA design implemented. Some typical power consumptions are provided in Table 1 for the following reference systems:

- Boards – GigaBee XC6SLX 45/100/150
- Base board – TE0603-02
- Power supply – 5 V from baseboard
- Connected Gigabit Ethernet cable

FPGA type	Unconfigured	Configured with Web-server reference design
LX45	0.15 A	0.6 A
LX100	0.17 A	0.5 A
LX150	0.2 A	0.5 A

Table 1: Power consumption

2 Detailed Description

2.1 Block Diagram

Figure 4 shows a block diagram of the GigaBee XC6SLX board.

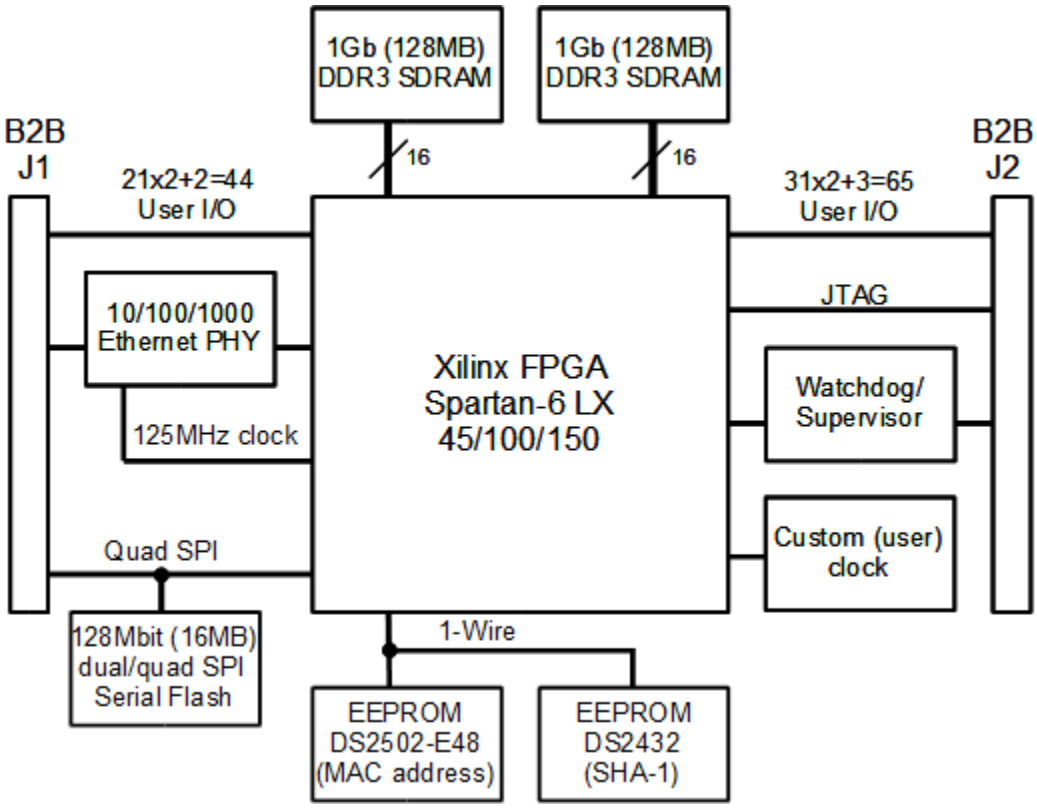

Figure 4: TE0600-02 Block Diagram

2.2 Power Supply

The nominal supply voltage of the GigaBee XC6SLX is 3.3 volt. The minimum supply voltage is 3.0 volt. The maximum supply voltage is 3.45 volt.

Supply voltages beyond the range might affect to device reliability, or even cause permanent damage of the device!

Board power supply diagram is shown in Figure 5.

- J2 connector (option: if zero-resistor R80 **is** populated and zero-resistor R79 is **not** populated).

2.2.3.5 VCCAUX Power Rail

It is converted from the 3.3V rail by a linear voltage regulator and can provide up to 0.8 A to:

- FPGA auxiliary circuits;
- J2 connector.

2.2.3.6 VCCIO0 Power Rail

There are 4 options to supply this rail:

- from 3.3 V power rail (if zero-resistor R79 **is** populated[2] and R80 is **not**);
- from 2.5 V power rail (if zero-resistor R80 **is** populated and R79 is **not**);
- from 1.5 V power rail (if zero-resistors R79 and R80 are **not** populated and VCCIO0 connected to 1.5 V power rail);
- from an external power source through J2 B2B connector (pins 1, 3, 5, 7, 9) (if R79 and R80 are **not** populated)

It supplies:

- FPGA bank 0 $V_{CCO.}$

Figure 6 show simplified schematic of power options. Dashed resistors are not populated by default.

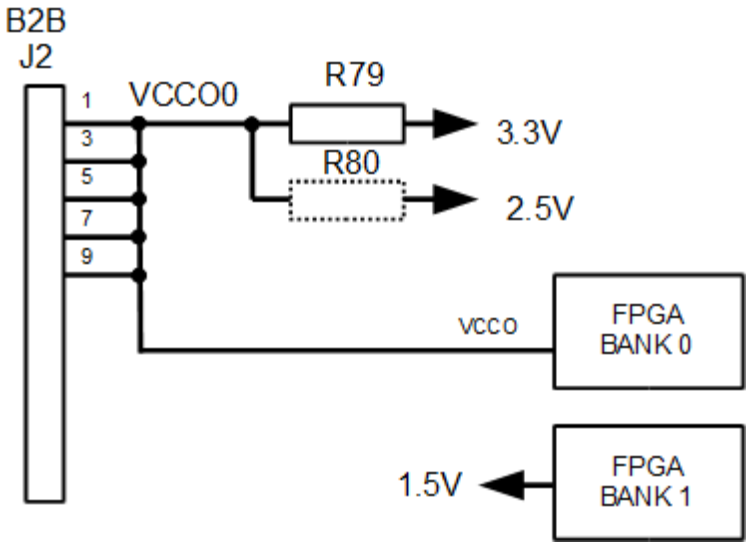

Figure 6: Power options diagram

2 Default assembling for VCCIO0 rail

Table 3 summarizes power rails information.

power-rail name	nominal voltage(V)	maximum current (A)	power source	system supply	user supply
3.3V	3.3	2.4 (3.3 option)	J1, J2	module	J1 (≤1.2 A) J2 (≤1.2 A, ≤2.1 option)
2.5V	2.5	0.8	3.3V ▸ linear	Ethernet	J1 (≤0.3 A) J2 (option)
1.5V	1.5	1.5	3.3V ▸ switch.	DDR3 SDRAM VCCO (1+3)	J1 (≤0.3 A)
1.2V	1.2	4.0	3.3V ▸ switch.	VCCINT Ethernet	J1 (≤0.6 A)
VCCAUX	2.5	0.8	3.3V ▸ linear	FPGA	J2 (≤0.3 A)
VCCCIO0	1.2, 1.5, 1.8, 2.5, 3.3	0.9	J2	VCCO (0)	J2 (≤0.9 A)

Table 3: On-board power rails summary

2.3 Power Supervision

2.3.1 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the supply rail remains below the threshold voltage (2.93 volt). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset prior to a regular system start-up. The typical delay time t_d of 200 ms starts after the supply rail has risen above the threshold voltage.

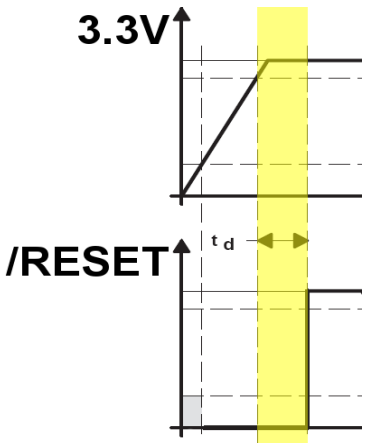

Figure 7: Reset on power-on

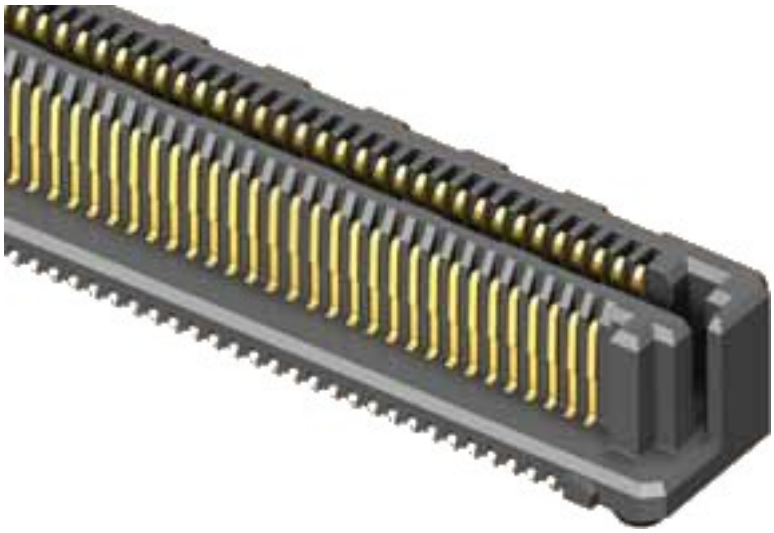

Figure 9: Samtec Razor Beam LSHM connector

The overall number of connector contacts on the GigaBee XC6SLX is 200.

Samtec Razor Beam LSHM is a high-speed interconnect system with very fine pitch (50 mil) and low profile design. Razor Beam connectors are well suited for high speed applications with performance up to 11.5 GHz (23 Gb/s) at -3 dB insertion loss. Razor Beam contacts are ideal for high speed and rugged applications featuring undercut retention notches that increase the withdrawal force and provide an audible click when the contacts engage. In addition, the self-mating (hermaphroditic) design can help reduce inventory costs. The LSHM Series features also optional shielding for EMI protection (default on GigaBee XC6SLX).

Samtec Razor Beam LSHM connectors are keyed. On the bottom side of the GigaBee XSL6, the connectors are assembled in such a way to prevent the module to be reverse mounted on carrier boards.

Samtec Razor Beam LSHM are available in different lead styles, see Table 4 for details.

lead style	A [mm]	B [mm]
-02.5	3.95	1.00
-03.0	4.45	1.50
-04.0	5.45	2.50
-06.0	7.45	4.50

Table 4: Samtec Razor Beam LSHM lead styles

Ordering codes for connectors J1 and J2 used in GigaBee XC6SLX board, and their mating connectors are given in Table 6.

lead style	gender	Samtec	Trenz Electronic
-02.5	hermaphroditic	LSHM-150-02.5-L-DV-A-S-K-TR	23836
-03.0	hermaphroditic	LSHM-150-03.0-L-DV-A-S-K-TR	23837
-04.0	hermaphroditic	LSHM-150-04.0-L-DV-A-S-K-TR	23838
-06.0	hermaphroditic	LSHM-150-06.0-L-DV-A-S-K-TR	23839

Table 6: Ordered codes of recommended B2B connectors

2.4.1 Connector Speed Rating

Samtec provides speed rating data for the Samtec Razor Beam LSHM connector system. The data presented in Table 7 are applicable only to the maximum and minimum mated heights. The speed rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signalling environment.

mated height	5 mm	12 mm
single-ended signalling	11.5 GHz 23.0 Gb/s	7.5 GHz 15.0 Gb/s
differential pair signalling	7.0 GHz 14.0 Gb/s	6.5 GHz 13.0 Gb/s

Table 7: Connectors speed rating

More details can be found in the Samtec Razor Beam LSHM series overview (“High Speed Characterization Reports”).

2.5 EPROM

GigaBee XC6SLX board contains a Maxim DS2502-E48 node address chip with factory-programmed valid MAC-48 address and 768 bits of OTP-EPROM memory for user data.

Address chip provide convenient data access through 1-Wire interface up to 16.3 kbps (FPGA pin T11).

More information can be found in the Maxim DS2502-E48 product overwiew.

Additional 1Kb protected 1-Wire EEPROM with SHA-1 engine DS2432 accessible via the same line.

More information can be found at the Maxim DS2432 product page.

2.6 DDR3 SDRAM Memory

The board contains two 1 Gb (128 MB) or 4 Gb (512 MB) DDR3 SDRAM chips. Data width of each chip is 16 bit. DDR3 memory connected to FPGA bank 1 and FPGA bank 3. Spartan-6 Memory controller Blocks operations can be merged to implement effective 32-bit memory interface. Refer Xilinx XAPP496 for detailed information.

In the standard assembly, the /WDO (watchdog output) line is left unconnected[3] and the only possibility to reset the module is by driving the /MR (master reset) line active (low) through pin 18 of connector J2.

In the alternate assembly, the /WDO (watchdog output) line is connected through zero-resistor R3 to /MR (master reset) line.

If alternate assembly is used, pin 18 of connector J2 must be left unconnected.

3 Configuration Options

The FPGA on GigaBee XC6SLX board can be configured by means of the following devices:

- Xilinx download cable (JTAG)
- SPI Flash memory

3.1 JTAG Configuration

The FPGA can be configured through the JTAG interface. JTAG signals are connected to B2B connector J2. When GigaBee XC6SLX board is used with the TE0603 carrier board, the JTAG interface can be accessed via connectors J5 and J6 on the carrier board.

3.2 Flash Configuration

Default configuration option for FPGA is “Master Serial/SPI”. The bit-stream for the FPGA is stored in a serial Flash chip (U11). See chapter 2.7 Flash Memory for additional information.

3.3 eFUSE Programming

eFUSE programming feature is not directly supported by GigaBee XC6SLX modules, but it is possible to use it. To program eFUSE, please follow the steps below:

- Connect VCCAUX to 3.3V power rail.

  On TE0603 it can be done by connecting J5 pin 2 or J6 “VREF” (VCCAUX) to J1 any pin from 1,2,3,4 (3.3V). See Figure 13.

- Program eFUSE using JTAG cable and iMPACT software.
- Remove power supply connections to VCCAUX

3 Resistor R3 is not populated.

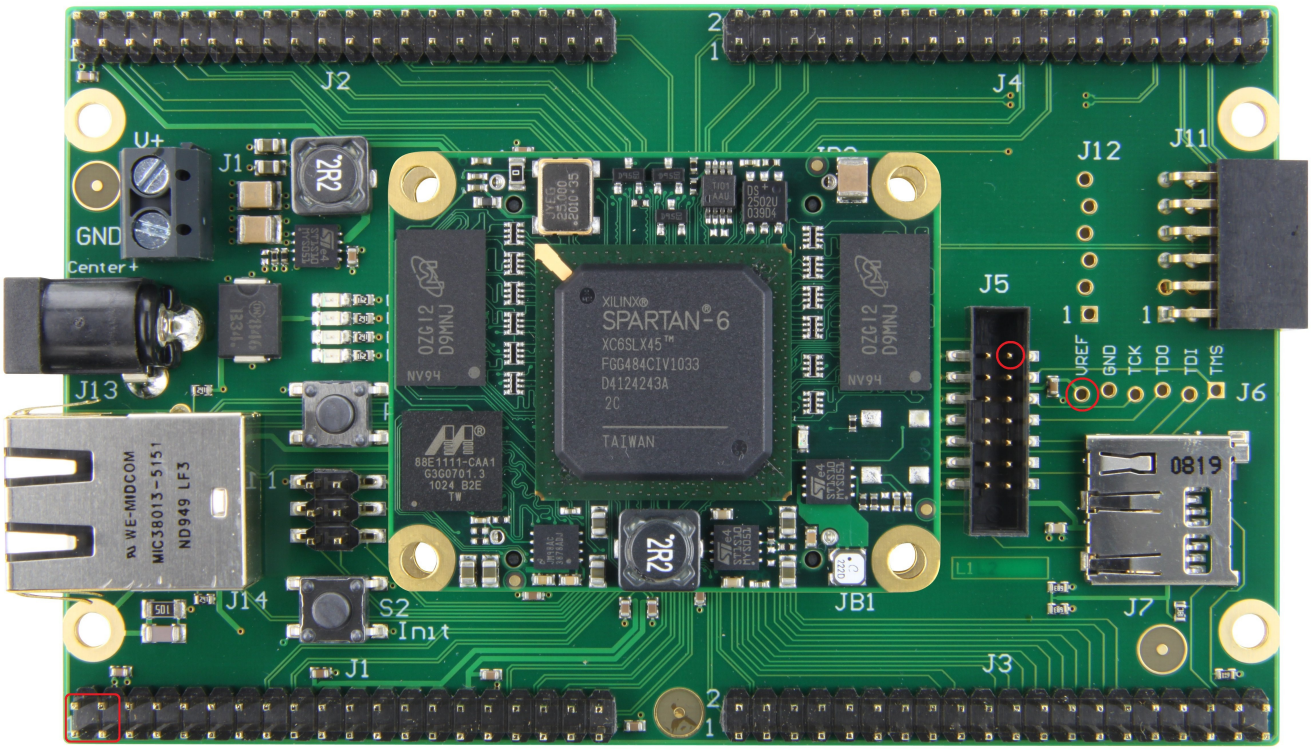

Figure 13: eFUSE Powering

4 B2B Connectors Pin Descriptions

This section describes how the various pins on B2B connectors J1 and J2 connects to TE0600 on-board components. There are five main signal types connected to B2B connectors:

- FPGA users signals;
- FPGA system signals;
- Power signals;
- Ethernet PHY signals;
- Other system signals.

FPGA Bank	Single-ended	Differential	Total	VCCIO
Bank 0	1	22	45	VCCIO 0 (3.3 V)
Bank 1	1	6	13	VCCIO 1 (1.5 V)
Bank 2	3	21	45	3.3 V
Bank 3	0	3	6	1.5 V
	5	52	109	

Table 9: B2B signals count

4.4 External Bank 2 differential clock connection

TE0600-02 module have optional connection to FPGA bank 2 differential clock input pins. To provide connection from B2B_B2_L41_P signal to Y13 FPGA pin, zero-resistor R69 should be soldered. To provide connection B2B_B2_L41_N signal to AB13 FPGA pin, zero-resistor R81 should be soldered. Note that in this case optional user oscillator U13 can't be used.

4.5 J1 Pin-out

J1 pin	Net	Type	FPGA pin	Net Length	J1 pin	Net	Type	FPGA pin	Net Length
1	3.3V	POW	-	-	2	GND	GND	-	-
3	3.3V	POW	-	-	4	PHY_MDI0_P	PHY	-	-
5	3.3V	POW	-	-	6	PHY_MDI0_N	PHY	-	-
7	3.3V	POW	-	-	8	GND	GND	-	-
9	3.3V	POW	-	-	10	PHY_MDI1_P	PHY	-	-
11	3.3V	POW	-	-	12	PHY_MDI1_N	PHY	-	-
13	3.3V	POW	-	-	14	PHY_AVDD	PHY	-	-
15	3.3V	POW	-	-	16	PHY_MDI2_P	PHY	-	-
17	PHY_L10	PHY	-	-	18	PHY_MDI2_N	PHY	-	-
19	PHY_L100	PHY	-	-	20	GND	GND	-	-
21	PHY_L1000	PHY	-	-	22	PHY_MDI3_P	PHY	-	-
23	PHY_DUP	PHY	-	-	24	PHY_MDI3_N	PHY	-	-
25	PHY_LED_TX	PHY	-	-	26	GND	GND	-	-
27	PHY_LED_RX	PHY	-	-	28	EN	TE	-	-
29	GND	GND	-	-	30	INIT	CONFIG	T6	-
31	B2B_B2_L57_N	DIO	AB4	8.66mm	32	B2B_B2_L32_N	SIO	AB11	8.12mm
33	B2B_B2_L57_P	DIO	AA4	9.84mm	34	GND	GND	-	-
35	B2B_B2_L49_N	DIO	AB6	8.66mm	36	B2B_B2_L60_P	DIO	T7	9.96mm
37	B2B_B2_L49_P	DIO	AA6	9.58mm	38	B2B_B2_L60_N	DIO	R7	11.16mm
39	2.5V	POW	-	-	40	B2B_B2_L59_N	DIO	R8	11.42mm
41	1.2V	POW	-	-	42	B2B_B2_L59_P	DIO	R9	11.36mm
43	1.2V	POW	-	-	44	GND	GND	-	-
45	B2B_B2_L48_N	DIO	AB7	9.98mm	46	B2B_B2_L44_N	DIO	Y10	11.34mm
47	B2B_B2_L48_P	DIO	Y7	10.98mm	48	B2B_B2_L44_P	DIO	W10	10.21mm
49	B2B_B2_L45_N	DIO	AB8	10.60mm	50	B2B_B2_L42_N	DIO	W11	7.52mm
51	B2B_B2_L45_P	DIO	AA8	11.053mm	52	B2B_B2_L42_P	DIO	V11	8.36mm
53	GND	GND	-	-	54	GND	GND	-	-
55	B2B_B2_L43_N	DIO	AB9	13.75mm	56	B2B_B2_L18_P	DIO	V13	7.94mm
57	B2B_B2_L43_P	DIO	Y9	12.97mm	58	B2B_B2_L18_N	DIO	W13	6.96mm
59	B2B_B2_L41_N	DIO	AB10, AB13	10.33mm	60	B2B_B2_L8_N	DIO	U16	9.92mm
61	B2B_B2_L41_P	DIO	AA10, Y13	11.01mm	62	B2B_B2_L8_P	DIO	U17	9.94mm
63	GND	GND	-	-	64	GND	GND	-	-
65	B2B_B2_L21_P	DIO	Y15	13.12mm	66	B2B_B2_L11_P	DIO	V17	8.31mm
67	B2B_B2_L21_N	DIO	AB15	12.37mm	68	B2B_B2_L11_N	DIO	W17	7.29mm
69	B2B_B2_L15_P	DIO	Y17	14.20mm	70	B2B_B2_L6_P	DIO	W18	7.40mm
71	B2B_B2_L15_N	DIO	AB17	13.77mm	72	B2B_B2_L6_N	DIO	Y18	6.94mm
73	GND	GND	-	-	74	GND	GND	-	-
75	B2B_B2_L31_N	SIO	AB12	12.30mm	76	B2B_B2_L5_P	DIO	Y19	6.18mm

Signal FPGA pin	BR3 R19	BR2 P18	BR1 N16	BR0 P17
Revision 01	1	1	1	1
Revision 02	1	1	1	0

Table 13: Board revisions pin coding

Main differences between 01 and 02 revisions:

- More powerful regulators for 1.2V and 1.5V rails
- VCCAUX separated from 2.5V power rail
- 128Mbit SPI Flash
- Additional secure 1Kbit EEPROM
- Optional B2B connection to bank 2 differential clock input

Module assembly variants coded by 4 zero ohm resistors, connected to FPGA AV[3:0] pins. All these pins should be configures to have internal PULLUP.

Signal FPGA pin	AV3 M18	AV2 M17	AV1 V20	AV0 U19	Speed grade	SDRAM	Temp grade
TE0600-02[V|B]	0	0	0	0	2	2x128MBit	C
TE0600-02[V|B]I	0	0	0	1	2	2x128MBit	I
TE0600-02[V|B]F	0	0	1	0	3	2x128MBit	C
TE0600-02[V|B]IF	0	0	1	1	3	2x128MBit	I
TE0600-02[V|B]MF	0	1	0	0	3	2x512MBit	C

Table 14: Assembly variants pin coding

7 Glossary of Abbreviations and Acronyms

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

A CAUTION notice denotes a risk. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in a fault. (undesired condition that can lead to an error) Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

API	application programming interface
B2B	board-to-board
DSP	digital signal processing; digital signal processor
EDK	Embedded Development Kit
IOB	input / output blocks; I/O blocks
IP	intellectual property
ISP	In-System Programmability
OTP	one-time programmable
PB	push button
SDK	Software Development Kit
TE	Trenz Electronic
XPS	Xilinx Platform Studio

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According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products.

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9.3 WEEE (Waste Electrical and Electronic Equipment)

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment.

Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol

consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Document Change History

ver.	date	author	description
0.01	2011-10-01	AIK	Release.
0.02	2011-10-05	AIK	Added B2B pin-out section.
0.03	2011-10-06	AIK	Reformatted pin-out tables. Added eFUSE programming section.
0.04	2011-10-06	AIK	Added board photos. Additions to eFUSE section.
0.05	2011-10-06	AIK	Removed net length information for nets which can't be measured right.
0.06	2011-10-06	AIK	Added power consumption section.
0.07	2011-10-08	AIK	Little fixes after FDR audit.
0.08	2011-10-12	AIK	Fix in eFUSE section.
0.09	2011-11-11	AIK	Added pin numbering description for B2B connectors
0.10	2012-01-20	AIK	Added pin compatibility note and manual reference.
0.11	2012-04-12	AIK	Added FPGA banks VCCIO voltages table.
1.00	2012-04-17	FDR	Updated documentation link. Replaced obsolete ElDesI and RedMine links with current GitHub links. Updated dating convention.
1.01	2012-05-18	AIK	Corrected cross-reference in section 3.2. Corrected LED description.
1.02	2012-06-18	FDR	Removed junction temperature limits under connector current ratings.
1.03	2012-07-18	AIK	Added table with B2B signals summary per FPGA bank
2.01	2012-10-30	AIK	Fork to 01 and 02 board revisions
2.01	2012-11-06	AIK	Fixed bank 1 power options
2.02	2012-11-21	AIK	Updated module diagram
2.03	2012-11-30	AIK	Added Ethernet disable note
2.04	2012-12-19	AIK	Fixed SPI Flash size on block diagram
2.05	2013-01-21	AIK	Added PHY reset note
2.06	2013-03-13	AIK	Connectors current chapter moved to separate document
2.07	2013-03-13	AIK	Changed Bank 1 power supply description and VCCIO0 sources description