Trenz Electronic GmbH - TE0600-02IVFN Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Spartan-6 LX-150
Co-Processor	-
Speed	125MHz
Flash Size	16MB
RAM Size	256MB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0600-02ivfn

Table of Contents

1 Technical Specifications

1.1 Components

- Xilinx Spartan-6 LX FPGA:
  - XC6SLX**45**-2FGG484**C** = 43 K logic cells, commercial grade
    XC6SLX**45**-2FGG484**I** = 43 K logic cells, industrial grade
  - XC6SLX**100**-2FGG484**C** = 101 K logic cells, commercial grade
    XC6SLX**100**-2FGG484**I** = 101 K logic cells, industrial grade
  - XC6SLX**150**-2FGG484**C** = 147 K logic cells, commercial grade
    XC6SLX**150**-2FGG484**I** = 147 K logic cells, industrial grade
- 10/100/1000 Gigabit Ethernet transceiver (physical layer)
  Marvell Semiconductor 88E1111
- 2 × independent 16-bit-wide (data-bus) 1 Gigabit (128 megabyte) or 4 Gigabit (512 megabyte) DDR3 SDRAM
- 128 megabit (16 megabyte) serial Flash memory with dual/quad SPI interface
- 48-bit node address chip
  Maxim Integrated Products DS2502-E48
- 1Kb Protected 1-Wire EEPROM with SHA-1 Engine

  Maxim Embedded Security Products DS2432
- 2 x fine-pitch (0.5 mm) 100-pin high-speed (up to 10.0 GHz / 20 Gbps) hermaphroditic strips
  LSHM-150-04.0-L-DV-A-S-K-TR
- Up to 52 differential FPGA input/output pins available on B2B strips
- Up to 109 single-ended (+ 1 dual-purpose) FPGA input/output pins available on B2B strips
- Ethernet (PHY), JTAG and SPI pins available on B2B strips
- 4.0 A high-efficiency DC-DC switching regulator for power rail 1.2V
- 1.5 A high-efficiency DC-DC switching regulator for power rail 1.5V
- 2 x 800 mA DC-DC linear regulator for power rails 2.5V and VCCAUX
- Processor supervisory circuits with power-fail and watchdog
  Texas Instruments TPS3705-33
- 125 MHz clock signal (system + user)
- Footprint for custom single-ended oscillator (option)
- 1 x LED (user)
- Power supply voltage: 3.3 V
- Power supply source: board-to-board interconnect (e.g. carrier board)
- Dimensions: 50 mm × 40 mm (20 cm^2)
- Minimum module height: 8 mm (without connectors)

- Maximum height on carrier board surface: ≈ 13 mm (standard connectors)
- Minimum height on carrier board surface: ≈ 5 mm (standard connectors)
- Weight: 17.2 ± 0.1 g
- Temperature grades:
- commercial (C-type FPGA device)
- industrial (I-type FPGA device)

1.2 Dimensions

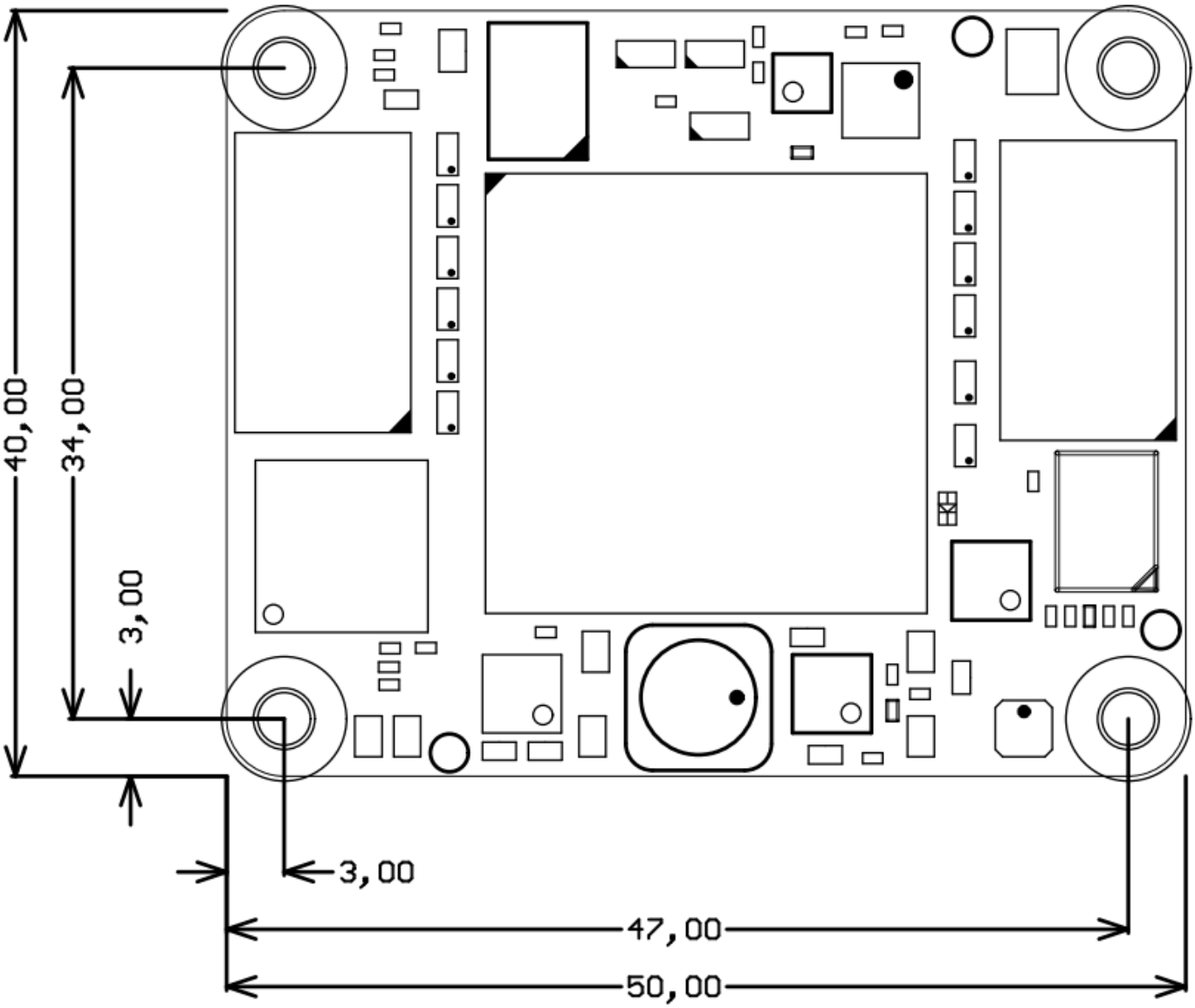

Figure 3: GigaBee board dimensions (top view)

GigaBee XC6SLX can reach a minimum vertical height of about 8 mm, if B2B

connectors are not assembled. The maximum component height on the module board on the top side is about 3.5 mm. The maximum component height on the module board on the bottom side is about 3.0 mm.

The typical minimum and maximum height from the carrier board surface, of a GigaBee XC6SLX when it mounted on a carrier board, is respectively about 5.0 mm and about 13 mm.

GigaBee XC6SLX has 4 mounting holes, one in each corner. The module can be fixed by screwing M3 screws (ISO 262) onto a carrier board through those mounting holes.

GigaBee XC6SLX weighs between 17.1 and 17.3 g with standard connectors.

1.3 Power Consumption

Power consumption of GigaBee XC6SLX modules highly depend on the FPGA design implemented. Some typical power consumptions are provided in Table 1 for the following reference systems:

- Boards – GigaBee XC6SLX 45/100/150
- Base board – TE0603-02
- Power supply – 5 V from baseboard
- Connected Gigabit Ethernet cable

FPGA type	Unconfigured	Configured with Web-server reference design
LX45	0.15 A	0.6 A
LX100	0.17 A	0.5 A
LX150	0.2 A	0.5 A

Table 1: Power consumption

2 Detailed Description

2.1 Block Diagram

Figure 4 shows a block diagram of the GigaBee XC6SLX board.

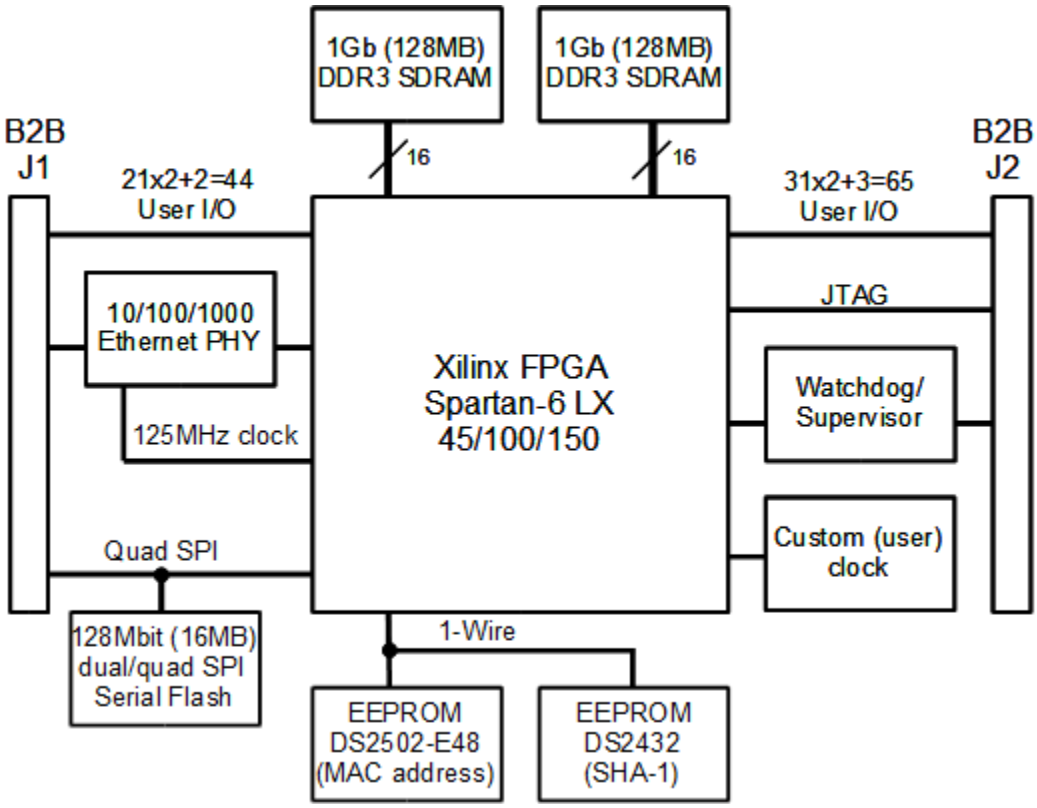

Figure 4: TE0600-02 Block Diagram

2.2 Power Supply

The nominal supply voltage of the GigaBee XC6SLX is 3.3 volt. The minimum supply voltage is 3.0 volt. The maximum supply voltage is 3.45 volt.

Supply voltages beyond the range might affect to device reliability, or even cause permanent damage of the device!

Board power supply diagram is shown in Figure 5.

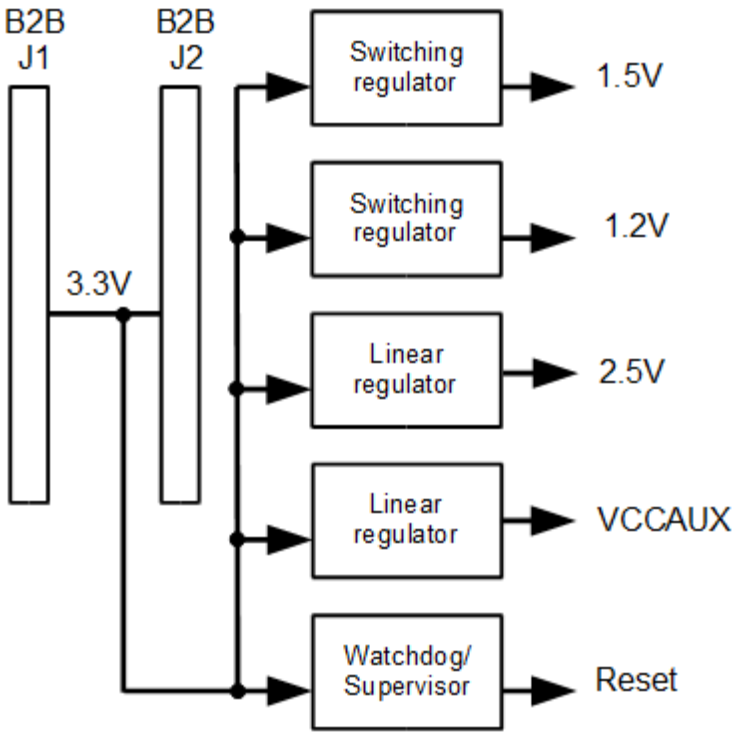

Figure 5: Power supply diagram

2.2.1 Power Supply Sources

GigaBee XC6SLX board must be powered at least in one of the following two ways:

- through B2B connector J1 (pins 1, 3, 5, 7, 9, 11, 13, 15),
- through B2B connector J2 (pins 2, 4, 6, 8, 10, 12).

We recommend to supply the module with all these 14 pins. When one or more of these pins are not power supplied, it or they can be used as power source for user applications.

Please make sure that your logic design does not draw more RMS current per pin than specified in section 2.4 Board-to-board Connectors.

2.2.2 FPGA banks VCCIO power supply

FPGA VCCIO power options shown in Table 2. Default values for configurable voltages shown in braces.

Bank	Supply voltage
B0	VCCIO 0 (3.3 V)
B1	VCCIO 1 (1.5 V)
B2	3.3 V
B3	1.5 V

Table 2: FPGA banks VCCIO power supply

Bank 0 power supply VCCIO 0 can be configured by user to 3.3 V, 2.5 V or

1.5 V, see Chapter 2.2.3.6 VCCIO0 Power Rail. Bank 1 VCCIO supply voltage is configured to 1.5 V to communicate with DDR3 SDRAM memory chip.[1]

2.2.3 On-board Power Rails

GigaBee XC6SLX has the following power rails on-board.

2.2.3.1 3.3V Power Rail

It is the main internal power rail and must be supplied from an external power source.

It supplies the other following power rails:

- 1.2V / 4 A on-board high-efficiency switching voltage regulator;
- 1.5V / 1.5 A on-board high-efficiency switching voltage regulator;
- 2.5V 0.8 A linear voltage regulator;
- VCCIO0 power rail (option) (if zero-resistor R80 is not populated and zero-resistor R79 is populated).

2.2.3.2 1.2V Power Rail

It is converted from the 3.3V rail by a switching voltage regulator and can provide up to 4.0 A to:

- FPGA V_{CCINT} power supply pins;
- Ethernet PHY;
- J1 connector.

2.2.3.3 1.5V Power Rail

It is converted from the 3.3V rail by a switching voltage regulator and can provide up to 1.5 A to:

- DDR3 SDRAM;
- Vref1 / Vref2 DDR3 SDRAM reference voltages;
- FPGA bank 3 V_{CCO};
- J1 connector.

2.2.3.4 2.5V Power Rail

It is converted from the 3.3V rail by a linear voltage regulator and can provide up to 0.8 A to:

- VCCAUX power rail;
- Ethernet physical layer;
- J1 connector;

1 By special request modules can be supplied without DDR3 SDRAM chips. Contact Trenz Electronic support for details

- J2 connector (option: if zero-resistor R80 **is** populated and zero-resistor R79 is **not** populated).

2.2.3.5 VCCAUX Power Rail

It is converted from the 3.3V rail by a linear voltage regulator and can provide up to 0.8 A to:

- FPGA auxiliary circuits;
- J2 connector.

2.2.3.6 VCCIO0 Power Rail

There are 4 options to supply this rail:

- from 3.3 V power rail (if zero-resistor R79 **is** populated[2] and R80 is **not**);
- from 2.5 V power rail (if zero-resistor R80 **is** populated and R79 is **not**);
- from 1.5 V power rail (if zero-resistors R79 and R80 are **not** populated and VCCIO0 connected to 1.5 V power rail);
- from an external power source through J2 B2B connector (pins 1, 3, 5, 7, 9) (if R79 and R80 are **not** populated)

It supplies:

- FPGA bank 0 $V_{CCO.}$

Figure 6 show simplified schematic of power options. Dashed resistors are not populated by default.

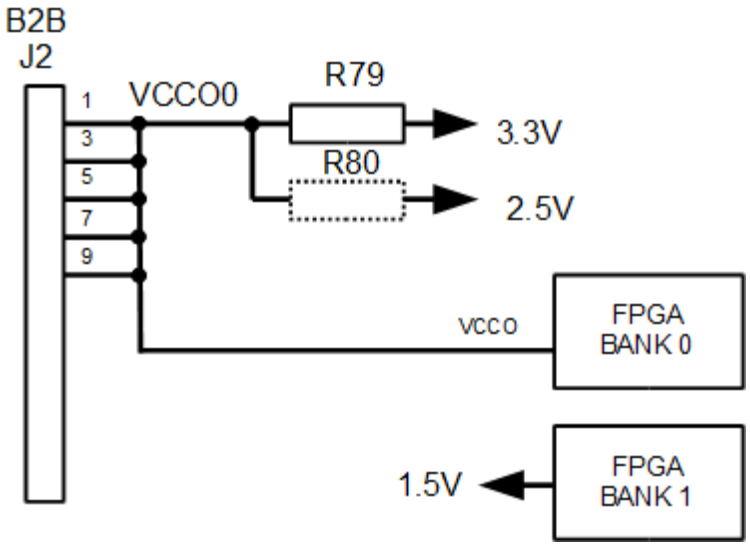

Figure 6: Power options diagram

2 Default assembling for VCCIO0 rail

Table 3 summarizes power rails information.

power-rail name	nominal voltage(V)	maximum current (A)	power source	system supply	user supply
3.3V	3.3	2.4 (3.3 option)	J1, J2	module	J1 (≤1.2 A) J2 (≤1.2 A, ≤2.1 option)
2.5V	2.5	0.8	3.3V ▸ linear	Ethernet	J1 (≤0.3 A) J2 (option)
1.5V	1.5	1.5	3.3V ▸ switch.	DDR3 SDRAM VCCO (1+3)	J1 (≤0.3 A)
1.2V	1.2	4.0	3.3V ▸ switch.	VCCINT Ethernet	J1 (≤0.6 A)
VCCAUX	2.5	0.8	3.3V ▸ linear	FPGA	J2 (≤0.3 A)
VCCCIO0	1.2, 1.5, 1.8, 2.5, 3.3	0.9	J2	VCCO (0)	J2 (≤0.9 A)

Table 3: On-board power rails summary

2.3 Power Supervision

2.3.1 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the supply rail remains below the threshold voltage (2.93 volt). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset prior to a regular system start-up. The typical delay time t_d of 200 ms starts after the supply rail has risen above the threshold voltage.

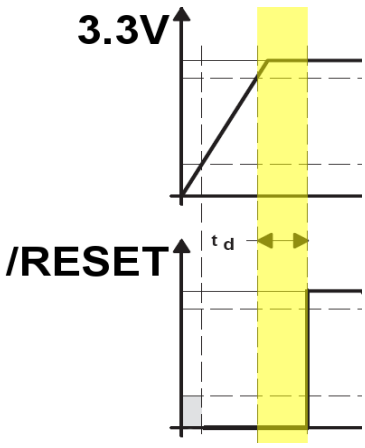

Figure 7: Reset on power-on

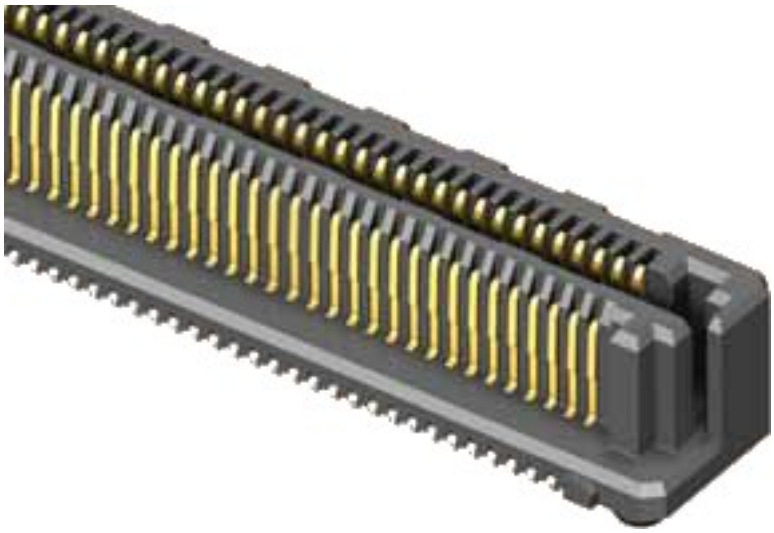

Figure 9: Samtec Razor Beam LSHM connector

The overall number of connector contacts on the GigaBee XC6SLX is 200.

Samtec Razor Beam LSHM is a high-speed interconnect system with very fine pitch (50 mil) and low profile design. Razor Beam connectors are well suited for high speed applications with performance up to 11.5 GHz (23 Gb/s) at -3 dB insertion loss. Razor Beam contacts are ideal for high speed and rugged applications featuring undercut retention notches that increase the withdrawal force and provide an audible click when the contacts engage. In addition, the self-mating (hermaphroditic) design can help reduce inventory costs. The LSHM Series features also optional shielding for EMI protection (default on GigaBee XC6SLX).

Samtec Razor Beam LSHM connectors are keyed. On the bottom side of the GigaBee XSL6, the connectors are assembled in such a way to prevent the module to be reverse mounted on carrier boards.

Samtec Razor Beam LSHM are available in different lead styles, see Table 4 for details.

lead style	A [mm]	B [mm]
-02.5	3.95	1.00
-03.0	4.45	1.50
-04.0	5.45	2.50
-06.0	7.45	4.50

Table 4: Samtec Razor Beam LSHM lead styles

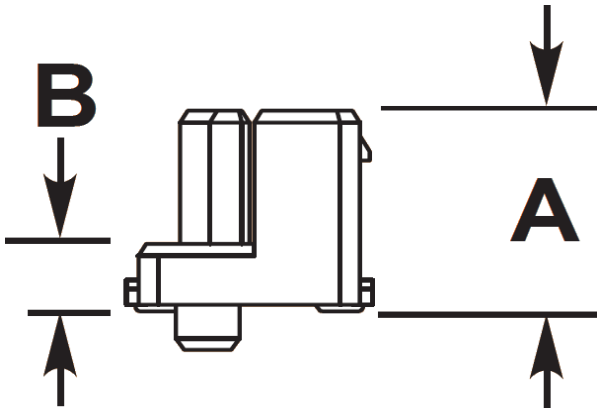

Figure 10: A and B features of Samtec Razor Beam LSHM series

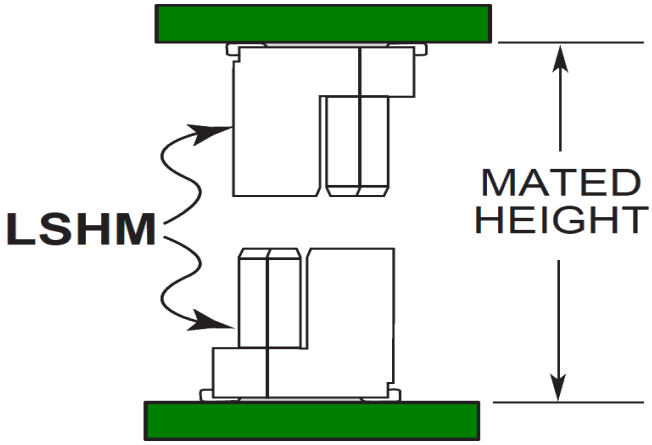

Figure 11: Definition of mated height for Samtec Razor Beam LSHM series.

The standard connector mounted on the GigaBee XC6SLX is Samtec Razor Beam LSHM-150-04.0-L-DV-A-S-K-TR (lead style: –04.0, tail option: vertical, shield option: with shield).

Trenz Electronic recommends the same part as mating connector, due to its self-mating capability.

The Samtec Razor Beam LSHM series offers a variety of mated heights form 5.0 mm to 12.0 mm. Two mated standard GigaBee XC6SLX connectors have a typical mated height of 8.0 mm. Processing conditions will affect the following heights.

standard connector lead style	mating connector lead style	mated height [mm]	min. height from carrier board [mm]	max. height on carrier board [mm]
–04.0	–02.5	6.5	≈ 3.5	≈ 11.5
–04.0	–03.0	7.0	≈ 4.0	≈ 12.0
–04.0	**–04.0**	**8.0**	**≈ 5.0**	**≈ 13.0**
–04.0	–06.0	10.0	≈ 7.0	≈ 15.0

Table 5: Samtec Razor Beam LSHM mated heights

2.7 Flash Memory

GigaBee XC6SLX board contains 128 Mb (16 MB) serial flash memory chip Winbond W25Q128BV (U11). This serial flash chip can operate as general SPI memory mode and in double or quad modes. Usage of dual and quad modes increase bandwidth up to 40 MB/s.

For more information see Winbond W25Q128BV product overview.

Flash can be programmed in several ways:

- Direct SPI programming via J1 connector.
- Indirect SPI programming via FPGA pins, controlled by JTAG.
- Direct SPI programming by FPGA, using SPI core.

Serial flash is connected to FPGA bank 2 and B2B connector J1; used pins are listed in Table 8.

Flash signal	FPGA pin	J1 pin
/CS	T5	87
CLK	Y21	91
DI(IO0)	AB20	95
DO(IO1)	AA20	93
/WP(IO2)	U14	99
/HOLD(IO3)	U13	97

Table 8: Serial flash signals connection

2.8 Ethernet

The board contains a Marvell Alaska Ethernet PHY chip (88E1111) operating at 10/100/1000 Mb/s. The board supports GMII interface mode with the FPGA. Configuration details:

- PHY address – 00111
- Advertise pause
- Auto Neg
- Advertise all caps
- Prefer slave
- Auto crossover
- 125clk - enabled
- GMII to copper
- Fiber auto-detect - disabled
- Sleep mode - disabled

Ethernet signals from PHY are connected to B2B connector J1. To use Ethernet in your design, GigaBee module should be connected to the carrier board, which have Ethernet magnetics and RJ45 connector. TE0603 carrier board can be used to access Ethernet capabilities of GigaBee XC6SLX series modules.

4.1 Pin Labelling

FPGA user signals connected to B2B connectors are characterized by the "B2B_Bx_Lyy_p" naming convention, where:

- B2B defines a "FPGA to B2B" signal type;
- Bx defines the FPGA bank (x = bank number);
- Lyy defines a differential pair or signal number (yy = pair number);
- p defines a differential signal polarity (P = positive, N = negative); single ended signals do not have this field.

Ethernet PHY signals use "PHY_name" naming conversions where "PHY" defines signal type "PHY to B2B" and "name" is PHY signal name.

Remaining signals use custom names.

4.2 Pin Numbering

Note that GigaBee XC6SLX have hermaphroditic B2B connectors. A feature of hermaphroditic connector numbering is that connected signal numbers don't match. Odd signals on module connect to even signals on baseboard. For example module signal 1 to baseboard signal 2, module signal 2 to baseboard signal 1, module signal 3 to baseboard signal 4 and so on.

4.3 Pin Types

Most pins of B2B connectors J1 and J2 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 8 different functional types of pins on the TE0600, as outlined in Table 10. In pin-out tables Table 11 and Table 12, the individual pins are colour-coded according to pin type as in Table 10.

type colour code	description
DIO[4]	Unrestricted, general-purpose differential user-I/O pin.
SIO	Unrestricted, general-purpose user-I/O pin.
CONFIG	Dedicated configuration signals.
PWRMGMT	Control and status signals for the power-saving Suspend mode.
JTAG	Dedicated JTAG signals.
GND	Dedicated ground pin. All must be connected.
TE	Trenz Electronic specific pin type. See the description of each pin in the user manual for additional information on the corresponding signals.
POW	Power signals.
SPI	SPI signals.
PHY	Ethernet PHY signals.

Table 10: TE0600 pin types

Note that some of Spartan-6 I/O types are partially compatible, so pins of compatible types can be used as inputs for signal of other type. For example pins from FPGA bank with 1.5V VCCO (IOSTANDARD = LVCMOS15) can be used as inputs for 1.2V, 1.8V, 2.5V and 3.3V signals.

See “Spartan-6 FPGA SelectIO Resources” page 38 for detailed information.

4 DIO pins can be used as SIO.

J1 pin	Net	Type	FPGA pin	Net Length	J1 pin	Net	Type	FPGA pin	Net Length
77	SUSPEND	SYS	N15	19.23mm	78	B2B_B2_L5_N	DIO	AB19	6.12mm
79	VBATT	CONFIG	R17	-	80	B2B_B2_L9_N	DIO	V18	8.43mm
81	VFS	CONFIG	P16	-	82	B2B_B2_L9_P	DIO	V19	8.36mm
83	RFUSE	CONFIG	P15	-	84	GND	GND	-	-
85	AWAKE	SYS	T19	14.15mm	86	B2B_B2_L4_N	DIO	T17	11.88mm
87	CSO_B	SPI	T5	-	88	B2B_B2_L4_P	DIO	T18	11.96mm
89	GND	GND	-	-	90	GND	GND	-	-
91	CCLK	SPI	Y21	-	92	B2B_B2_L29_N	SIO	Y12	13.58mm
93	MISO	SPI	AA20	-	94	B2B_B2_L10_N	DIO	R15	17.01mm
95	MOSI	SPI	AB20	-	96	B2B_B2_L10_P	DIO	R16	16.97mm
97	MISO3	SPI	U13	-	98	B2B_B2_L2_N	DIO	AB21	5.06mm
99	MISO2	SPI	U14	-	100	B2B_B2_L2_P	DIO	AA21	6.19mm

Table 11: J1 pin-out

4.6 J2 Pin-out

J2 pin	Net	Type	FPGA pin	Net Length	J2 pin	Net	Type	FPGA pin	Net Length
1	VCCIO0	POW	-	-	2	3.3V	POW	-	-
3	VCCIO0	POW	-	-	4	3.3V	POW	-	-
5	VCCIO0	POW	-	-	6	3.3V	POW	-	-
7	VCCIO0	POW	-	-	8	3.3V	POW	-	-
9	VCCIO0	POW	-	-	10	3.3V	POW	-	-
11	B2B_PROGB	CONFIG	-	-	12	3.3V	POW	-	-
13	HSWAPEN	CONFIG	A3	-	14	B2B_B0_L1	SIO	A4	9.017mm
15	B2B_B3_L60_N	DIO	B1	5.44mm	16	PFI	TE	-	-
17	B2B_B3_L60_P	DIO	B2	5.27mm	18	/MR	TE	-	-
19	1.5V	POW	-	-	20	GND	GND	-	-
21	B2B_B3_L9_N	DIO	T3	19.36mm	22	B2B_B0_L2_P	DIO	C5	10.17mm
23	B2B_B3_L9_P	DIO	T4	18.76mm	24	B2B_B0_L2_N	DIO	A5	9.60mm
25	B2B_B0_L3_P	DIO	D6	6.76mm	26	B2B_B0_L4_N	DIO	A6	7.65mm
27	B2B_B0_L3_N	DIO	C6	5.66mm	28	B2B_B0_L4_P	DIO	B6	8.71mm
29	GND	GND	-	-	30	GND	GND	-	-
31	B2B_B3_L59_P	DIO	J7	11.90mm	32	B2B_B0_L5_N	DIO	A7	8.59mm
33	B2B_B3_L59_N	DIO	H8	11.71mm	34	B2B_B0_L5_P	DIO	C7	9.54mm
35	B2B_B0_L32_P	DIO	D7	6.93mm	36	B2B_B0_L6_N	DIO	A8	7.42mm
37	B2B_B0_L32_N	DIO	D8	6.87mm	38	B2B_B0_L6_P	DIO	B8	8.43mm
39	GND	GND	-	-	40	GND	GND	-	-
41	B2B_B0_L7_N	DIO	C8	6.62mm	42	B2B_B0_L8_N	DIO	A9	9.28mm
43	B2B_B0_L7_P	DIO	D9	6.71mm	44	B2B_B0_L8_P	DIO	C9	9.92mm
45	B2B_B0_L33_N	DIO	C10	5.66mm	46	B2B_B0_L34_N	DIO	A10	7.58mm
47	B2B_B0_L33_P	DIO	D10	6.76mm	48	B2B_B0_L34_P	DIO	B10	8.60mm
49	GND	GND	-	-	50	GND	GND	-	-
51	B2B_B0_L36_P	DIO	D11	6.76mm	52	B2B_B0_L35_N	DIO	A11	8.89mm
53	B2B_B0_L36_N	DIO	C12	5.87mm	54	B2B_B0_L35_P	DIO	C11	9.92mm
55	B2B_B0_L49_P	DIO	D14	6.96mm	56	B2B_B0_L37_N	DIO	A12	7.52mm
57	B2B_B0_L49_N	DIO	C14	5.96mm	58	B2B_B0_L37_P	DIO	B12	8.74mm

6 Related Materials and References

The following documents provide supplementary information useful with this user manual.

6.1 Data Sheets

- Xilinx DS160: Spartan-6 Family Overview
  This overview outlines the features and product selection of the Spartan®-6 family.
  http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf
- Xilinx DS162: Spartan-6 FPGA Data Sheet: DC and Switching Characteristics
  This data sheet contains the DC and switching characteristic specifications for the Spartan®-6 family.
  http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf
- Samtec Razor Beam LSHM series overview.
  http://www.samtec.com/LSHM
- Maxim DS2502-E48 product overview.

  http://www.maxim-ic.com/datasheet/index.mvp/id/3748
- Winbond W25Q128BV product overview.

  http://www.winbond.com/hq/enu/ProductAndSales/ProductLines/FlashMemory/SerialFlash/W25Q128BV.htm
- Maxim DS2432 product page.

  http://www.maximintegrated.com/datasheet/index.mvp/id/2914

6.2 Documentation Archives

- Xilinx Spartan-6 Documentation
  http://www.xilinx.com/support/documentation/spartan-6.htm
- Xilinx Documentation
  http://www.xilinx.com/documentation/
  http://www.xilinx.com/support/documentation/
- Trenz Electronic GigaBee Series Documentation
  http://docs.trenz-electronic.de/Trenz_Electronic/products/TE0600-GigaBee_series/

6.3 User Guides

- Xilinx UG380: Spartan-6 FPGA Configuration User Guide
  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.
  http://www.xilinx.com/support/documentation/user_guides/ug380.pdf
- Xilinx UG381: Spartan-6 FPGA SelectIO Resources

http://www.xilinx.com/support/documentation/user_guides/ug381.pdf

6.4 Design and Development Tools

- Xilinx ISE Design Suite
  http://www.xilinx.com/ISE/
  http://www.xilinx.com/tools/designtools.htm
- Xilinx ISE Design Suite (version archive)
  http://www.xilinx.com/download/
  http://www.xilinx.com/support/download/
- Xilinx ISE WebPACK
  http://www.xilinx.com/tools/webpack.htm
  http://www.xilinx.com/webpack/

6.5 Design Resources

- Trenz Electronic GigaBee Design Resources
  http://www.trenz-electronic.de/download/d0/Trenz_Electronic/d1/TE0600-GigaBee_series.html
- Trenz Electronic GigaBee Reference Designs
  https://github.com/Trenz-Electronic/
  https://github.com/Trenz-Electronic/TE-EDK-IP/
  https://github.com/Trenz-Electronic/TE060X-GigaBee-Reference-Designs/

6.6 Tutorials

- Xilinx UG695: ISE In-Depth Tutorial
  Chapter 8: Configuration Using iMPACT
  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/ise_tutorial_ug695.pdf

7 Glossary of Abbreviations and Acronyms

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

A CAUTION notice denotes a risk. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in a fault. (undesired condition that can lead to an error) Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

API	application programming interface
B2B	board-to-board
DSP	digital signal processing; digital signal processor
EDK	Embedded Development Kit
IOB	input / output blocks; I/O blocks
IP	intellectual property
ISP	In-System Programmability
OTP	one-time programmable
PB	push button
SDK	Software Development Kit
TE	Trenz Electronic
XPS	Xilinx Platform Studio

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