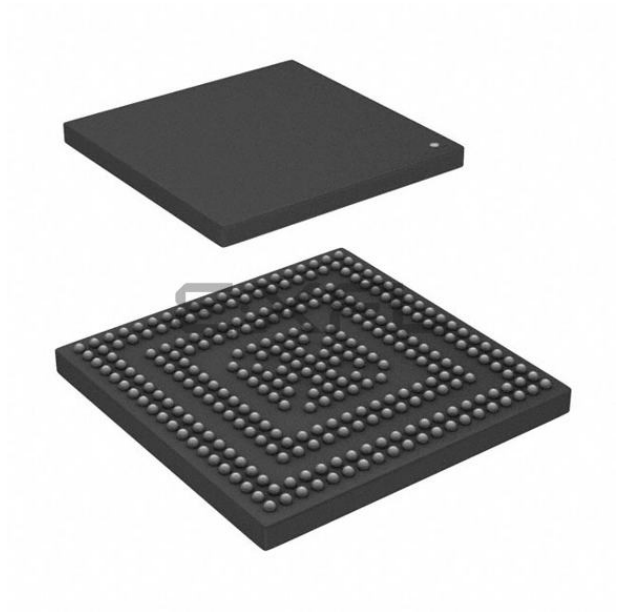
Infineon Technologies - TC1784F320F180EPBAKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	ASC, CANbus, EBI/EMI, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	91
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	176K x 8
Voltage - Supply (Vcc/Vdd)	1.235V ~ 3.47V
Data Converters	A/D 8x10b, 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	292-LFBGA
Supplier Device Package	PG-LFBGA-292-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1784f320f180epbakxuma1

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32-Bit

Microcontroller

TC1784

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.1.1 2014-05

Microcontrollers

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6)

Pin	Symbol	Ctrl.	Type	Function
Port 0				
E12	P0.0	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 0**
	IN0	I		**GPTA0 Input 0**
	IN0	I		**LTCA2 Input 0**
	HWCFG0	I		**Hardware Configuration Input 0**
	OUT0	O1		**GPTA0 Output 0**
	OUT56	O2		**GPTA0 Output 56**
	OUT0	O3		**LTCA2 Output 0**
D12	P0.1	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 1**
	IN1	I		**GPTA0 Input 1**
	IN1	I		**LTCA2 Input 1**
	SDI1	I		**MSC0 Serial Data Input 1**
	HWCFG1	I		**Hardware Configuration Input 1**
	OUT1	O1		**GPTA0 Output 1**
	OUT57	O2		**GPTA0 Output 57**
	OUT1	O3		**LTCA2 Output 1**
D11	P0.2	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 2**
	IN2	I		**GPTA0 Input 2**
	IN2	I		**LTCA2 Input 2**
	HWCFG2	I		**Hardware Configuration Input 2**
	OUT2	O1		**GPTA0 Output 2**
	OUT58	O2		**GPTA0 Output 58**
	OUT2	O3		**LTCA2 Output 2**
E11	P0.3	I/O0	A1+/ PU	**Port 0 General Purpose I/O Line 3**
	IN3	I		**GPTA0 Input 3**
	IN3	I		**LTCA2 Input 3**
	HWCFG3	I		**Hardware Configuration Input 3**
	OUT3	O1		**GPTA0 Output 3**
	OUT59	O2		**GPTA0 Output 59**
	OUT3	O3		**LTCA2 Output 3**

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
E9	P0.4	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 4**
	IN4	I		**GPTA0 Input 4**
	IN4	I		**LTCA2 Input 4**
	HWCFG4	I		**Hardware Configuration Input 4**
	OUT4	O1		**GPTA0 Output 4**
	OUT60	O2		**GPTA0 Output 60**
	OUT4	O3		**LTCA2 Output 4**
E8	P0.5	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 5**
	IN5	I		**GPTA0 Input 5**
	IN5	I		**LTCA2 Input 5**
	HWCFG5	I		**Hardware Configuration Input 5**
	OUT5	O1		**GPTA0 Output 5**
	OUT61	O2		**GPTA0 Output 61**
	OUT5	O3		**LTCA2 Output 5**
D8	P0.6	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 6**
	IN6	I		**GPTA0 Input 6**
	IN6	I		**LTCA2 Input 6**
	HWCFG6	I		**Hardware Configuration Input 6**
	REQ2	I		**External Request Input 2**
	OUT6	O1		**GPTA0 Output 6**
	OUT62	O2		**GPTA0 Output 62**
	OUT6	O3		**LTCA2 Output 6**
E7	P0.7	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 7**
	IN7	I		**GPTA0 Input 7**
	IN7	I		**LTCA2 Input 7**
	HWCFG7	I		**Hardware Configuration Input 7**
	REQ3	I		**External Request Input 3**
	OUT7	O1		**GPTA0 Output 7**
	OUT63	O2		**GPTA0 Output 63**
	OUT7	O3		**LTCA2 Output 7**

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
M16	P1.2	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 2**
	IN18	I		**GPTA0 Input 18**
	OUT18	O1		**GPTA0 Output 18**
	OUT74	O2		**GPTA0 Output 74**
	OUT18	O3		**LTCA2 Output 18**
K16	P1.3	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 3**
	IN19	I		**GPTA0 Input 19**
	IN19	I		**LTCA2 Input 19**
	OUT19	O1		**GPTA0 Output 19**
	OUT75	O2		**GPTA0 Output 75**
	OUT19	O3		**LTCA2 Output 19**
J16	P1.4	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 4**
	IN20	I		**GPTA0 Input 20**
	IN20	I		**LTCA2 Input 20**
	EMGSTOP	I		**Emergency Stop Input**
	OUT20	O1		**GPTA0 Output 20**
	OUT76	O2		**GPTA0 Output 76**
	OUT20	O3		**LTCA2 Output 20**
H16	P1.5	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 35**
	IN21	I		**GPTA0 Input 21**
	IN21	I		**LTCA2 Input 21**
	OUT21	O1		**GPTA0 Output 21**
	OUT77	O2		**GPTA0 Output 77**
	OUT21	O3		**LTCA2 Output 21**
G16	P1.6	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 6**
	IN22	I		**GPTA0 Input 22**
	IN22	I		**LTCA2 Input 22**
	OUT22	O1		**GPTA0 Output 22**
	OUT78	O2		**GPTA0 Output 78**
	OUT22	O3		**LTCA2 Output 22**

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L20	P1.11	I/O0	A1+/ PU	**Port 1 General Purpose I/O Line 11**
	IN27	I		**GPTA0 Input 27**
	IN51	I		**GPTA0 Input 51**
	SCLK1B	I		**SSC1 Clock Input B**
	OUT27	O1		**GPTA0 Output 27**
	OUT51	O2		**GPTA0 Output 51**
	SCLK1B	O3		**SSC1 Clock Output B**
T10	P1.12	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 12**
	IN16	I		**LTCA2 Input 16**
	AD0EMUX0	O1		**ADC0 External Multiplexer Control Output 0**
	AD0EMUX0	O2		**ADC0 External Multiplexer Control Output 0**
	OUT16	O3		**LTCA2 Output 16**
U10	P1.13	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 13**
	IN17	I		**LTCA2 Input 17**
	AD0EMUX1	O1		**ADC0 External Multiplexer Control Output 1**
	AD0EMUX1	O2		**ADC0 External Multiplexer Control Output 1**
	OUT17	O3		**LTCA2 Output 17**
U9	P1.14	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 14**
	IN18	I		**LTCA2 Input 18**
	AD0EMUX2	O1		**ADC0 External Multiplexer Control Output 2**
	AD0EMUX2	O2		**ADC0 External Multiplexer Control Output 2**
	OUT18	O3		**LTCA2 Output 18**
F16	P1.15	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 15**
	$\overline{\text{BRKIN}}$	I		**OCDS Break Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	$\overline{\text{BRKOUT}}$	O		**OCDS Break Output**

Port 2

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B15	P3.12	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 12**
	RXDCAN0	I		**CAN Node 0 Receiver Input**
	RXD0B	I		**ASC0 Receiver Input B**
	RXD0B	O1		**ASC0 Receiver Output B (Synchronous Mode)**
	RXD0B	O2		**ASC0 Receiver Output B (Synchronous Mode)**
	OUT94	O3		**GPTA0 Output 94**
A15	P3.13	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 13**
	TXDCAN0	O1		**CAN Node 0 Transmitter Output**
	TXD0	O2		**ASC0 Transmit Output**
	OUT95	O3		**GPTA0 Output 95**
B16	P3.14	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 14**
	RXDCAN1	I		**CAN Node 1 Receiver Input**
	RXD1B	I		**ASC1 Receiver Input B**
	SDI2	I		**MSC0 Serial Data Input 2**
	RXD1B	O1		**ASC1 Receiver Output B (Synchronous Mode)**
	RXD1B	O2		**ASC1 Receiver Output B (Synchronous Mode)**
	OUT96	O3		**GPTA0 Output 96**
A16	P3.15	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 15**
	TXDCAN1	O1		**CAN Node 1 Transmitter Output**
	TXD1	O2		**ASC1 Transmit Output**
	OUT97	O3		**GPTA0 Output 97**
Port 4				
T13	P4.0	I/O0	A1+/ PU	**Port 4 General Purpose I/O Line 0**
	IN28	I		**GPTA0 Input 28**
	IN52	I		**GPTA0 Input 52**
	RXDCAN2	I		**CAN Node 2 Receiver Input**
	OUT28	O1		**GPTA0 Output 28**
	OUT28	O1		**GPTA0 Output 28**
	OUT52	O2		**GPTA0 Output 52**

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
E2	P5.1	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 1**
	IN41	I		**GPTA0 Input 41**
	IN27	I		**LTCA2 Input 27**
	OUT41	O1		**GPTA0 Output 41**
	OUT9	O2		**LTCA2 Output 9**
	SLSO21	O3		**SSC2 Slave Select Output 1**
F4	P5.2	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 2**
	IN42	I		**GPTA0 Input 42**
	IN28	I		**LTCA2 Input 28**
	OUT42	O1		**GPTA0 Output 42**
	OUT10	O2		**LTCA2 Output 10**
	SLSO22	O3		**SSC2 Slave Select Output 2**
G5	P5.3	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 3**
	IN43	I		**GPTA0 Input 43**
	OUT43	O1		**GPTA0 Output 43**
	OUT11	O2		**LTCA2 Output 11**
	SLSO23	O3		**SSC2 Slave Select Output 3**
H5	P5.4	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 4**
	IN44	I		**GPTA0 Input 44**
	IN29	I		**LTCA2 Input 29**
	$\overline{\text{SLSI2A}}$	I		**SSC2 Slave Select Input A**
	OUT44	O1		**GPTA0 Output 44**
	OUT12	O2		**LTCA2 Output 12**
	SLSO24	O3		**SSC2 Slave Select Output 4**

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L7, L8, L9, L10, L11, L12, L13, L14	V_{SS}	-	-	**Digital Ground**
M7, M8, M10, M11, M13, M14	V_{SS}	-	-	**Digital Ground**
N9, N10, N11, N12	V_{SS}	-	-	**Digital Ground (cont´d)**
P9, P10, P11, P12	V_{SS}	-	-	**Digital Ground (cont´d)**
T16, U17, W19, Y20	V_{SS}	-	-	**Digital Ground (cont´d)**
K19	V_{DDOSC}	-	-	**Main Oscillator and PLL Power Supply (1.3V)**
H20	V_{DDOSC3}	-	-	**Main Oscillator Power Supply (3.3V)**
K17	V_{DDPF}	-	-	**Flexray Oscillator and PLL Power Supply (1.3V)**
J17	V_{DDPF3}	-	-	**Flexray Oscillator Power Supply (3.3V)**
K20	V_{SSOSC}	-	-	**Main Oscillator and PLL Ground**
D13, D14	V_{DDFL3}	-	-	**Power Supply for Flash (3.3V)**
J20	XTAL1	I		**Oscillator/PLL/Clock Generator Input**
J19	XTAL2	O		**Oscillator/PLL/Clock Generator Output**

A1 = Pad class A1 (LVTTL)
A1+ = Pad class A1+ (LVTTL)
A2 = Pad class A2 (LVTTL)
F = Pad class F (LVDS/CMOS)
D = Pad class D (ADC)
I = Pad class I (LVTTL)

PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
TR = tri-state during reset ($\overline{\text{PORST}}$ = 0)

Table 9 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Absolute sum of short circuit currents per pin group	ΣI_{SC_PG} CC	–	–	20	mA	
Ambient Temperature	T_A SR	-40	–	125	°C	
Junction temperature	T_J SR	-40	–	150	°C	
Core Supply Voltage	V_{DD} SR	1.235	1.3	1.365[2)]	V	
Flash supply voltage 3.3V	V_{DDFL3} SR	3.13	3.3	3.47[4)]	V	
ADC analog supply voltage	V_{DDM} SR	3.13	3.3	5.5[3)]	V	
Oscillator core supply voltage	V_{DDOSC} SR	1.235	1.3	1.365[2)]	V	
Oscillator 3.3V supply voltage	V_{DDOSC3} SR	3.05	3.3	3.47[4)]	V	
E-Ray PLL core supply voltage	V_{DDPF} SR	1.235	1.3	1.365[2)]	V	
E-Ray PLL 3.3V supply voltage	V_{DDPF3} SR	3.05	3.3	3.47[4)]	V	
Digital supply voltage for IO pads	V_{DDP} SR	3.13	3.3	3.47 [4)]	V	
VDDP voltage to ensure defined pad states[5)]	V_{DDPPA} CC	0.65	–	–	V	
Digital ground voltage	V_{SS} SR	0	–	–	V	
Analog ground voltage for V_{DDM}	V_{SSM} SR	-0.1	0	0.1	V	
Analog core supply	V_{DDAF} SR	1.235	1.3	1.365[2)]	V	
FADC / ADC analog supply voltage	V_{DDMF} SR	3.13	3.3	3.47[4)]	V	
Analog ground voltage for V_{DDMF}	V_{SSAF} SR	-0.1	0	0.1	V	

1) Applicable for digital outputs.

Table 12 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1	t_{RA1} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage class A1 pads	V_{IHA1} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+0.3,3.6)$	V	
Input low voltage class A1 pads	V_{ILA1} SR	-0.3	–	0.36 x V_{DDP}	V	

Table 12 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A1 pads	V_{OHA1} CC	V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= medium
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= medium
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -400 µA; pin out driver= weak
		2.4	–	–	V	I_{OH}≥ -500 µA; pin out driver= weak
Output voltage low class A1 pads	V_{OLA1} CC	–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= medium
		–	–	0.4	V	I_{OL}≤ 500 µA; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Table 13 Standard_Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A1+ pads [1]	*HYSA1* + CC	0.1 x V_{DDP}	–	–	V	
Input Leakage Current Class A1+	I_{OZA1+} CC	-1000	–	1000	nA	
On-Resistance of the class A1+ pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	I_{OH}> -0.5 mA; P_MOS
		–	210	340	Ohm	I_{OL}< 0.5 mA; N_MOS

Table 13 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A1+ pads	$V_{OHA1+CC}$	V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= medium
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= strong
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= medium
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= strong
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -400 µA; pin out driver= weak
		2.4	–	–	V	I_{OH}≥ -500 µA; pin out driver= weak
Output voltage low class A1+ pads	$V_{OLA1+CC}$	–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= medium
		–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= strong
		–	–	0.4	V	I_{OL}≤ 500 µA; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

5.3.5 ERAY Phase Locked Loop (ERAY_PLL)

Table 26 PLL_ERAY Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated jitter at SYSCLK pin	D_{PP} CC	-0.8	–	0.8	ns	
Accumulated_Jitter	D_P CC	-0.5	–	0.5	ns	
PLL Base Frequency of the ERAY PLL	$f_{PLLBASE\_ERAY}$ CC	50	250	360	MHz	
VCO input frequency of the ERAY PLL	f_{REF} CC	20	–	40	MHz	
VCO frequency range of the ERAY PLL	f_{VCO_ERAY} CC	450	–	500	MHz	
PLL lock-in time	t_L CC	5.6	–	200	µs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDPF3} and V_{SSOSC}, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.
These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

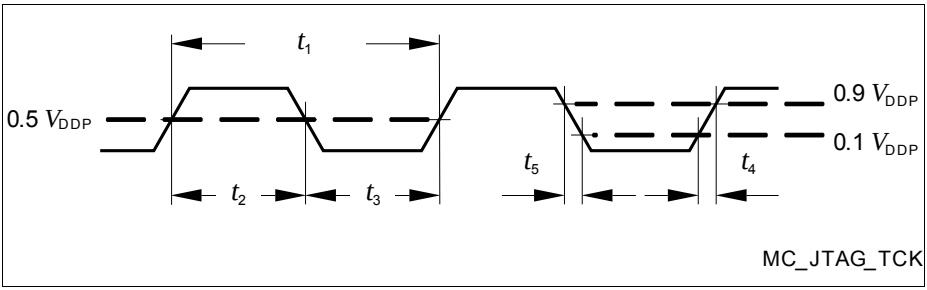

Figure 10 Test Clock Timing (TCK)

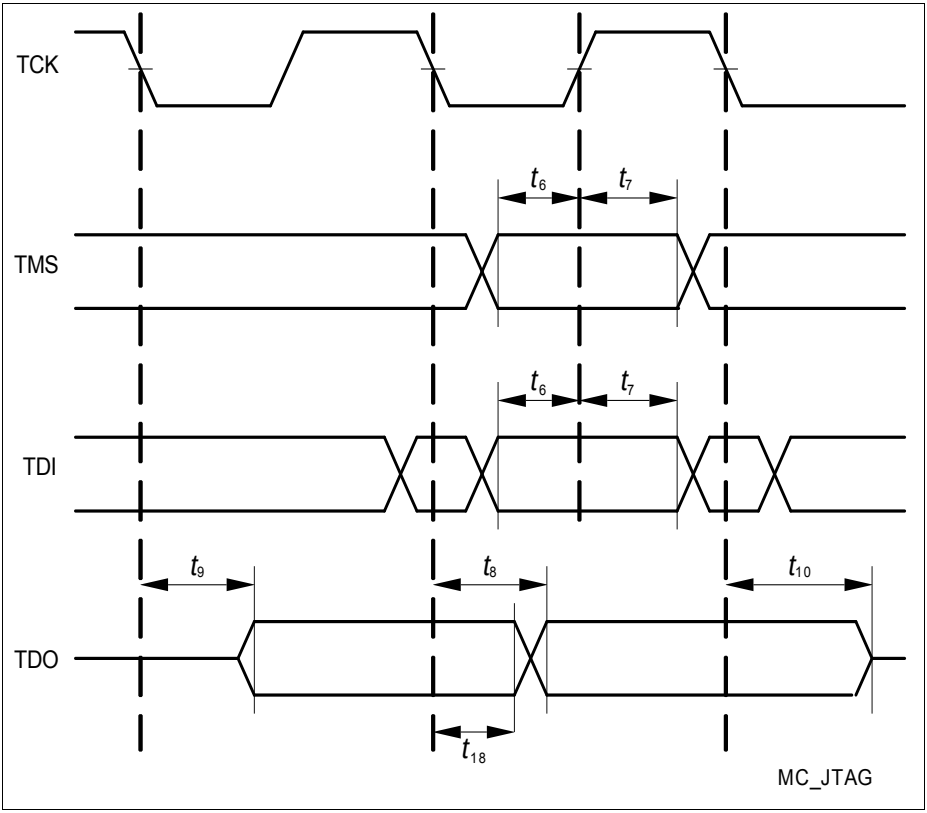

Figure 11 JTAG Timing

Table 30 MLI Transmitter (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK fall time	t_{14} CC	–	–	0.3 x t_{10} 3)	ns	
TDATA/TVALID output delay time	t_{15} CC	-3	–	4.4	ns	
TREADY setup time before TCLK rising edge	t_{16} SR	18	–	–	ns	
TREADY hold time after TCLK rising edge	t_{17} SR	-2	–	–	ns	

1) The following formula is valid: t11 + t12 = t10.

2) The min./max. TCLK low/high times t11/t12 include the PLL jitter of fSYS. Fractional divider settings must be regarded additionally to t11 / t12.

3) For high-speed MLI interface, strong driver sharp or medium edge selection (class A2 pad) is recommended for TCLK.

5.3.8.2 Micro Second Channel (MSC) Interface Timing

The MSC parameters are vaild for C_L = 50 pF.

Table 31 MSC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLP clock period[1)2)]	t_{40} CC	2 x T_{MSC} 3)	–	–	ns	
SOP[4)]/ENx outputs delay from FCLP[4)] rising edge	t_{45} CC	-2	–	5	ns	ENx with strong driver and sharp (minus) edge
		-2	–	10	ns	ENx with strong driver and medium (minus) edge
		0	–	21	ns	ENx with strong driver and soft edge

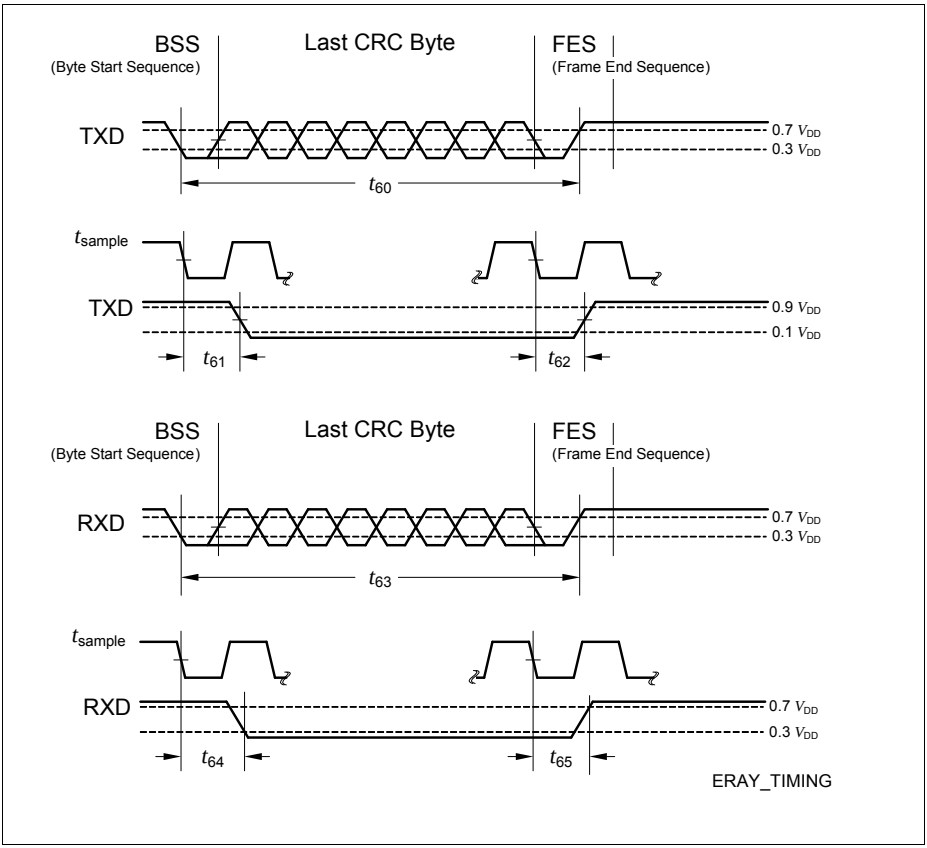

Figure 19 ERAY Timing

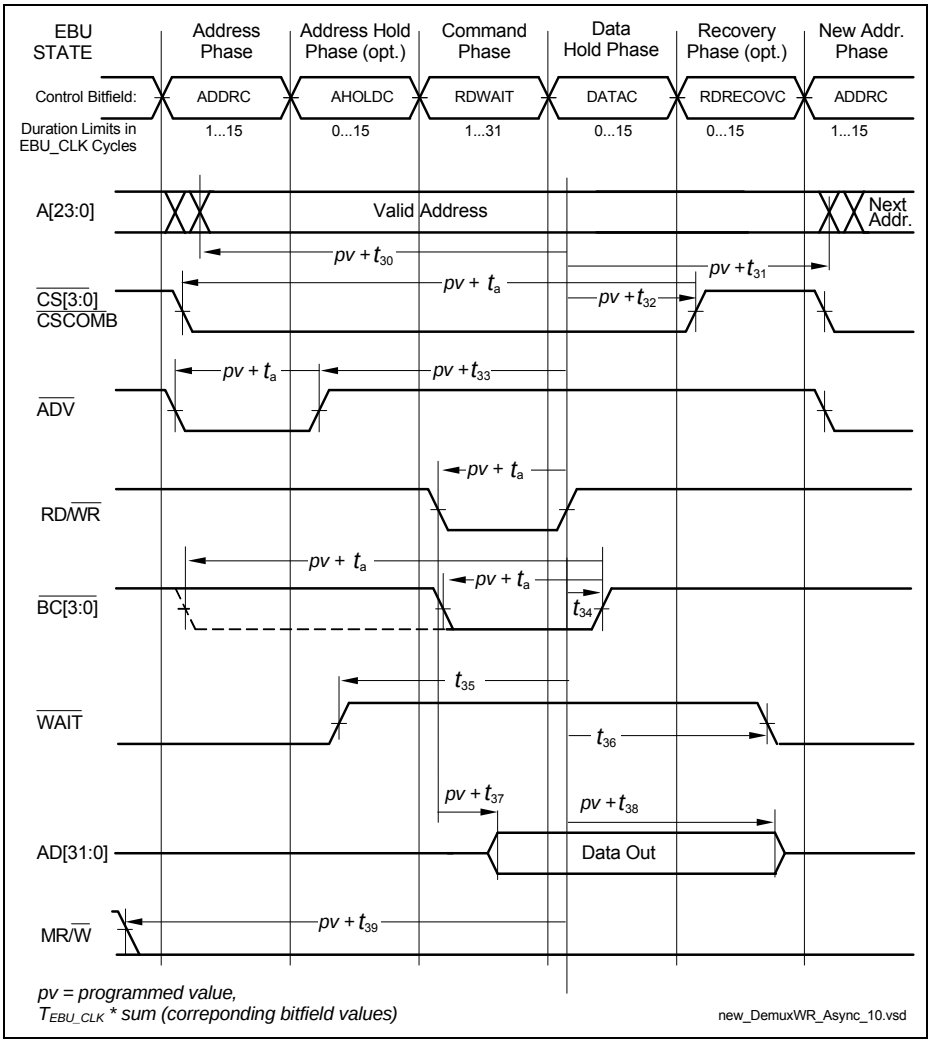

Figure 23 Demultiplexed Write Access

5.4.2 Package Outline

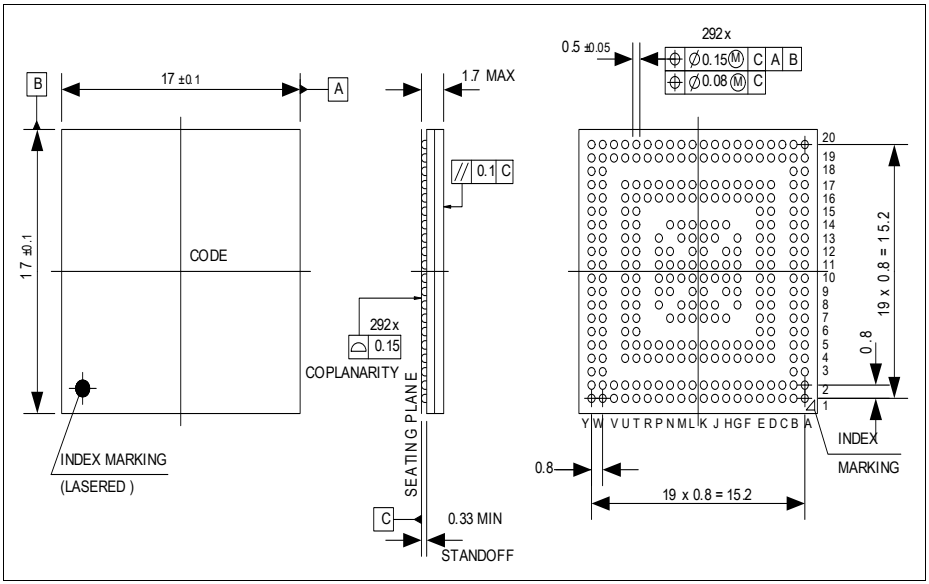

Figure 24 Package Outlines PG-LFBGA-292-6

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: ***http://www.infineon.com/products***.

5.4.3 Flash Memory Parameters

The data retention time of the TC1784’s Flash memory depends on the number of times the Flash memory has been erased and programmed.

Table 38 FLASH32 Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Sector	t_{ERD} CC	–	–	3[1)]	s	
Program Flash Erase Time per 256 KByte Sector	t_{ERP} CC	–	–	5	s	