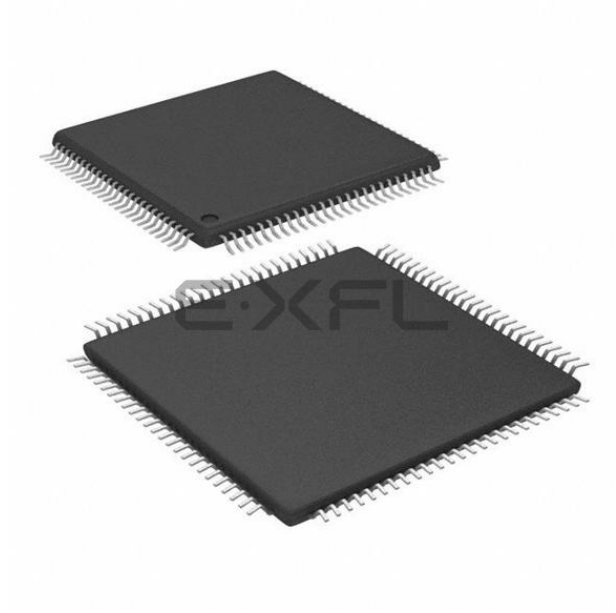
# Microchip Technology - PIC24FJ192GB110T-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, LVD, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 192KB (65.5K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24fj192gb110t-i-pt |

**TABLE 1-4: PIC24FJ256GB110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)**

| Function | Pin Number | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-Pin TQFP, QFN | 80-Pin TQFP | 100-Pin TQFP | | | |
| D+ | 37 | 47 | 57 | I/O | — | USB Differential Plus line (internal transceiver). |
| D- | 36 | 46 | 56 | I/O | — | USB Differential Minus line (internal transceiver). |
| DMH | 46 | 58 | 72 | O | — | D- External Pull-up Control Output. |
| DMLN | 42 | 54 | 68 | O | — | D- External Pull-down Control Output. |
| DPH | 50 | 62 | 77 | O | — | D+ External Pull-up Control Output. |
| DPLN | 43 | 55 | 69 | O | — | D+ External Pull-down Control Output. |
| ENVREG | 57 | 71 | 86 | I | ST | Voltage Regulator Enable. |
| INT0 | 46 | 58 | 72 | I | ST | External Interrupt Input. |
| $\overline{\text{MCLR}}$ | 7 | 9 | 13 | I | ST | Master Clear (device Reset) Input. This line is brought low to cause a Reset. |
| OSCI | 39 | 49 | 63 | I | ANA | Main Oscillator Input Connection. |
| OSCO | 40 | 50 | 64 | O | ANA | Main Oscillator Output Connection. |
| PGEC1 | 15 | 19 | 24 | I/O | ST | In-Circuit Debugger/Emulator/ICSP™ Programming Clock. |
| PGED1 | 16 | 20 | 25 | I/O | ST | In-Circuit Debugger/Emulator/ICSP Programming Data. |
| PGEC2 | 17 | 21 | 26 | I/O | ST | In-Circuit Debugger/Emulator/ICSP Programming Clock. |
| PGED2 | 18 | 22 | 27 | I/O | ST | In-Circuit Debugger/Emulator/ICSP Programming Data. |
| PGEC3 | 11 | 15 | 20 | I/O | ST | In-Circuit Debugger/Emulator/ICSP Programming Clock. |
| PGED3 | 12 | 16 | 21 | I/O | ST | In-Circuit Debugger/Emulator/ICSP Programming Data. |
| PMA0 | 30 | 36 | 44 | I/O | ST | Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes). |
| PMA1 | 29 | 35 | 43 | I/O | ST | Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes). |
| PMA2 | 8 | 10 | 14 | O | — | Parallel Master Port Address (Demultiplexed Master modes). |
| PMA3 | 6 | 8 | 12 | O | — | |
| PMA4 | 5 | 7 | 11 | O | — | |
| PMA5 | 4 | 6 | 10 | O | — | |
| PMA6 | 16 | 24 | 29 | O | — | |
| PMA7 | 22 | 23 | 28 | O | — | |
| PMA8 | 32 | 40 | 50 | O | — | |
| PMA9 | 31 | 39 | 49 | O | — | |
| PMA10 | 28 | 34 | 42 | O | — | |
| PMA11 | 27 | 33 | 41 | O | — | |
| PMA12 | 24 | 30 | 35 | O | — | |
| PMA13 | 23 | 29 | 34 | O | — | |
| PMCS1 | 45 | 57 | 71 | I/O | ST/TTL | Parallel Master Port Chip Select 1 Strobe/Address Bit 15. |
| PMCS2 | 44 | 56 | 70 | O | ST | Parallel Master Port Chip Select 2 Strobe/Address Bit 14. |
| PMBE | 51 | 63 | 78 | O | — | Parallel Master Port Byte Enable Strobe. |

**Legend:** TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
$I^2C$™ = $I^2C$/SMBus input buffer

## 2.7 Configuration of Analog and Digital Pins During ICSP Operations

If an ICSP compliant emulator is selected as a debugger, it automatically initializes all of the A/D input pins (ANx) as “digital” pins. Depending on the particular device, this is done by setting all bits in the ADnPCFG register(s), or clearing all bit in the ANSx registers.

All PIC24F devices will have either one or more ADnPCFG registers or several ANSx registers (one for each port); no device will have both. Refer to **Section 22.0 “10-Bit High-Speed A/D Converter”** for more specific information.

The bits in these registers that correspond to the A/D pins that initialized the emulator must not be changed by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain A/D pins as analog input pins during the debug session, the user application must modify the appropriate bits during initialization of the ADC module, as follows:

- For devices with an ADnPCFG register, clear the bits corresponding to the pin(s) to be configured as analog. Do not change any other bits, particularly those corresponding to the PGECx/PGEDx pair, at any time.
- For devices with ANSx registers, set the bits corresponding to the pin(s) to be configured as analog. Do not change any other bits, particularly those corresponding to the PGECx/PGEDx pair, at any time.

When a Microchip debugger/emulator is used as a programmer, the user application firmware must correctly configure the ADnPCFG or ANSx registers. Automatic initialization of this register is only done during debugger operation. Failure to correctly configure the register(s) will result in all A/D pins being recognized as analog input pins, resulting in the port value being read as a logic '0', which may affect user application functionality.

## 2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to $V_{SS}$ on unused pins and drive the output to logic low.

### 4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® devices and improve data space memory usage efficiency, the PIC24F instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word which contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register which matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed; if it occurred on a write, the instruction will be executed but the write will not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the Least Significant Byte. The Most Significant Byte is not modified.

A sign-extend instruction (SE) is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSB of any W register by executing a zero-extend (ZE) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions operate only on words.

### 4.2.3 NEAR DATA SPACE

The 8-Kbyte area between 0000h and 1FFFh is referred to as the near data space. Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. The remainder of the data space is addressable indirectly. Additionally, the whole data space is addressable using MOV instructions, which support Memory Direct Addressing with a 16-bit address field.

### 4.2.4 SFR SPACE

The first 2 Kbytes of the near data space, from 0000h to 07FFh, are primarily occupied with Special Function Registers (SFRs). These are used by the PIC24F core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'. A diagram of the SFR space, showing where SFRs are actually implemented, is shown in Table 4-2. Each implemented area indicates a 32-byte region where at least one address is implemented as an SFR. A complete listing of implemented SFRs, including their addresses, is shown in Tables 4-3 through 4-30.

**TABLE 4-2: IMPLEMENTED REGIONS OF SFR DATA SPACE**

| | SFR Space Address | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **xx00** | **xx20** | **xx40** | **xx60** | **xx80** | **xxA0** | **xxC0** | **xxE0** |
| **000h** | Core | | | ICN | Interrupts | | | — |
| **100h** | Timers | | Capture | | Compare | | | |
| **200h** | I²C™ | UART | SPI/UART | SPI/I²C | SPI | UART | I/O | |
| **300h** | A/D | A/D/CTMU | — | — | — | — | — | — |
| **400h** | — | — | — | — | USB | | | — |
| **500h** | — | — | — | — | — | — | — | — |
| **600h** | PMP | RTC/Comp | CRC | — | PPS | | | — |
| **700h** | — | — | System | NVM/PMD | — | — | — | — |

**Legend:** — = No implemented SFRs in this block

**TABLE 4-3: CPU CORE REGISTERS MAP**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WREG0 | 0000 | Working Register 0 | | | | | | | | | | | | | | | | 0000 |
| WREG1 | 0002 | Working Register 1 | | | | | | | | | | | | | | | | 0000 |
| WREG2 | 0004 | Working Register 2 | | | | | | | | | | | | | | | | 0000 |
| WREG3 | 0006 | Working Register 3 | | | | | | | | | | | | | | | | 0000 |
| WREG4 | 0008 | Working Register 4 | | | | | | | | | | | | | | | | 0000 |
| WREG5 | 000A | Working Register 5 | | | | | | | | | | | | | | | | 0000 |
| WREG6 | 000C | Working Register 6 | | | | | | | | | | | | | | | | 0000 |
| WREG7 | 000E | Working Register 7 | | | | | | | | | | | | | | | | 0000 |
| WREG8 | 0010 | Working Register 8 | | | | | | | | | | | | | | | | 0000 |
| WREG9 | 0012 | Working Register 9 | | | | | | | | | | | | | | | | 0000 |
| WREG10 | 0014 | Working Register 10 | | | | | | | | | | | | | | | | 0000 |
| WREG11 | 0016 | Working Register 11 | | | | | | | | | | | | | | | | 0000 |
| WREG12 | 0018 | Working Register 12 | | | | | | | | | | | | | | | | 0000 |
| WREG13 | 001A | Working Register 13 | | | | | | | | | | | | | | | | 0000 |
| WREG14 | 001C | Working Register 14 | | | | | | | | | | | | | | | | 0000 |
| WREG15 | 001E | Working Register 15 | | | | | | | | | | | | | | | | 0800 |
| SPLIM | 0020 | Stack Pointer Limit Value Register | | | | | | | | | | | | | | | | xxxx |
| PCL | 002E | Program Counter Low Word Register | | | | | | | | | | | | | | | | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | Program Counter Register High Byte | | | | | | | | 0000 |
| TBLPAG | 0032 | — | — | — | — | — | — | — | — | Table Memory Page Address Register | | | | | | | | 0000 |
| PSVPAG | 0034 | — | — | — | — | — | — | — | — | Program Space Visibility Page Address Register | | | | | | | | 0000 |
| RCOUNT | 0036 | Repeat Loop Counter Register | | | | | | | | | | | | | | | | xxxx |
| SR | 0042 | — | — | — | — | — | — | — | DC | IPL2 | IPL1 | IPL0 | RA | N | OV | Z | C | 0000 |
| CORCON | 0044 | — | — | — | — | — | — | — | — | — | — | — | — | IPL3 | PSV | — | — | 0000 |
| DISICNT | 0052 | — | — | Disable Interrupts Counter Register | | | | | | | | | | | | | | xxxx |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 7-2: IMPLEMENTED INTERRUPT VECTORS**

| Interrupt Source | Vector Number | IVT Address | AIVT Address | Interrupt Bit Locations | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| ADC1 Conversion Done | 13 | 00002Eh | 00012Eh | IFS0<13> | IEC0<13> | IPC3<6:4> |
| Comparator Event | 18 | 000038h | 000138h | IFS1<2> | IEC1<2> | IPC4<10:8> |
| CRC Generator | 67 | 00009Ah | 00019Ah | IFS4<3> | IEC4<3> | IPC16<14:12> |
| CTMU Event | 77 | 0000AEh | 0001AEh | IFS4<13> | IEC4<13> | IPC19<6:4> |
| External Interrupt 0 | 0 | 000014h | 000114h | IFS0<0> | IEC0<0> | IPC0<2:0> |
| External Interrupt 1 | 20 | 00003Ch | 00013Ch | IFS1<4> | IEC1<4> | IPC5<2:0> |
| External Interrupt 2 | 29 | 00004Eh | 00014Eh | IFS1<13> | IEC1<13> | IPC7<6:4> |
| External Interrupt 3 | 53 | 00007Eh | 00017Eh | IFS3<5> | IEC3<5> | IPC13<6:4> |
| External Interrupt 4 | 54 | 000080h | 000180h | IFS3<6> | IEC3<6> | IPC13<10:8> |
| I2C1 Master Event | 17 | 000036h | 000136h | IFS1<1> | IEC1<1> | IPC4<6:4> |
| I2C1 Slave Event | 16 | 000034h | 000134h | IFS1<0> | IEC1<0> | IPC4<2:0> |
| I2C2 Master Event | 50 | 000078h | 000178h | IFS3<2> | IEC3<2> | IPC12<10:8> |
| I2C2 Slave Event | 49 | 000076h | 000176h | IFS3<1> | IEC3<1> | IPC12<6:4> |
| I2C3 Master Event | 85 | 0000BEh | 0001BEh | IFS5<5> | IEC5<5> | IPC21<6:4> |
| I2C3 Slave Event | 84 | 0000BCh | 0001BCh | IFS5<4> | IEC5<4> | IPC21<2:0> |
| Input Capture 1 | 1 | 000016h | 000116h | IFS0<1> | IEC0<1> | IPC0<6:4> |
| Input Capture 2 | 5 | 00001Eh | 00011Eh | IFS0<5> | IEC0<5> | IPC1<6:4> |
| Input Capture 3 | 37 | 00005Eh | 00015Eh | IFS2<5> | IEC2<5> | IPC9<6:4> |
| Input Capture 4 | 38 | 000060h | 000160h | IFS2<6> | IEC2<6> | IPC9<10:8> |
| Input Capture 5 | 39 | 000062h | 000162h | IFS2<7> | IEC2<7> | IPC9<14:12> |
| Input Capture 6 | 40 | 000064h | 000164h | IFS2<8> | IEC2<8> | IPC10<2:0> |
| Input Capture 7 | 22 | 000040h | 000140h | IFS1<6> | IEC1<6> | IPC5<10:8> |
| Input Capture 8 | 23 | 000042h | 000142h | IFS1<7> | IEC1<7> | IPC5<14:12> |
| Input Capture 9 | 93 | 0000CEh | 0001CEh | IFS5<13> | IEC5<13> | IPC23<6:4> |
| Input Change Notification | 19 | 00003Ah | 00013Ah | IFS1<3> | IEC1<3> | IPC4<14:12> |
| LVD Low-Voltage Detect | 72 | 0000A4h | 0001A4h | IFS4<8> | IEC4<8> | IPC18<2:0> |
| Output Compare 1 | 2 | 000018h | 000118h | IFS0<2> | IEC0<2> | IPC0<10:8> |
| Output Compare 2 | 6 | 000020h | 000120h | IFS0<6> | IEC0<6> | IPC1<10:8> |
| Output Compare 3 | 25 | 000046h | 000146h | IFS1<9> | IEC1<9> | IPC6<6:4> |
| Output Compare 4 | 26 | 000048h | 000148h | IFS1<10> | IEC1<10> | IPC6<10:8> |
| Output Compare 5 | 41 | 000066h | 000166h | IFS2<9> | IEC2<9> | IPC10<6:4> |
| Output Compare 6 | 42 | 000068h | 000168h | IFS2<10> | IEC2<10> | IPC10<10:8> |
| Output Compare 7 | 43 | 00006Ah | 00016Ah | IFS2<11> | IEC2<11> | IPC10<14:12> |
| Output Compare 8 | 44 | 00006Ch | 00016Ch | IFS2<12> | IEC2<12> | IPC11<2:0> |
| Output Compare 9 | 92 | 0000CCh | 0001CCh | IFS5<12> | IEC5<12> | IPC23<2:0> |
| Parallel Master Port | 45 | 00006Eh | 00016Eh | IFS2<13> | IEC2<13> | IPC11<6:4> |
| Real-Time Clock/Calendar | 62 | 000090h | 000190h | IFS3<14> | IEC3<14> | IPC15<10:8> |
| SPI1 Error | 9 | 000026h | 000126h | IFS0<9> | IEC0<9> | IPC2<6:4> |
| SPI1 Event | 10 | 000028h | 000128h | IFS0<10> | IEC0<10> | IPC2<10:8> |
| SPI2 Error | 32 | 000054h | 000154h | IFS2<0> | IEC2<0> | IPC8<2:0> |
| SPI2 Event | 33 | 000056h | 000156h | IFS2<1> | IEC2<1> | IPC8<6:4> |
| SPI3 Error | 90 | 0000C8h | 0001C8h | IFS5<10> | IEC5<10> | IPC22<10:8> |
| SPI3 Event | 91 | 0000CAh | 0001CAh | IFS5<11> | IEC5<11> | IPC22<14:12> |

**REGISTER 7-22: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC8IP2 | IC8IP1 | IC8IP0 | — | IC7IP2 | IC7IP1 | IC7IP0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | INT1IP2 | INT1IP1 | INT1IP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **IC8IP<2:0>:** Input Capture Channel 8 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **IC7IP<2:0>:** Input Capture Channel 7 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2-0 **INT1IP<2:0>:** External Interrupt 1 Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

**REGISTER 7-28: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | PMPIP2 | PMPIP1 | PMPIP0 | — | OC8IP2 | OC8IP1 | OC8IP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **PMPIP<2:0>:** Parallel Master Port Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **OC8IP<2:0>:** Output Compare Channel 8 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

## 7.4 Interrupt Setup Procedures

### 7.4.1 INITIALIZATION

To configure an interrupt source:

1. Set the NSTDIS Control bit (INTCON1<15>) if nested interrupts are not desired.
2. Select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bits for all enabled interrupt sources may be programmed to the same non-zero value.

| **Note:** | At a device Reset, the IPCx registers are initialized, such that all user interrupt sources are assigned to priority level 4. |
|---|---|

3. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
4. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

### 7.4.2 INTERRUPT SERVICE ROUTINE

The method that is used to declare an ISR and initialize the IVT with the correct vector address will depend on the programming language (i.e., 'C' or assembler) and the language development toolsuite that is used to develop the application. In general, the user must clear the interrupt flag in the appropriate IFSx register for the source of the interrupt that the ISR handles. Otherwise, the ISR will be re-entered immediately after exiting the routine. If the ISR is coded in assembly language, it must be terminated using a `RETFIE` instruction to unstack the saved PC value, SRL value and old CPU priority level.

### 7.4.3 TRAP SERVICE ROUTINE

A Trap Service Routine (TSR) is coded like an ISR, except that the appropriate trap status flag in the INTCON1 register must be cleared to avoid re-entry into the TSR.

### 7.4.4 INTERRUPT DISABLE

All user interrupts can be disabled using the following procedure:

1. Push the current SR value onto the software stack using the `PUSH` instruction.
2. Force the CPU to priority level 7 by inclusive ORing the value E0h with SRL.

To enable user interrupts, the `POP` instruction may be used to restore the previous SR value.

Note that only user interrupts with a priority level of 7 or less can be disabled. Trap sources (level 8-15) cannot be disabled.

The `DISI` instruction provides a convenient way to disable interrupts of priority levels 1-6 for a fixed period of time. Level 7 interrupt sources are not disabled by the `DISI` instruction.

## 15.0 SERIAL PERIPHERAL INTERFACE (SPI)

| | |
|---|---|
| **Note:** | This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **Section 23. "Serial Peripheral Interface (SPI)"** (DS39699). |

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D Converters, etc. The SPI module is compatible with Motorola's SPI and SIOP interfaces. All devices of the PIC24FJ256GB110 family include three SPI modules

The module supports operation in two buffer modes. In Standard mode, data is shifted through a single serial buffer. In Enhanced Buffer mode, data is shifted through an 8-level FIFO buffer.

| | |
|---|---|
| **Note:** | Do not perform read-modify-write operations (such as bit-oriented instructions) on the SPIxBUF register in either Standard or Enhanced Buffer mode. |

The module also supports a basic framed SPI protocol while operating in either Master or Slave mode. A total of four framed SPI configurations are supported.

The SPI serial interface consists of four pins:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{SS}$x: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPI module can be configured to operate using 2, 3 or 4 pins. In the 3-pin mode, $\overline{SS}$x is not used. In the 2-pin mode, both SDOx and $\overline{SS}$x are not used.

Block diagrams of the module in Standard and Enhanced modes are shown in Figure 15-1 and Figure 15-2.

| | |
|---|---|
| **Note:** | In this section, the SPI modules are referred to together as SPIx or separately as SPI1, SPI2 or SPI3. Special Function Registers will follow a similar notation. For example, SPIxCON1 and SPIxCON2 refer to the control registers for any of the 3 SPI modules. |

## 17.1 UART Baud Rate Generator (BRG)

The UART module includes a dedicated 16-bit Baud Rate Generator. The UxBRG register controls the period of a free-running, 16-bit timer. Equation 17-1 shows the formula for computation of the baud rate with BRGH = 0.

**EQUATION 17-1: UART BAUD RATE WITH BRGH = 0(1,2)**

$$\text{Baud Rate} = \frac{F_{CY}}{16 \bullet (\text{UxBRG} + 1)}$$

$$\text{UxBRG} = \frac{F_{CY}}{16 \bullet \text{Baud Rate}} - 1$$

**Note 1:** FCY denotes the instruction cycle clock frequency (FOSC/2).

**2:** Based on FCY = FOSC/2, Doze mode and PLL are disabled.

Example 17-1 shows the calculation of the baud rate error for the following conditions:

- FCY = 4 MHz
- Desired Baud Rate = 9600

The maximum baud rate (BRGH = 0) possible is FCY/16 (for UxBRG = 0) and the minimum baud rate possible is FCY/(16 * 65536).

Equation 17-2 shows the formula for computation of the baud rate with BRGH = 1.

**EQUATION 17-2: UART BAUD RATE WITH BRGH = 1(1,2)**

$$\text{Baud Rate} = \frac{F_{CY}}{4 \bullet (\text{UxBRG} + 1)}$$

$$\text{UxBRG} = \frac{F_{CY}}{4 \bullet \text{Baud Rate}} - 1$$

**Note 1:** FCY denotes the instruction cycle clock frequency.

**2:** Based on FCY = FOSC/2, Doze mode and PLL are disabled.

The maximum baud rate (BRGH = 1) possible is FCY/4 (for UxBRG = 0) and the minimum baud rate possible is FCY/(4 * 65536).

Writing a new value to the UxBRG register causes the BRG timer to be reset (cleared). This ensures the BRG does not wait for a timer overflow before generating the new baud rate.

**EXAMPLE 17-1: BAUD RATE ERROR CALCULATION (BRGH = 0)(1)**

Desired Baud Rate = FCY/(16 (UxBRG + 1))

Solving for UxBRG value:

UxBRG = ((FCY/Desired Baud Rate)/16) – 1
UxBRG = ((4000000/9600)/16) – 1
UxBRG = 25

Calculated Baud Rate= 4000000/(16 (25 + 1))
= 9615

Error = (Calculated Baud Rate – Desired Baud Rate) / Desired Baud Rate
= (9615 – 9600)/9600
= 0.16%

**Note 1:** Based on FCY = FOSC/2, Doze mode and PLL are disabled.

**REGISTER 18-4: U1OTGCON: USB ON-THE-GO CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DPPULUP | DMPULUP | DPPULDWN(1) | DMPULDWN(1) | VBUSON(1) | OTGEN(1) | VBUSCHG(1) | VBUSDIS(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit
1 = D+ data line pull-up resistor enabled
0 = D+ data line pull-up resistor disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit
1 = D- data line pull-up resistor enabled
0 = D- data line pull-up resistor disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit(1)
1 = D+ data line pull-down resistor enabled
0 = D+ data line pull-down resistor disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit(1)
1 = D- data line pull-down resistor enabled
0 = D- data line pull-down resistor disabled

bit 3 **VBUSON:** VBUS Power-on bit(1)
1 = VBUS line powered
0 = VBUS line not powered

bit 2 **OTGEN:** OTG Features Enable bit(1)
1 = USB OTG enabled; all D+/D- pull-ups and pull-downs bits are enabled
0 = USB OTG disabled; D+/D- pull-ups and pull-downs are controlled in hardware by the settings of the HOSTEN and USBEN bits (U1CON<3,0>)

bit 1 **VBUSCHG:** VBUS Charge Select bit(1)
1 = VBUS line set to charge to 3.3V
0 = VBUS line set to charge to 5V

bit 0 **VBUSDIS:** VBUS Discharge Enable bit(1)
1 = VBUS line discharged through a resistor
0 = VBUS line not discharged

**Note 1:** These bits are only used in Host mode; do not use in Device mode.

**REGISTER 18-5: U1PWRC: USB POWER CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0, HS | U-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0, HC | R/W-0 |
|---|---|---|---|---|---|---|---|
| UACTPND | — | — | USLPGRD | — | — | USUSPND | USBPWR |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | HC = Hardware Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
1 = Module should not be suspended at the moment (requires USLPGRD bit to be set)
0 = Module may be suspended or powered down

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** Sleep/Suspend Guard bit
1 = Indicate to the USB module that it is about to be suspended or powered down
0 = No suspend

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **USUSPND:** USB Suspend Mode Enable bit
1 = USB OTG module is in Suspend mode; USB clock is gated and the transceiver is placed in a low-power state
0 = Normal USB OTG operation

bit 0 **USBPWR:** USB Operation Enable bit
1 = USB OTG module is enabled
0 = USB OTG module is disabled(1)

**Note 1:** Do not clear this bit unless the HOSTEN, USBEN and OTGEN bits (U1CON<3,0> and U1OTGCON<2>) are all cleared.

**REGISTER 18-16: U1IR: USB INTERRUPT STATUS REGISTER (DEVICE MODE ONLY)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/K-0, HS | U-0 | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R-0 | R/K-0, HS |
|---|---|---|---|---|---|---|---|
| STALLIF | — | RESUMEIF | IDLEIF | TRNIF | SOFIF | UERRIF | URSTIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | K = Write '1' to clear bit | HS = Hardware Settable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
- 1 = A STALL handshake was sent by the peripheral during the handshake phase of the transaction in Device mode
- 0 = A STALL handshake has not been sent

bit 6 **Unimplemented:** Read as '0'

bit 5 **RESUMEIF:** Resume Interrupt bit
- 1 = A K-state is observed on the D+ or D- pin for 2.5 μs (differential '1' for low speed, differential '0' for full speed)
- 0 = No K-state observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
- 1 = Idle condition detected (constant Idle state of 3 ms or more)
- 0 = No Idle condition detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit
- 1 = Processing of current token is complete; read U1STAT register for endpoint information
- 0 = Processing of current token not complete; clear U1STAT register or load next token from STAT (clearing this bit causes the STAT FIFO to advance)

bit 2 **SOFIF:** Start-Of-Frame Token Interrupt bit
- 1 = A Start-Of-Frame token received by the peripheral or the Start-Of-Frame threshold reached by the host
- 0 = No Start-Of-Frame token received or threshold reached

bit 1 **UERRIF**: USB Error Condition Interrupt bit (read-only)
- 1 = An unmasked error condition has occurred; only error states enabled in the U1EIE register can set this bit
- 0 = No unmasked error condition has occurred

bit 0 **URSTIF:** USB Reset Interrupt bit
- 1 = Valid USB Reset has occurred for at least 2.5 μs; Reset state must be cleared before this bit can be reasserted
- 0 = No USB Reset has occurred. Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits at the moment of the write to become cleared.

**Note:** Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits at the moment of the write to become cleared.

**NOTES:**

**REGISTER 19-1: PMCON: PARALLEL PORT CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0(1) | R/W-0(1) | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PMPEN | — | PSIDL | ADRMUX1 | ADRMUX0 | PTBEEN | PTWREN | PTRDEN |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0(1) | R/W-0(1) | R/W-0(1) | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSF1 | CSF0 | ALP | CS2P | CS1P | BEP | WRSP | RDSP |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PMPEN:** Parallel Master Port Enable bit
1 = PMP enabled
0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **PSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits(1)
11 = Reserved
10 = All 16 bits of address are multiplexed on PMD<7:0> pins
01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper 3 bits are multiplexed on PMA<10:8>
00 = Address and data appear on separate pins

bit 10 **PTBEEN:** Byte Enable Port Enable bit (16-Bit Master mode)
1 = PMBE port enabled
0 = PMBE port disabled

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port enabled
0 = PMWR/PMENB port disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/$\overline{\text{PMWR}}$ port enabled
0 = PMRD/$\overline{\text{PMWR}}$ port disabled

bit 7-6 **CSF1:CSF0:** Chip Select Function bits
11 = Reserved
10 = PMCS1 and PMCS2 function as chip select
01 = PMCS2 functions as chip select, PMCS1 functions as address bit 14
00 = PMCS1 and PMCS2 function as address bits 15 and 14

bit 5 **ALP:** Address Latch Polarity bit(1)
1 = Active-high ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)
0 = Active-low (PMALL and PMALH)

bit 4 **CS2P:** Chip Select 2 Polarity bit(1)
1 = Active-high ($\overline{\text{PMCS2}}$/PMCS2)
0 = Active-low (PMCS2/$\overline{\text{PMCS2}}$)

bit 3 **CS1P:** Chip Select 1 Polarity bit(1)
1 = Active-high ($\overline{\text{PMCS1}}$/PMCS1)
0 = Active-low (PMCS1/$\overline{\text{PMCS1}}$)

**Note 1:** These bits have no effect when their corresponding pins are used as address lines.

## 26.5 JTAG Interface

PIC24FJ256GB110 family devices implement a JTAG interface, which supports boundary scan device testing.

## 26.6 In-Circuit Serial Programming

PIC24FJ256GB110 family microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock (PGECx) and data (PGEDx) and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

## 26.7 In-Circuit Debugger

When MPLAB® ICD 2 is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pins.

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{\text{MCLR}}$, $V_{DD}$, $V_{SS}$ and the PGECx/PGEDx pin pair designated by the ICS Configuration bits. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

**TABLE 29-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(1)** | **Max** | **Units** | **Conditions** | | |
| **Idle Current (IIDLE)(2)** | | | | | | |
| DC40 | 220 | 310 | μA | -40°C | 2.0V(3) | 1 MIPS |
| DC40a | 220 | 310 | μA | +25°C | | |
| DC40b | 220 | 310 | μA | +85°C | | |
| DC40d | 300 | 390 | μA | -40°C | 3.3V(4) | |
| DC40e | 300 | 390 | μA | +25°C | | |
| DC40f | 300 | 420 | μA | +85°C | | |
| DC43 | 0.85 | 1.1 | mA | -40°C | 2.0V(3) | 4 MIPS |
| DC43a | 0.85 | 1.1 | mA | +25°C | | |
| DC43b | 0.87 | 1.2 | mA | +85°C | | |
| DC43d | 1.1 | 1.4 | mA | -40°C | 3.3V(4) | |
| DC43e | 1.1 | 1.4 | mA | +25°C | | |
| DC43f | 1.1 | 1.4 | mA | +85°C | | |
| DC47 | 4.4 | 5.6 | mA | -40°C | 2.5V(3) | 16 MIPS |
| DC47a | 4.4 | 5.6 | mA | +25°C | | |
| DC47b | 4.4 | 5.6 | mA | +85°C | | |
| DC47c | 4.4 | 5.6 | mA | -40°C | 3.3V(4) | |
| DC47d | 4.4 | 5.6 | mA | +25°C | | |
| DC47e | 4.4 | 5.6 | mA | +85°C | | |
| DC50 | 1.1 | 1.4 | mA | -40°C | 2.0V(3) | FRC (4 MIPS) |
| DC50a | 1.1 | 1.4 | mA | +25°C | | |
| DC50b | 1.1 | 1.4 | mA | +85°C | | |
| DC50d | 1.4 | 1.8 | mA | -40°C | 3.3V(4) | |
| DC50e | 1.4 | 1.8 | mA | +25°C | | |
| DC50f | 1.4 | 1.8 | mA | +85°C | | |
| DC51 | 4.3 | 13 | μA | -40°C | 2.0V(3) | LPRC (31 kHz) |
| DC51a | 4.5 | 13 | μA | +25°C | | |
| DC51b | 10 | 32 | μA | +85°C | | |
| DC51d | 44 | 77 | μA | -40°C | 3.3V(4) | |
| DC51e | 44 | 77 | μA | +25°C | | |
| DC51f | 70 | 132 | μA | +85°C | | |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** Base IIDLE current is measured with the core off, OSCI driven with external square wave from rail to rail. All I/O pins are configured as inputs and pulled to VDD. $\overline{MCLR}$ = VDD; WDT and FSCM are disabled. No peripheral modules are operating and all of the Peripheral Module Disable (PMD) bits are set.

**3:** On-chip voltage regulator disabled (ENVREG tied to VSS).

**4:** On-chip voltage regulator enabled (ENVREG tied to VDD). Low-Voltage Detect (LVD) and Brown-out Detect (BOD) are enabled.

**TABLE 29-7: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage(4)** | | | | | |
| DI10 | | I/O Pins with ST Buffer | VSS | — | 0.2 VDD | V | |
| DI11 | | I/O Pins with TTL Buffer | VSS | — | 0.15 VDD | V | |
| DI15 | | $\overline{MCLR}$ | VSS | — | 0.2 VDD | V | |
| DI16 | | OSC1 (XT mode) | VSS | — | 0.2 VDD | V | |
| DI17 | | OSC1 (HS mode) | VSS | — | 0.2 VDD | V | |
| DI18 | | I/O Pins with I2C™ Buffer: | VSS | — | 0.3 VDD | V | |
| DI19 | | I/O Pins with SMBus Buffer: | VSS | — | 0.8 | V | SMBus enabled |
| | VIH | **Input High Voltage(4)** | | | | | |
| DI20 | | I/O Pins with ST Buffer:<br>with Analog Functions,<br>Digital Only | <br>0.8 VDD<br>0.8 VDD | <br>—<br>— | <br>VDD<br>5.5 | <br>V<br>V | |
| DI21 | | I/O Pins with TTL Buffer:<br>with Analog Functions,<br>Digital Only | <br>0.25 VDD + 0.8<br>0.25 VDD + 0.8 | <br>—<br>— | <br>VDD<br>5.5 | <br>V<br>V | |
| DI25 | | $\overline{MCLR}$ | 0.8 VDD | — | VDD | V | |
| DI26 | | OSC1 (XT mode) | 0.7 VDD | — | VDD | V | |
| DI27 | | OSC1 (HS mode) | 0.7 VDD | — | VDD | V | |
| DI28 | | I/O Pins with I2C Buffer:<br>with Analog Functions,<br>Digital Only | <br>0.7 VDD<br>0.7 VDD | <br>—<br>— | <br>VDD<br>5.5 | <br>V<br>V | |
| DI29 | | I/O Pins with SMBus Buffer:<br>with Analog Functions,<br>Digital Only | <br>2.1<br>2.1 | | <br>VDD<br>5.5 | <br>V<br>V | 2.5V ≤ VPIN ≤ VDD |
| DI30 | ICNPU | **CNxx Pull-up Current** | 50 | 250 | 400 | μA | VDD = 3.3V, VPIN = VSS |
| DI30A | ICNPD | **CNxx Pull-Down Current** | — | 80 | — | μA | VDD = 3.3V, VPIN = VDD |
| | IIL | **Input Leakage Current(2,3)** | | | | | |
| DI50 | | I/O Ports | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD,<br>Pin at high-impedance |
| DI51 | | Analog Input Pins | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD,<br>Pin at high-impedance |
| DI52 | | USB Differential Pins<br>(D+, D-) | — | — | ±1 | μA | VUSB ≥ VDD |
| DI55 | | $\overline{MCLR}$ | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD |
| DI56 | | OSC1 | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD,<br>XT and HS modes |

**Note 1:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

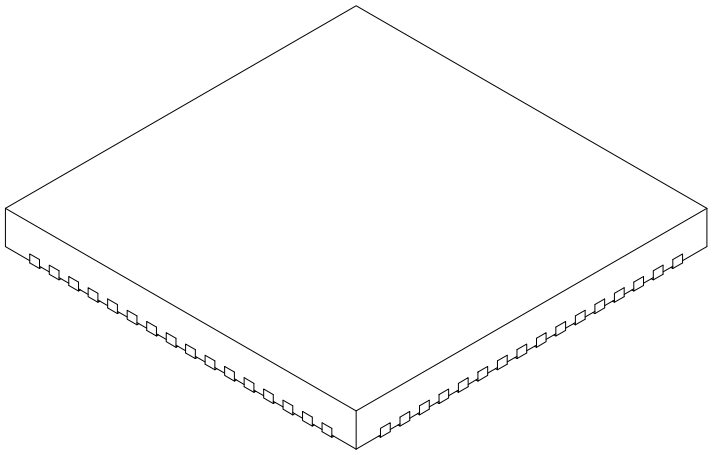
**2:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** Refer to Table 1-4 for I/O pins buffer types.

## 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 64 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 9.00 BSC | |
| Exposed Pad Width | E2 | 7.05 | 7.15 | 7.50 |
| Overall Length | D | | 9.00 BSC | |
| Exposed Pad Length | D2 | 7.05 | 7.15 | 7.50 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149B Sheet 2 of 2

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