



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	8.38MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	DMA, PSM, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/analog-devices/aduc841bcpz62-3">https://www.e-xfl.com/product-detail/analog-devices/aduc841bcpz62-3</a>

<sup>1</sup> Temperature Range  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

<sup>2</sup> ADC linearity is guaranteed during normal MicroConverter core operation.

<sup>3</sup> ADC LSB size =  $V_{\text{REF}}/2^{12}$ , that is, for internal  $V_{\text{REF}} = 2.5\text{ V}$ , 1 LSB = 610  $\mu\text{V}$ , and for external  $V_{\text{REF}} = 1\text{ V}$ , 1 LSB = 244  $\mu\text{V}$ .

<sup>4</sup> These numbers are not production tested but are supported by design and/or characterization data on production release.

<sup>5</sup> Offset and gain error and offset and gain error match are measured after factory calibration.

<sup>6</sup> Based on external ADC system components, the user may need to execute a system calibration to remove additional external channel errors to achieve these specifications.

<sup>7</sup> SNR calculation includes distortion and noise components.

<sup>8</sup> Channel-to-channel crosstalk is measured on adjacent channels.

<sup>9</sup> The temperature monitor gives a measure of the die temperature directly; air temperature can be inferred from this result.

<sup>10</sup> DAC linearity is calculated using:

Reduced code range of 100 to 4095, 0 V to  $V_{\text{REF}}$  range.

Reduced code range of 100 to 3945, 0 V to  $V_{\text{DD}}$  range.

DAC output load = 10 k $\Omega$  and 100 pF.

<sup>11</sup> DAC differential nonlinearity specified on 0 V to  $V_{\text{REF}}$  and 0 V to  $V_{\text{DD}}$  ranges.

<sup>12</sup> DAC specification for output impedance in the unbuffered case depends on DAC code.

<sup>13</sup> DAC specifications for  $I_{\text{SINK}}$ , voltage output settling time, and digital-to-analog glitch energy depend on external buffer implementation in unbuffered mode. DAC in unbuffered mode tested with OP270 external buffer, which has a low input leakage current.

<sup>14</sup> Measured with  $C_{\text{REF}}$  pin decoupled with 0.47  $\mu\text{F}$  capacitor to ground. Power-up time for the internal reference is determined by the value of the decoupling capacitor chosen for the  $C_{\text{REF}}$  pin.

<sup>15</sup> When using an external reference device, the internal band gap reference input can be bypassed by setting the ADCCON1.6 bit.

<sup>16</sup> Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and the Flash/EE data memory.

<sup>17</sup> Endurance is qualified to 100,000 cycles as per JEDEC Std. 22 method A117 and measured at  $-40^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+85^{\circ}\text{C}$ . Typical endurance at  $25^{\circ}\text{C}$  is 700,000 cycles.

<sup>18</sup> Retention lifetime equivalent at junction temperature ( $T_j$ ) =  $55^{\circ}\text{C}$  as per JEDEC Std. 22 method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature as shown in Figure 38 in the Flash/EE Memory Reliability section.

<sup>19</sup> Power supply current consumption is measured in normal, idle, and power-down modes under the following conditions:

Normal Mode: Reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON (ADuC842/ADuC843), core executing internal software loop.

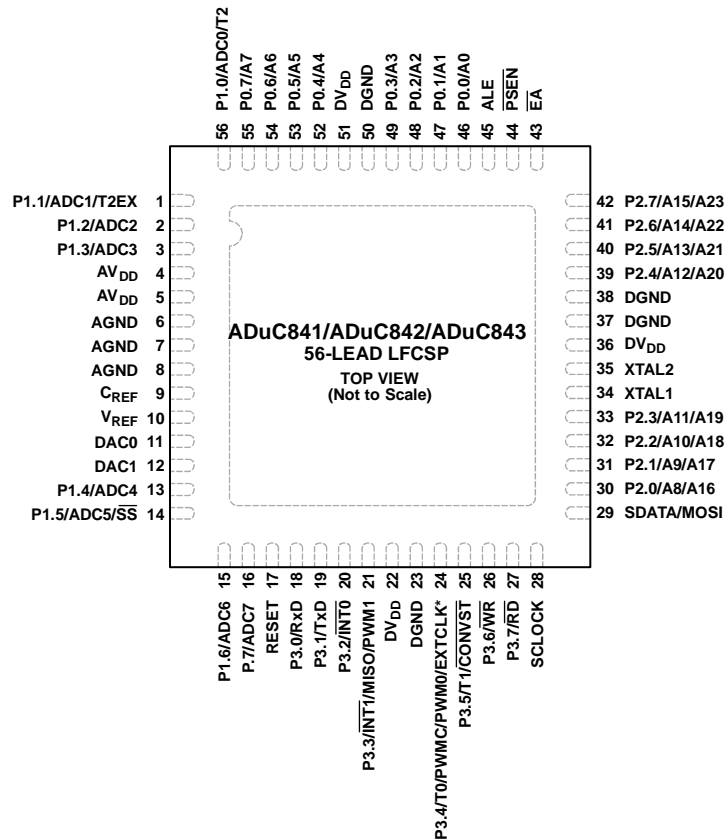
Idle Mode: Reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON (ADuC842/ADuC843), PCON.0 = 1, core execution suspended in idle mode.

Power-Down Mode: Reset = 0.4 V, all Port 0 pins = 0.4 V, All other digital I/O and Port 1 pins are open circuit, Core Clk changed via CD bits in PLLCON (ADuC842/ADuC843), PCON.0 = 1, core execution suspended in power-down mode, OSC turned on or off via OSC\_PD bit (PLLCON.7) in PLLCON SFR (ADuC842/ADuC843).

<sup>20</sup>  $V_{\text{DD}}$  power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

<sup>21</sup> Power supply currents are production tested at 5.25 V and 3.3 V for a 5 V and 3 V part, respectively.





\*EXTCLK NOT PRESENT ON THE ADuC841

#### NOTES

1. THE LFCSP HAS AN EXPOSED PAD THAT MUST BE SOLDERED TO THE METAL PLATE ON THE PRINTED CIRCUIT BOARD (PCB) FOR MECHANICAL REASONS AND TO DGND.

03260-004

Figure 4. 56-Lead LFCSP Pin Configuration

Table 4. 56-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Type <sup>1</sup>	Description
1	P1.1/ADC1/T2EX	I	Input Port 1 (P1.1). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit. Single-Ended Analog Input 1 (ADC1). Channel selection is via ADCCON2 SFR. Capture/Reload Trigger for Counter 2 (T2EX). Digital Input. This pin also functions as an up/down control input for Counter 2.
2	P1.2/ADC2	I	Input Port 1 (P1.2). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit. Single-Ended Analog Input (ADC2). Channel selection is via ADCCON2 SFR.
3	P1.3/ADC3	I	Input Port 1 (P1.3). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit. Single-Ended Analog Input (ADC3). Channel selection is via ADCCON2 SFR.
4, 5	AV <sub>DD</sub>	P	Analog Positive Supply Voltage. 3 V or 5 V nominal.
6, 7, 8	AGND	G	Analog Ground. AGND is the ground reference point for the analog circuitry.
9	C <sub>REF</sub>	I/O	Decoupling Input for On-Chip Reference. Connect a 0.47 $\mu$ F capacitor between this pin and AGND.
10	V <sub>REF</sub>	NC	Not Connected. This was a reference output on the <a href="#">ADuC812</a> ; use the C <sub>REF</sub> pin instead.
11	DAC0	O	Voltage Output from DAC0. This pin is a no connect on the <a href="#">ADuC843</a> .

## TERMINOLOGY

### ADC SPECIFICATIONS

#### Integral Nonlinearity

The maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point  $\frac{1}{2}$  LSB below the first code transition, and full scale, a point  $\frac{1}{2}$  LSB above the last code transition.

#### Differential Nonlinearity

The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

#### Offset Error

The deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, that is,  $+\frac{1}{2}$  LSB.

#### Gain Error

The deviation of the last code transition from the ideal AIN voltage (Full Scale –  $\frac{1}{2}$  LSB) after the offset error has been adjusted out.

#### Signal-to-(Noise + Distortion) Ratio

The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ( $f_s/2$ ), excluding dc. The ratio depends on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\text{Signal-to-(Noise + Distortion)} = (6.02N + 1.76) \text{ dB}$$

Thus for a 12-bit converter, this is 74 dB.

#### Total Harmonic Distortion (THD)

The ratio of the rms sum of the harmonics to the fundamental.

### DAC SPECIFICATIONS

#### Relative Accuracy

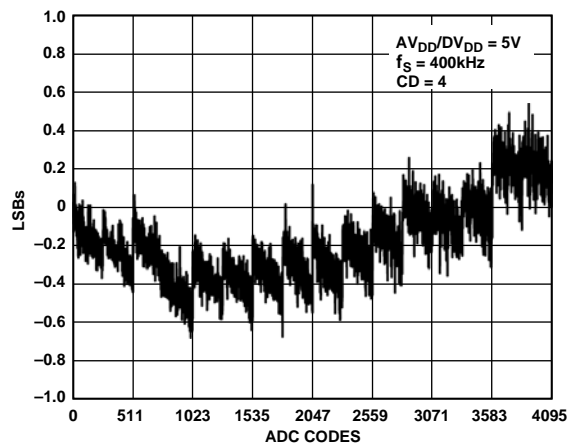
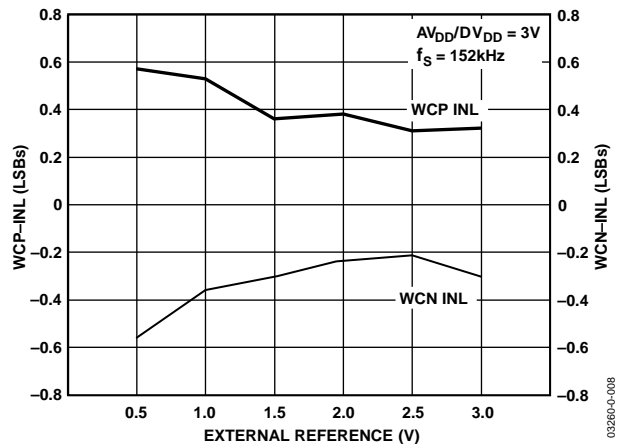
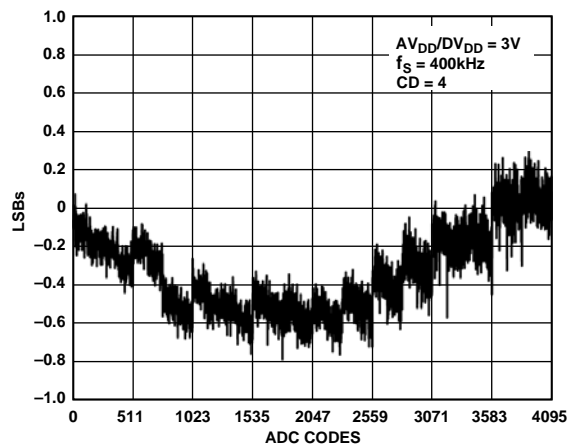
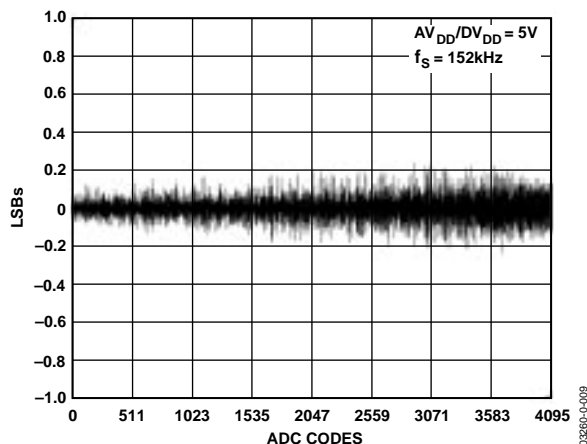
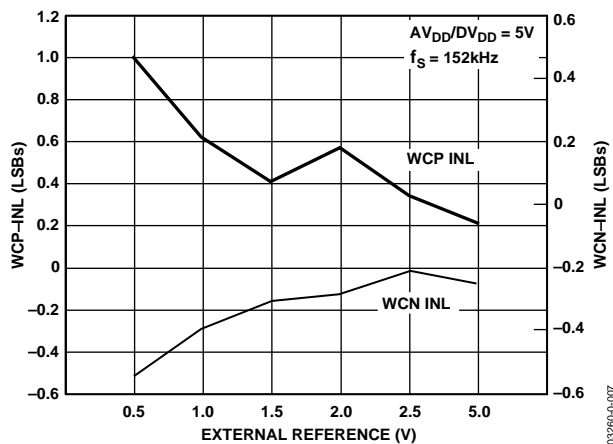
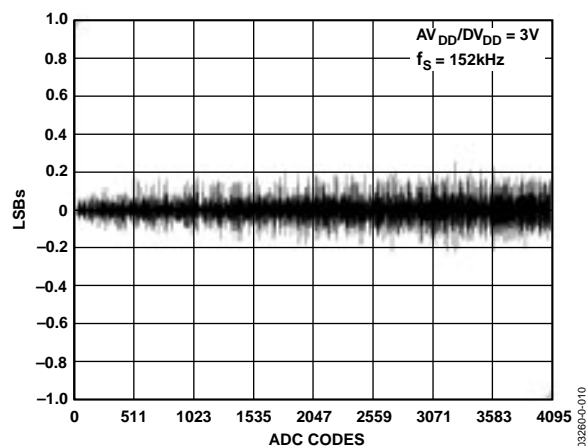
Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

#### Voltage Output Settling Time

The amount of time it takes for the output to settle to a specified level for a full-scale input change.

#### Digital-to-Analog Glitch Impulse

The amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV-sec.

Figure 7. Typical INL Error,  $V_{DD} = 5\text{ V}$ ,  $f_S = 400\text{ kHz}$ Figure 10. Typical Worst-Case INL Error vs.  $V_{REF}$ ,  $V_{DD} = 3\text{ V}$ Figure 8. Typical INL Error,  $V_{DD} = 3\text{ V}$ ,  $f_S = 400\text{ kHz}$ Figure 11. Typical DNL Error,  $V_{DD} = 5\text{ V}$ Figure 9. Typical Worst-Case INL Error vs.  $V_{REF}$ ,  $V_{DD} = 5\text{ V}$ Figure 12. Typical DNL Error,  $V_{DD} = 3\text{ V}$

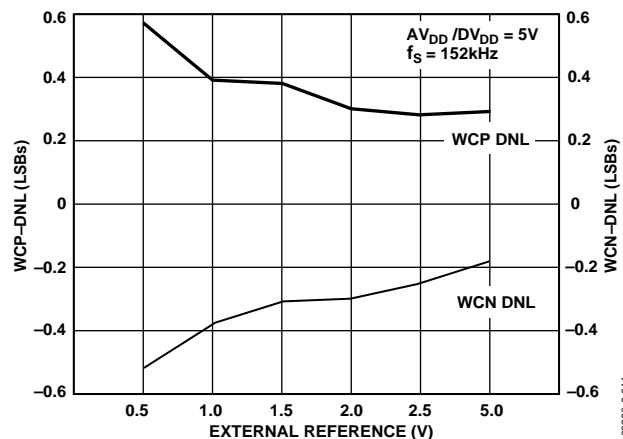


Figure 13. Typical Worst-Case DNL Error vs.  $V_{REF}$ ,  $V_{DD} = 5\text{ V}$

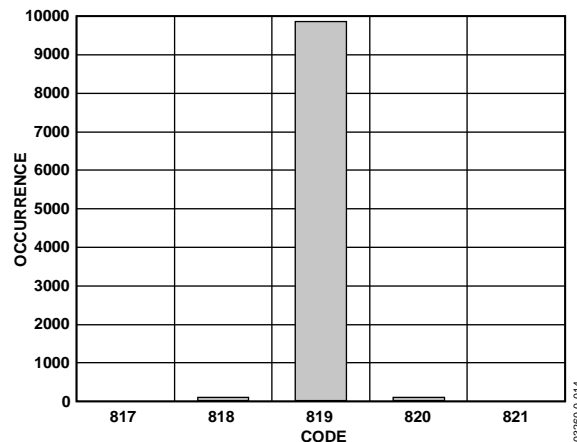


Figure 16. Code Histogram Plot,  $V_{DD} = 3\text{ V}$

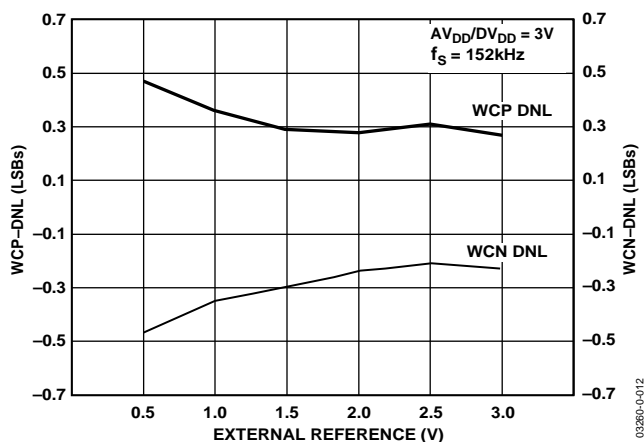


Figure 14. Typical Worst-Case DNL Error vs.  $V_{REF}$ ,  $V_{DD} = 3\text{ V}$

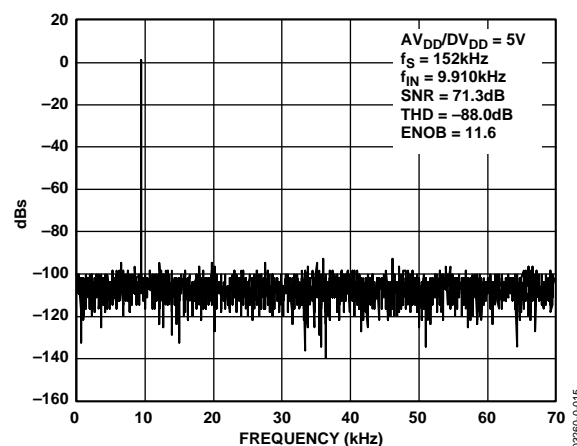


Figure 17. Dynamic Performance at  $V_{DD} = 5\text{ V}$

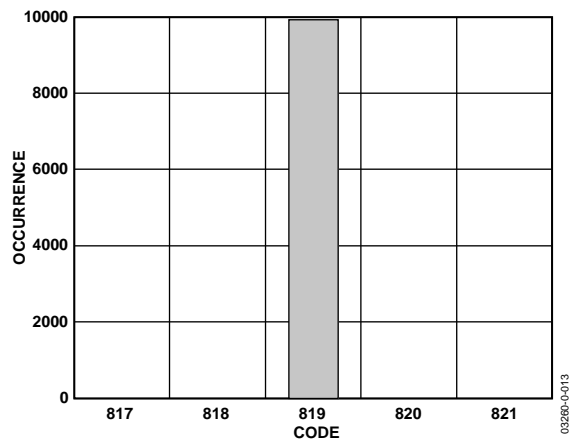


Figure 15. Code Histogram Plot,  $V_{DD} = 5\text{ V}$

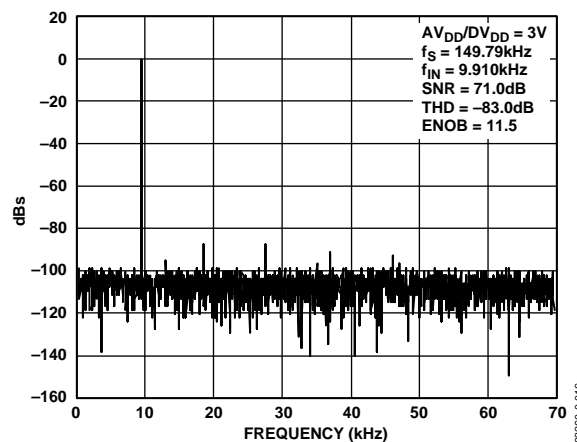


Figure 18. Dynamic Performance at  $V_{DD} = 3\text{ V}$

If using the temperature sensor as the ADC input, the ADC should be configured to use an ADCCLK of MCLK/32 and four acquisition clocks.

Increasing the conversion time on the temperature monitor channel improves the accuracy of the reading. To further improve the accuracy, an external reference with low temperature drift should also be used.

### ADC DMA Mode

The on-chip ADC has been designed to run at a maximum conversion speed of 2.38  $\mu$ s (420 kHz sampling rate). When converting at this rate, the ADuC841/ADuC842/ADuC843 MicroConverter® has 2  $\mu$ s to read the ADC result and to store the result in memory for further postprocessing; otherwise the next ADC sample could be lost. In an interrupt driven routine, the MicroConverter would also have to jump to the ADC interrupt service routine, which also increases the time required to store the ADC results. In applications where the parts cannot sustain the interrupt rate, an ADC DMA mode is provided.

To enable DMA mode, Bit 6 in ADCCON2 (DMA) must be set, which allows the ADC results to be written directly to a 16 MByte external static memory SRAM (mapped into data memory space) without any interaction from the core of the part. This mode allows the part to capture a contiguous sample stream at full ADC update rates (420 kHz).

### Typical DMA Mode Configuration Example

Setting the parts to DMA mode consists of the following steps:

1. The ADC must be powered down. This is done by ensuring that MD1 and MD0 are both set to 0 in ADCCON1.
2. The DMA address pointer must be set to the start address of where the ADC results are to be written. This is done by writing to the DMA mode address pointers DMAL, DMAH, and DMAP. DMAL must be written to first, followed by DMAH, and then by DMAP.
3. The external memory must be preconfigured. This consists of writing the required ADC channel IDs into the top four bits of every second memory location in the external SRAM, starting at the first address specified by the DMA address pointer. Because the ADC DMA mode operates independently from the ADuC841/ADuC842/ADuC843 core, it is necessary to provide it with a stop command. This is done by duplicating the last channel ID to be converted followed by 1111 into the next channel selection field. A typical preconfiguration of external memory is shown in Figure 34.

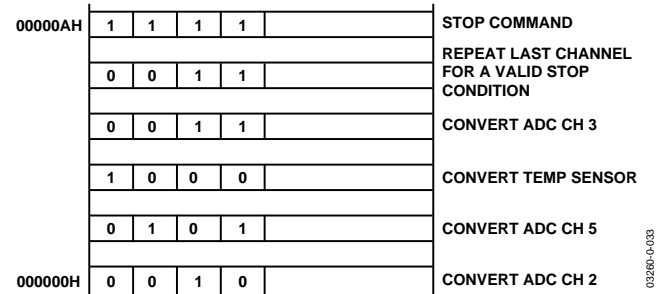


Figure 34. Typical DMA External Memory Preconfiguration

4. The DMA is initiated by writing to the ADC SFRs in the following sequence:
  - a. ADCCON2 is written to enable the DMA mode, that is, MOV ADCCON2, #40H; DMA mode enabled.
  - b. ADCCON1 is written to configure the conversion time and power-up of the ADC. It can also enable Timer 2 driven conversions or external triggered conversions if required.
  - c. ADC conversions are initiated. This is done by starting single conversions, starting Timer 2, running for Timer 2 conversions, or receiving an external trigger.

When the DMA conversions are complete, the ADC interrupt bit, ADCI, is set by hardware, and the external SRAM contains the new ADC conversion results as shown in Figure 35. Note that no result is written to the last two memory locations.

When the DMA mode logic is active, it takes the responsibility of storing the ADC results away from both the user and the core logic of the part. As the DMA interface writes the results of the ADC conversions to external memory, it takes over the external memory interface from the core. Thus, any core instructions that access the external memory while DMA mode is enabled does not get access to the external memory. The core executes the instructions, and they take the same time to execute, but they cannot access the external memory.

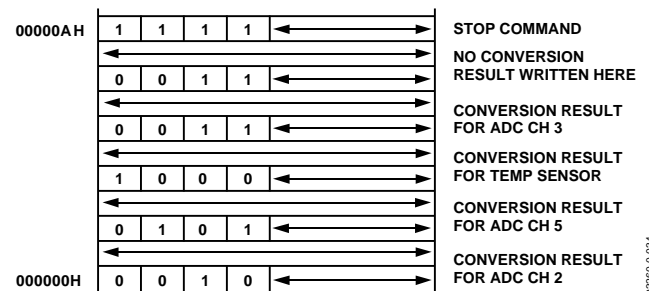


Figure 35. Typical External Memory Configuration Post ADC DMA Operation



**Example: Programming the Flash/EE Data Memory**

A user wants to program F3H into the second byte on Page 03H of the Flash/EE data memory space while preserving the other 3 bytes already in this page. A typical program of the Flash/EE data array involves

1. Setting EADRH/L with the page address.
2. Writing the data to be programmed to the EDATA1-4.
3. Writing the ECON SFR with the appropriate command.

**Step 1: Set Up the Page Address**

Address registers EADRH and EADRL hold the high byte address and the low byte address of the page to be addressed. The assembly language to set up the address may appear as

```
MOV EADRH,#0           ; Set Page Address Pointer
MOV EADRL,#03H
```

**Step 2: Set Up the EDATA Registers**

Write the four values to be written into the page into the four SFRs, EDATA1-4. Unfortunately, the user does not know three of them. Thus, the user must read the current page and overwrite the second byte.

```
MOV ECON,#1           ; Read Page into EDATA1-4
MOV EDATA2,#0F3H      ; Overwrite byte 2
```

**Step 3: Program Page**

A byte in the Flash/EE array can be programmed only if it has previously been erased. To be more specific, a byte can be programmed only if it already holds the value FFH. Because of the Flash/EE architecture, this erase must happen at a page level; therefore, a minimum of 4 bytes (1 page) are erased when an erase command is initiated. Once the page is erase, the user can program the 4 bytes in-page and then perform a verification of the data.

```
MOV ECON,#5           ; ERASE Page
MOV ECON,#2           ; WRITE Page
MOV ECON,#4           ; VERIFY Page
MOV A,ECON             ; Check if ECON=0 (OK!)
JNZ ERROR
```

Although the 4 kBytes of Flash/EE data memory are shipped from the factory pre-erased, that is, byte locations set to FFH, it is nonetheless good programming practice to include an ERASEALL routine as part of any configuration/setup code running on the parts. An ERASEALL command consists of writing 06H to the ECON SFR, which initiates an erase of the 4-kByte Flash/EE array. This command coded in 8051 assembly would appear as

```
MOV ECON,#06H         ; Erase all Command
                     ; 2 ms Duration
```

**Flash/EE Memory Timing**

Typical program and erase times for the parts are as follows:

**Normal Mode (operating on Flash/EE data memory)**

READPAGE (4 bytes)	22 machine cycles
WRITEPAGE (4 bytes)	380 $\mu$ s
VERIFYPAGE (4 bytes)	22 machine cycles
ERASEPAGE (4 bytes)	2 ms
ERASEALL (4 kBytes)	2 ms
READBYTE (1 byte)	9 machine cycles
WRITEBYTE (1 byte)	200 $\mu$ s

**ULOAD Mode (operating on Flash/EE program memory)**

WRITEPAGE (256 bytes)	16.5 ms
ERASEPAGE (64 bytes)	2 ms
ERASEALL (56 kBytes)	2 ms
WRITEBYTE (1 byte)	200 $\mu$ s

Note that a given mode of operation is initiated as soon as the command word is written to the ECON SFR. The core micro-controller operation on the parts is idled until the requested program/read or erase mode is completed. In practice, this means that even though the Flash/EE memory mode of operation is typically initiated with a two machine cycle MOV instruction (to write to the ECON SFR), the next instruction is not executed until the Flash/EE operation is complete. This means that the core cannot respond to interrupt requests until the Flash/EE operation is complete, although the core peripheral functions like counter/timers continue to count and time as configured throughout this period.

CFG841	ADuC841 Config SFR
SFR Address	AFH
Power-On Default	10H <sup>1</sup>
Bit Addressable	No

Table 15. CFG841 SFR Bit Designations

Bit No.	Name	Description																												
7	EXSP	Extended SP Enable. When set to 1 by the user, the stack rolls over from SPH/SP = 00FFH to 0100H. When set to 0 by the user, the stack rolls over from SP = FFH to SP = 00H.																												
6	PWPO	PWM Pin Out Selection. Set to 1 by the user to select P3.4 and P3.3 as the PWM output pins. Set to 0 by the user to select P2.6 and P2.7 as the PWM output pins.																												
5	DBUF	DAC Output Buffer. Set to 1 by the user to bypass the DAC output buffer. Set to 0 by the user to enable the DAC output buffer.																												
4	EPM2	Flash/EE Controller and PWM Clock Frequency Configuration Bits. Frequency should be configured such that $F_{osc}/Divide\ Factor = 32\ kHz + 50\%$ .																												
3	EPM1	<table><tr><th>EPM2</th><th>EPM1</th><th>EPM0</th><th>Divide Factor</th></tr><tr><td>0</td><td>0</td><td>0</td><td>32</td></tr><tr><td>0</td><td>0</td><td>1</td><td>64</td></tr><tr><td>0</td><td>1</td><td>0</td><td>128</td></tr><tr><td>0</td><td>1</td><td>1</td><td>256</td></tr><tr><td>1</td><td>0</td><td>0</td><td>512</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1024</td></tr></table>	EPM2	EPM1	EPM0	Divide Factor	0	0	0	32	0	0	1	64	0	1	0	128	0	1	1	256	1	0	0	512	1	0	1	1024
EPM2	EPM1		EPM0	Divide Factor																										
0	0		0	32																										
0	0		1	64																										
0	1		0	128																										
0	1		1	256																										
1	0	0	512																											
1	0	1	1024																											
2	EPM0																													
1	MSPI	Set to 1 by the user to move the SPI functionality of MISO, MOSI, and SCLOCK to P3.3, P3.4, and P3.5, respectively. Set to 0 by the user to leave the SPI functionality as usual on MISO, MOSI, and SCLOCK pins.																												
0	XRAMEN	XRAM Enable Bit. When set to 1 by the user, the internal XRAM is mapped into the lower two kBytes of the external address space. When set to 0 by the user, the internal XRAM is not accessible, and the external data memory is mapped into the lower two kBytes of external data memory.																												

<sup>1</sup> Note that the Flash/EE controller bits EPM2, EPM1, EPM0 are set to their correct values depending on the crystal frequency at power-up. The user should not modify these bits so all instructions to the CFG841 register should use the ORL, XRL, or ANL instructions. Value of 10H is for 11.0592 MHz crystal.

## USER INTERFACE TO ON-CHIP PERIPHERALS

This section gives a brief overview of the various peripherals also available on-chip. A summary of the SFRs used to control and configure these peripherals is also given.

### DAC

The ADuC841/ADuC842 incorporate two 12-bit voltage output DACs on-chip. Each has a rail-to-rail voltage output buffer capable of driving 10 k $\Omega$ /100 pF. Each has two selectable ranges, 0 V to  $V_{REF}$  (the internal band gap 2.5 V reference) and 0 V to  $AV_{DD}$ . Each can operate in 12-bit or 8-bit mode.

Both DACs share a control register, DACCON, and four data registers, DAC1H/L, DAC0/L. Note that in 12-bit asynchronous mode, the DAC voltage output is updated as soon as the DACL data SFR has been written; therefore, the DAC data registers should be updated as DACH first, followed by DACL. Note that for correct DAC operation on the 0 V to  $V_{REF}$  range, the ADC must be switched on. This results in the DAC using the correct reference value.

DACCON	DAC Control Register
SFR Address	FDH
Power-On Default	04H
Bit Addressable	No

Table 16. DACCON SFR Bit Designations

Bit No.	Name	Description
7	MODE	The DAC MODE bit sets the overriding operating mode for both DACs. Set to 1 by the user to select 8-bit mode (write 8 bits to DACxL SFR). Set to 0 by the user to select 12-bit mode.
6	RNG1	DAC1 Range Select Bit. Set to 1 by the user to select the range for DAC1 as 0 V to $V_{DD}$ . Set to 0 by the user to select the range for DAC1 as 0 V to $V_{REF}$ .
5	RNG0	DAC0 Range Select Bit. Set to 1 by the user to select the range for DAC0 as 0 V to $V_{DD}$ . Set to 0 by the user to select the range for DAC0 as 0 V to $V_{REF}$ .
4	CLR1	DAC1 Clear Bit. Set to 1 by the user to leave the output of DAC1 at its normal level. Set to 0 by the user to force the output of DAC1 to 0 V.
3	CLR0	DAC0 Clear Bit. Set to 1 by the user to leave the output of DAC0 at its normal level. Set to 0 by the user to force the output of DAC0 to 0 V.
2	SYNC	DAC0/1 Update Synchronization Bit. When set to 1, the DAC outputs update as soon as DACxL SFRs are written. The user can simultaneously update both DACs by first updating the DACxL/H SFRs while SYNC is 0. Both DACs then update simultaneously when the SYNC bit is set to 1.
1	PD1	DAC1 Power-Down Bit. Set to 1 by the user to power on DAC1. Set to 0 by the user to power off DAC1.
0	PDO	DAC0 Power-Down Bit. Set to 1 by the user to power on DAC0. Set to 0 by the user to power off DAC0.

### DACxH/L

Function

SFR Address

Power-On Default

Bit Addressable

### DAC Data Registers

DAC data registers, written by the user to update the DAC output.

DAC0L (DAC0 Data Low Byte) -> F9H; DAC1L (DAC1 Data Low Byte) -> FBH

DACH (DAC0 Data High Byte) -> FAH; DAC1H (DAC1 Data High Byte) -> FCH

00H All Four Registers.

No All Four Registers.

The 12-bit DAC data should be written into DACxH/L right-justified such that DACxL contains the lower 8 bits, and the lower nibble of DACxH contains the upper 4 bits.

## PULSE-WIDTH MODULATOR (PWM)

The PWM on the [ADuC841/ADuC842/ADuC843](#) is a highly flexible PWM offering programmable resolution and an input clock, and can be configured for any one of six different modes of operation. Two of these modes allow the PWM to be configured as a  $\Sigma$ - $\Delta$  DAC with up to 16 bits of resolution. A block diagram of the PWM is shown in Figure 47. Note the PWM clock's sources are different for the [ADuC841](#), and are given in Table 18.

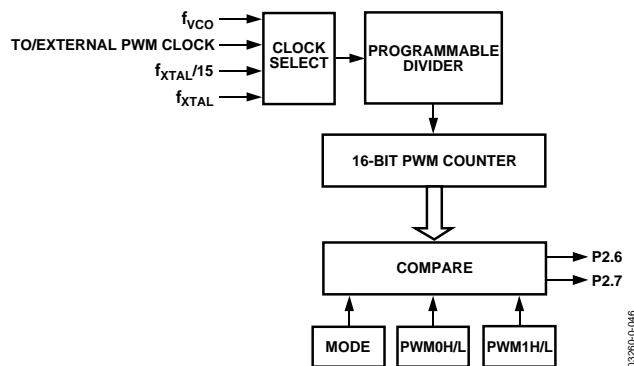


Figure 47. PWM Block Diagram

The PWM uses five SFRs: the control SFR (PWMCON) and four data SFRs (PWM0H, PWM0L, PWM1H, and PWM1L).

PWMCON, as described in the following sections, controls the different modes of operation of the PWM as well as the PWM clock frequency.

PWM0H/L and PWM1H/L are the data registers that determine the duty cycles of the PWM outputs. The output pins that the PWM uses are determined by the CFG841/CFG842 register, and can be either P2.6 and P2.7 or P3.4 and P3.3. In this section of the data sheet, it is assumed that P2.6 and P2.7 are selected as the PWM outputs.

To use the PWM user software, first write to PWMCON to select the PWM mode of operation and the PWM input clock. Writing to PWMCON also resets the PWM counter. In any of the 16-bit modes of operation (Modes 1, 3, 4, 6), user software should write to the PWM0L or PWM1L SFRs first. This value is written to a hidden SFR. Writing to the PWM0H or PWM1H SFRs updates both the PWMxH and the PWMxL SFRs but does not change the outputs until the end of the PWM cycle in progress. The values written to these 16-bit registers are then used in the next PWM cycle.

PWMCON PWM	Control SFR
SFR Address	AEH
Power-On Default	00H
Bit Addressable	No

Table 18. PWMCON SFR Bit Designations

Bit No.	Name	Description																																				
7	SNGL	Turns off PMW output at P2.6 or P3.4, leaving the port pin free for digital I/O.																																				
6	MD2	PWM Mode Bits.																																				
5	MD1	The MD2/1/0 bits choose the PWM mode as follows:																																				
4	MD0	<table><tr><td>MD2</td><td>MD1</td><td>MD0</td><td>Mode</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Mode 0: PWM Disabled</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Mode 1: Single variable resolution PWM on P2.7 or P3.3</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Mode 2: Twin 8-bit PWM</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Mode 3: Twin 16-bit PWM</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Mode 4: Dual NRZ 16-bit <math>\Sigma</math>-<math>\Delta</math> DAC</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Mode 5: Dual 8-bit PWM</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Mode 6: Dual RZ 16-bit <math>\Sigma</math>-<math>\Delta</math> DAC</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr></table>	MD2	MD1	MD0	Mode	0	0	0	Mode 0: PWM Disabled	0	0	1	Mode 1: Single variable resolution PWM on P2.7 or P3.3	0	1	0	Mode 2: Twin 8-bit PWM	0	1	1	Mode 3: Twin 16-bit PWM	1	0	0	Mode 4: Dual NRZ 16-bit $\Sigma$ - $\Delta$ DAC	1	0	1	Mode 5: Dual 8-bit PWM	1	1	0	Mode 6: Dual RZ 16-bit $\Sigma$ - $\Delta$ DAC	1	1	1	Reserved
MD2	MD1	MD0	Mode																																			
0	0	0	Mode 0: PWM Disabled																																			
0	0	1	Mode 1: Single variable resolution PWM on P2.7 or P3.3																																			
0	1	0	Mode 2: Twin 8-bit PWM																																			
0	1	1	Mode 3: Twin 16-bit PWM																																			
1	0	0	Mode 4: Dual NRZ 16-bit $\Sigma$ - $\Delta$ DAC																																			
1	0	1	Mode 5: Dual 8-bit PWM																																			
1	1	0	Mode 6: Dual RZ 16-bit $\Sigma$ - $\Delta$ DAC																																			
1	1	1	Reserved																																			
3	CDIV1	PWM Clock Divider.																																				
2	CDIV0	Scale the clock source for the PWM counter as follows: <table><tr><td>CDIV1</td><td>CDIV0</td><td>Description</td></tr><tr><td>0</td><td>0</td><td>PWM Counter = Selected Clock/1</td></tr><tr><td>0</td><td>1</td><td>PWM Counter = Selected Clock/4</td></tr><tr><td>1</td><td>0</td><td>PWM Counter = Selected Clock/16</td></tr><tr><td>1</td><td>1</td><td>PWM Counter = Selected Clock/64</td></tr></table>	CDIV1	CDIV0	Description	0	0	PWM Counter = Selected Clock/1	0	1	PWM Counter = Selected Clock/4	1	0	PWM Counter = Selected Clock/16	1	1	PWM Counter = Selected Clock/64																					
CDIV1	CDIV0	Description																																				
0	0	PWM Counter = Selected Clock/1																																				
0	1	PWM Counter = Selected Clock/4																																				
1	0	PWM Counter = Selected Clock/16																																				
1	1	PWM Counter = Selected Clock/64																																				
1	CSEL1	PWM Clock Divider.																																				
0	CSEL0	Select the clock source for the PWM as follows: <table><tr><td>CSEL1</td><td>CSEL0</td><td>Description</td></tr><tr><td>0</td><td>0</td><td>PWM Clock = <math>f_{XTAL}/15</math>, ADuC841 = <math>f_{OCS}/DIVIDE FACTOR /15</math> (see the CFG841 register)</td></tr><tr><td>0</td><td>1</td><td>PWM Clock = <math>f_{XTAL}</math>, ADuC841 = <math>f_{OCS}/DIVIDE FACTOR</math> (see the CFG841 register)</td></tr><tr><td>1</td><td>0</td><td>PWM Clock = External input at P3.4/T0</td></tr><tr><td>1</td><td>1</td><td>PWM Clock = <math>f_{VCO}</math> = 16.777216 MHz, ADuC841 = <math>f_{OSC}</math></td></tr></table>	CSEL1	CSEL0	Description	0	0	PWM Clock = $f_{XTAL}/15$ , ADuC841 = $f_{OCS}/DIVIDE FACTOR /15$ (see the CFG841 register)	0	1	PWM Clock = $f_{XTAL}$ , ADuC841 = $f_{OCS}/DIVIDE FACTOR$ (see the CFG841 register)	1	0	PWM Clock = External input at P3.4/T0	1	1	PWM Clock = $f_{VCO}$ = 16.777216 MHz, ADuC841 = $f_{OSC}$																					
CSEL1	CSEL0	Description																																				
0	0	PWM Clock = $f_{XTAL}/15$ , ADuC841 = $f_{OCS}/DIVIDE FACTOR /15$ (see the CFG841 register)																																				
0	1	PWM Clock = $f_{XTAL}$ , ADuC841 = $f_{OCS}/DIVIDE FACTOR$ (see the CFG841 register)																																				
1	0	PWM Clock = External input at P3.4/T0																																				
1	1	PWM Clock = $f_{VCO}$ = 16.777216 MHz, ADuC841 = $f_{OSC}$																																				

## PWM Modes of Operation

### Mode 0: PWM Disabled

The PWM is disabled allowing P2.6 and P2.7 to be used as normal.

### Mode 1: Single Variable Resolution PWM

In Mode 1, both the pulse length and the cycle time (period) are programmable in user code, allowing the resolution of the PWM to be variable.

PWM1H/L sets the period of the output waveform. Reducing PWM1H/L reduces the resolution of the PWM output but increases the maximum output rate of the PWM. For example, setting PWM1H/L to 65536 gives a 16-bit PWM with a maximum output rate of 266 Hz ( $16.777 \text{ MHz}/65536$ ). Setting PWM1H/L to 4096 gives a 12-bit PWM with a maximum output rate of 4096 Hz ( $16.777 \text{ MHz}/4096$ ).

PWM0H/L sets the duty cycle of the PWM output waveform, as shown in Figure 48.

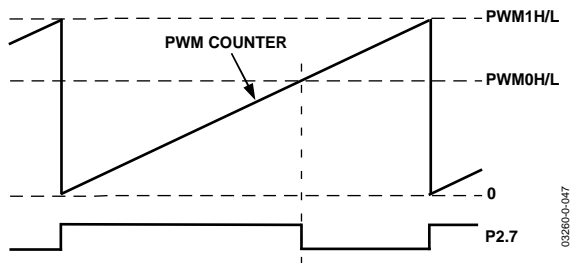


Figure 48. PWM in Mode 1

### Mode 2: Twin 8-Bit PWM

In Mode 2, the duty cycle of the PWM outputs and the resolution of the PWM outputs are both programmable. The maximum resolution of the PWM output is 8 bits.

PWM1L sets the period for both PWM outputs. Typically, this is set to 255 (FFH) to give an 8-bit PWM, although it is possible to reduce this as necessary. A value of 100 could be loaded here to give a percentage PWM, that is, the PWM is accurate to 1%.

The outputs of the PWM at P2.6 and P2.7 are shown in Figure 49. As can be seen, the output of PWM0 (P2.6) goes low when the PWM counter equals PWM0L. The output of PWM1 (P2.7) goes high when the PWM counter equals PWM1H and goes low again when the PWM counter equals PWM0H. Setting PWM1H to 0 ensures that both PWM outputs start simultaneously.

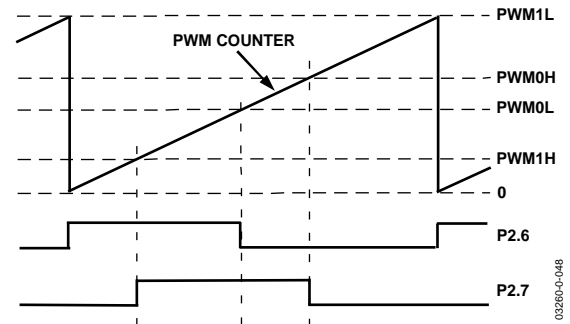


Figure 49. PWM Mode 2

### Mode 3: Twin 16-Bit PWM

In Mode 3, the PWM counter is fixed to count from 0 to 65536, giving a fixed 16-bit PWM. Operating from the 16.777 MHz core clock results in a PWM output rate of 256 Hz. The duty cycle of the PWM outputs at P2.6 and P2.7 is independently programmable.

As shown in Figure 50, while the PWM counter is less than PWM0H/L, the output of PWM0 (P2.6) is high. Once the PWM counter equals PWM0H/L, PWM0 (P2.6) goes low and remains low until the PWM counter rolls over.

Similarly, while the PWM counter is less than PWM1H/L, the output of PWM1 (P2.7) is high. Once the PWM counter equals PWM1H/L, PWM1 (P2.7) goes low and remains low until the PWM counter rolls over.

In this mode, both PWM outputs are synchronized, that is, once the PWM counter rolls over to 0, both PWM0 (P2.6) and PWM1 go high.

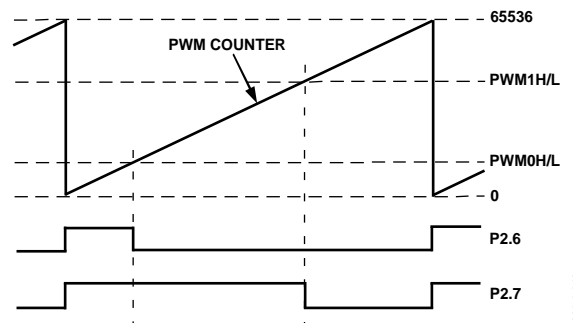


Figure 50. PWM Mode 3

<b>TIMECON</b>	<b>TIC Control Register</b>
SFR Address	A1H
Power-On Default	00H
Bit Addressable	No

Table 25. TIMECON SFR Bit Designations

Bit No.	Name	Description															
7	----	Reserved.															
6	TFH	Twenty-Four Hour Select Bit. Set by the user to enable the hour counter to count from 0 to 23. Cleared by the user to enable the hour counter to count from 0 to 255.															
5	ITS1	Interval Timebase Selection Bits.															
4	ITS0	Written by user to determine the interval counter update rate. <table> <tr> <td>ITS1</td><td>ITS0</td><td>Interval Timebase</td></tr> <tr> <td>0</td><td>0</td><td>1/128 Second</td></tr> <tr> <td>0</td><td>1</td><td>Seconds</td></tr> <tr> <td>1</td><td>0</td><td>Minutes</td></tr> <tr> <td>1</td><td>1</td><td>Hours</td></tr> </table>	ITS1	ITS0	Interval Timebase	0	0	1/128 Second	0	1	Seconds	1	0	Minutes	1	1	Hours
ITS1	ITS0	Interval Timebase															
0	0	1/128 Second															
0	1	Seconds															
1	0	Minutes															
1	1	Hours															
3	STI	Single Time Interval Bit. Set by the user to generate a single interval timeout. If set, a timeout clears the TIEN bit. Cleared by the user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.															
2	TII	TIC Interrupt Bit. Set when the 8-bit interval counter matches the value in the INTVAL SFR. Cleared by user software.															
1	TIEN	Time Interval Enable Bit. Set by the user to enable the 8-bit time interval counter. Cleared by the user to disable the interval counter.															
0	TCEN	Time Clock Enable Bit. Set by the user to enable the time clock to the time interval counters. Cleared by the user to disable the clock to the time interval counters and reset the time interval SFRs to the last value written to them by the user. The time registers (HTHSEC, SEC, MIN, and HOUR) can be written while TCEN is low.															

<b>T2CON</b>	<b>Timer/Counter 2 Control Register</b>
SFR Address	C8H
Power-On Default	00H
Bit Addressable	Yes

**Table 31. T2CON SFR Bit Designations**

Bit No.	Name	Description
7	TF2	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 cannot be set when either RCLK = 1 or TCLK = 1. Cleared by user software.
6	EXF2	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. Cleared by user software.
5	RCLK	Receive Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the receive clock.
4	TCLK	Transmit Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the transmit clock.
3	EXEN2	Timer 2 External Enable Flag. Set by the user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by the user for Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 Start/Stop Control Bit. Set by the user to start Timer 2. Cleared by the user to stop Timer 2.
1	CNT2	Timer 2 Timer or Counter Function Select Bit. Set by the user to select counter function (input from external T2 pin). Cleared by the user to select timer function (input from on-chip core clock).
0	CAP2	Timer 2 Capture/Reload Select Bit. Set by the user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by the user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

**Timer/Counter 2 Data Registers**

Timer/Counter 2 also has two pairs of 8-bit data registers associated with it. These are used as both timer data registers and as timer capture/reload registers.

**TH2 and TL2**

Timer 2, data high byte and low byte.  
SFR Address = CDH, CCH, respectively.

**RCAP2H and RCAP2L**

Timer 2, capture/reload byte and low byte.  
SFR Address = CBH, CAH, respectively.

### Mode 3: 9-Bit UART with Variable Baud Rate

Mode 3 is selected by setting both SM0 and SM1. In this mode, the 8051 UART serial port operates in 9-bit mode with a variable baud rate determined by either Timer 1 or Timer 2. The operation of the 9-bit UART is the same as for Mode 2, but the baud rate can be varied as for Mode 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

### UART Serial Port Baud Rate Generation

#### Mode 0 Baud Rate Generation

The baud rate in Mode 0 is fixed.

$$\text{Mode 0 Baud Rate} = (\text{Core Clock Frequency}/12)$$

#### Mode 2 Baud Rate Generation

The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/32 of the core clock. If SMOD = 1, the baud rate is 1/16 of the core clock:

$$\text{Mode 2 Baud Rate} = (2^{\text{SMOD}}/32 \times [\text{Core Clock Frequency}])$$

#### Modes 1 and 3 Baud Rate Generation

The baud rates in Modes 1 and 3 are determined by the overflow rate in Timer 1 or Timer 2, or in both (one for transmit and the other for receive).

#### Timer 1 Generated Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$\text{Modes 1 and 3 Baud Rate} = (2^{\text{SMOD}}/32 \times (\text{Timer 1 Overflow Rate}))$$

The Timer 1 interrupt should be disabled in this application. The timer itself can be configured for either timer or counter operation, and in any of its three running modes. In the most typical application, it is configured for timer operation in the autoreload mode (high nibble of TMOD = 0010 binary). In that case, the baud rate is given by the formula

$$\begin{aligned} \text{Modes 1 and 3 Baud Rate} = \\ (2^{\text{SMOD}}/32) \times (\text{Core Clock} / [256 - \text{TH1}]) \end{aligned}$$

#### Timer 2 Generated Baud Rates

Baud rates can also be generated using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted/received. Because Timer 2 has a 16-bit autoreload mode, a wider range of baud rates is possible using Timer 2.

$$\text{Modes 1 and 2 Baud Rate} = (1/16) \times (\text{Timer 2 Overflow Rate})$$

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles rather than every core machine cycle as before. Thus, it increments six times faster than Timer 1, and therefore baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible.

Timer 2 is selected as the baud rate generator by setting the TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 73.

In this case, the baud rate is given by the formula

$$\begin{aligned} \text{Modes 1 and 3 Baud Rate} = \\ (\text{Core Clock}) / (16 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]) \end{aligned}$$

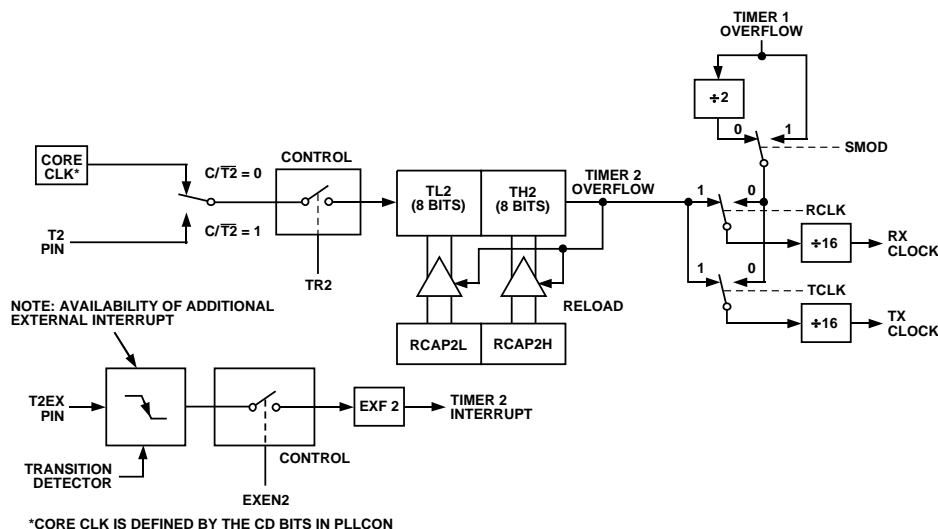


Figure 73. Timer 2, UART Baud Rates



<b>IEIP2</b>	<b>Secondary Interrupt Enable Register</b>
SFR Address	A9H
Power-On Default	A0H
Bit Addressable	No

**Table 38. IEIP2 SFR Bit Designations**

Bit No.	Name	Description
7	----	Reserved.
6	PTI	Priority for time interval interrupt.
5	PPSM	Priority for power supply monitor interrupt.
4	PSI	Priority for SPI/I <sup>2</sup> C interrupt.
3	----	This bit must contain zero.
2	ETI	Set by the user to enable, or cleared to disable time interval counter interrupts.
1	EPSMI	Set by the user to enable, or cleared to disable power supply monitor interrupts.
0	ESI	Set by the user to enable, or cleared to disable SPI or I <sup>2</sup> C serial port interrupts.

**Interrupt Priority**

The interrupt enable registers are written by the user to enable individual interrupt sources, while the interrupt priority registers allow the user to select one of two priority levels for each interrupt. An interrupt of a high priority may interrupt the service routine of a low priority interrupt, and if two interrupts of different priority occur at the same time, the higher level interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed as shown in Table 39.

**Table 39. Priority within an Interrupt Level**

Source	Priority	Description
PSMI	1 (Highest)	Power Supply Monitor Interrupt.
WDS	2	Watchdog Timer Interrupt.
IE0	2	External Interrupt 0.
ADCI	3	ADC Interrupt.
TF0	4	Timer/Counter 0 Interrupt.
IE1	5	External Interrupt 1.
TF1	6	Timer/Counter 1 Interrupt.
ISPI/I <sup>2</sup> CI	7	SPI Interrupt/I <sup>2</sup> C Interrupt.
RI + TI	8	Serial Interrupt.
TF2 + EXF2	9	Timer/Counter 2 Interrupt.
TII	11(Lowest)	Time Interval Counter Interrupt.

**Interrupt Vectors**

When an interrupt occurs, the program counter is pushed onto the stack, and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown in Table 40.

**Table 40. Interrupt Vector Addresses**

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH
ADCI	0033H
ISPI/I <sup>2</sup> CI	003BH
PSMI	0043H
TII	0053H
WDS	005BH

If access to more than 64 kBytes of RAM is desired, a feature unique to the ADuC841/ADuC842/ADuC843 allows addressing up to 16 MBytes of external RAM simply by adding an additional latch as illustrated in Figure 79.

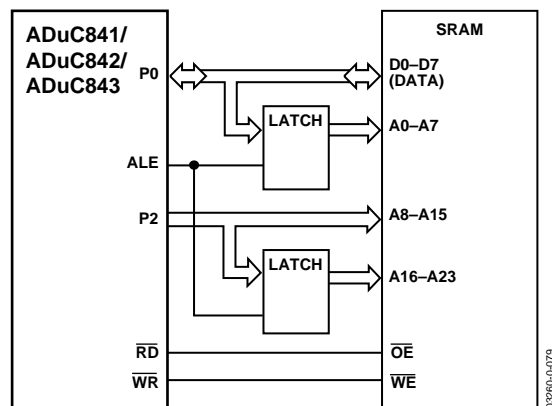


Figure 79. External Data Memory Interface (16 MBytes Address Space)

In either implementation, Port 0 (P0) serves as a multiplexed address/data bus. It emits the low byte of the data pointer (DPL) as an address, which is latched by a pulse of ALE prior to data being placed on the bus by the ADuC841/ADuC842/ADuC843 (write operation) or by the SRAM (read operation). Port 2 (P2) provides the data pointer page byte (DPP) to be latched by ALE, followed by the data pointer high byte (DPH). If no latch is connected to P2, DPP is ignored by the SRAM, and the 8051 standard of 64 kBytes external data memory access is maintained.

### Power Supplies

The operational power supply voltage of the parts depends on whether the part is the 3 V version or the 5 V version. The specifications are given for power supplies within 2.7 V to 3.6 V or  $\pm 5\%$  of the nominal 5 V level.

Note that Figure 80 and Figure 81 refer to the PQFP package. For the CSP package, connect the extra DV<sub>DD</sub>, DGND, AV<sub>DD</sub>, and AGND in the same manner. Also, the paddle on the bottom of the package should be soldered to a metal plate to provide mechanical stability. This metal plate should not be connected to ground.

Separate analog and digital power supply pins (AV<sub>DD</sub> and DV<sub>DD</sub>, respectively) allow AV<sub>DD</sub> to be kept relatively free of the noisy digital signals that are often present on the system DV<sub>DD</sub> line. However, though you can power AV<sub>DD</sub> and DV<sub>DD</sub> from two separate supplies if desired, you must ensure that they remain within  $\pm 0.3$  V of one another at all times to avoid damaging the chip (as per the Absolute Maximum Ratings section). Therefore, it is recommended that unless AV<sub>DD</sub> and DV<sub>DD</sub> are

connected directly together, back-to-back Schottky diodes should be connected between them, as shown in Figure 80.

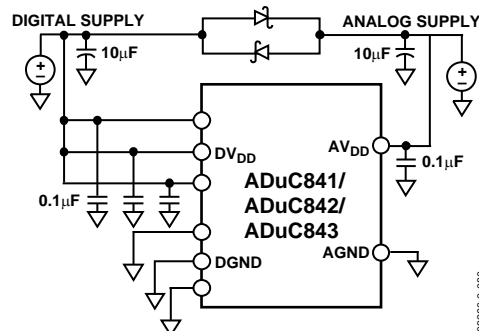


Figure 80. External Dual-Supply Connections

As an alternative to providing two separate power supplies, the user can help keep AV<sub>DD</sub> quiet by placing a small series resistor and/or ferrite bead between it and DV<sub>DD</sub>, and then decoupling AV<sub>DD</sub> separately to ground. An example of this configuration is shown in Figure 81. With this configuration, other analog circuitry (such as op amps and voltage reference) can be powered from the AV<sub>DD</sub> supply line as well. The user still needs to include back-to-back Schottky diodes between AV<sub>DD</sub> and DV<sub>DD</sub> to protect them from power-up and power-down transient conditions that could momentarily separate the two supply voltages.

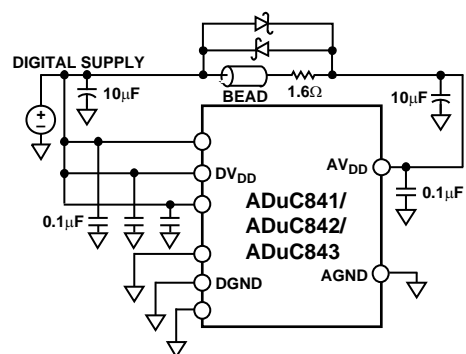


Figure 81. External Single-Supply Connections

Notice that in both Figure 80 and Figure 81, a large value (10 µF) reservoir capacitor sits on DV<sub>DD</sub> and a separate 10 µF capacitor sits on AV<sub>DD</sub>. Also, local small-value (0.1 µF) capacitors are located at each V<sub>DD</sub> pin of the chip. As per standard design practice, be sure to include all of these capacitors, and ensure the smaller capacitors are close to each AV<sub>DD</sub> pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, note that at all times, the analog and digital ground pins on the part must be referenced to the same system ground reference point.

TIMING SPECIFICATIONS<sup>1, 2, 3</sup>Table 42.  $AV_{DD} = 2.7\text{ V to }3.6\text{ V or }4.75\text{ V to }5.25\text{ V}$ ,  $DV_{DD} = 2.7\text{ V to }3.6\text{ V or }4.75\text{ V to }5.25\text{ V}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted

Parameter ADuC842/ADuC843 CLOCK INPUT (External Clock Driven XTAL1)		32.768 kHz External Crystal			Unit
		Min	Typ	Max	
$t_{CK}$	XTAL1 Period		30.52		$\mu\text{s}$
$t_{CKL}$	XTAL1 Width Low		6.26		$\mu\text{s}$
$t_{CKH}$	XTAL1 Width High		6.26		$\mu\text{s}$
$t_{CKR}$	XTAL1 Rise Time		9		ns
$t_{CKF}$	XTAL1 Fall Time		9		ns
$1/t_{CORE}$	ADuC842/ADuC843 Core Clock Frequency <sup>4</sup>	0.131		16.78	MHz
$t_{CORE}$	ADuC842/ADuC843 Core Clock Period <sup>5</sup>		0.476		$\mu\text{s}$
$t_{CYC}$	ADuC842/ADuC843 Machine Cycle Time <sup>6</sup>	0.059	0.476	7.63	$\mu\text{s}$

<sup>1</sup> AC inputs during testing are driven at  $DV_{DD} - 0.5\text{ V}$  for a Logic 1 and  $0.45\text{ V}$  for Logic 0. Timing measurements are made at  $V_{IH}$  min for Logic 1 and  $V_{IL}$  max for Logic 0, as shown in Figure 87.

<sup>2</sup> For timing purposes, a port pin is no longer floating when a  $100\text{ mV}$  change from load voltage occurs. A port pin begins to float when a  $100\text{ mV}$  change from the loaded  $V_{OH}/V_{OL}$  level occurs, as shown in Figure 87.

<sup>3</sup>  $C_{LOAD}$  for all outputs =  $80\text{ pF}$ , unless otherwise noted.

<sup>4</sup> ADuC842/ADuC843 internal PLL locks onto a multiple (512 times) of the  $32.768\text{ kHz}$  external crystal frequency to provide a stable  $16.78\text{ MHz}$  internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core\_Clk, selected via the PLLCON SFR.

<sup>5</sup> This number is measured at the default Core\_Clk operating frequency of  $2.09\text{ MHz}$ .

<sup>6</sup> ADuC842/ADuC843 machine cycle time is nominally defined as  $1/\text{Core\_CLK}$ .

Parameter ADuC841 CLOCK INPUT (External Clock Driven XTAL1)		Variable External Crystal			Unit
		Min	Typ	Max	
$t_{CK}$	XTAL1 Period	62.5		1000	ns
$t_{CKL}$	XTAL1 Width Low	20			ns
$t_{CKH}$	XTAL1 Width High	20			ns
$t_{CKR}$	XTAL1 Rise Time			20	ns
$t_{CKF}$	XTAL1 Fall Time			20	ns
$1/t_{CORE}$	ADuC841 Core Clock Frequency	0.131		20	MHz
$t_{CORE}$	ADuC841 Core Clock Period		0.476		$\mu\text{s}$
$t_{CYC}$	ADuC841 Machine Cycle Time	0.05	0.476	7.63	$\mu\text{s}$

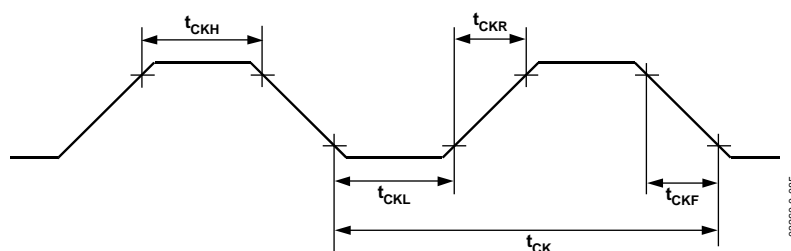


Figure 86. XTAL1 Input

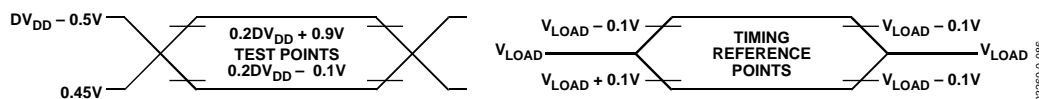


Figure 87. Timing Waveform Characteristics

Parameter		Min	Max	Unit
<b>I<sup>2</sup>C COMPATIBLE INTERFACE TIMING</b>				
$t_L$	SCLOCK Low Pulse Width	1.3		$\mu s$
$t_H$	SCLOCK High Pulse Width	0.6		$\mu s$
$t_{SHD}$	Start Condition Hold Time	0.6		$\mu s$
$t_{DSU}$	Data Setup Time	100		$\mu s$
$t_{DHD}$	Data Hold Time		0.9	$\mu s$
$t_{RSU}$	Setup Time for Repeated Start	0.6		$\mu s$
$t_{PSU}$	Stop Condition Setup Time	0.6		$\mu s$
$t_{BUF}$	Bus Free Time between a Stop Condition and a Start Condition	1.3		$\mu s$
$t_R$	Rise Time of Both SCLOCK and SDATA		300	ns
$t_F$	Fall Time of Both SCLOCK and SDATA		300	ns
$t_{SUP}^1$	Pulse Width of Spike Suppressed		50	ns

<sup>1</sup>Input filtering on both the SCLOCK and SDATA inputs suppresses noise spikes less than 50 ns.

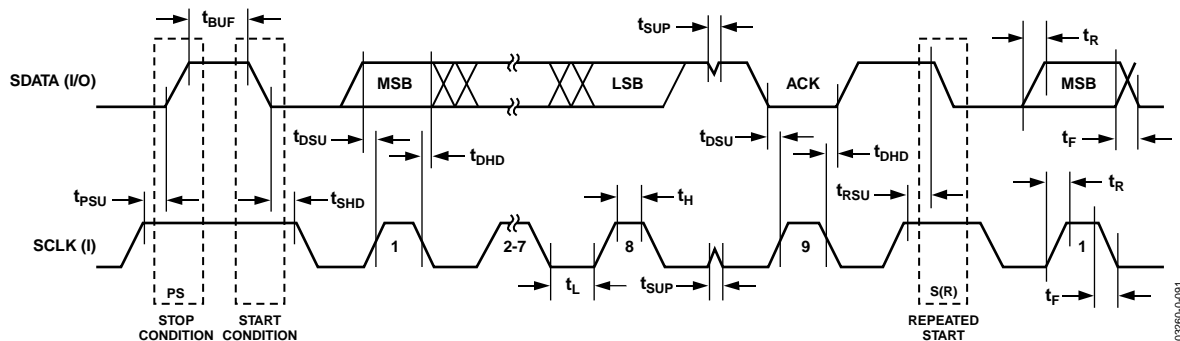


Figure 90. I<sup>2</sup>C Compatible Interface Timing

Parameter		Min	Typ	Max	Unit
<b>SPI SLAVE MODE TIMING (CPHA = 1)</b>					
$t_{SS}$	$\overline{SS}$ to SCLOCK Edge	0			ns
$t_{SL}$	SCLOCK Low Pulse Width		330		ns
$t_{SH}$	SCLOCK High Pulse Width		330		ns
$t_{DAV}$	Data Output Valid after SCLOCK Edge			50	ns
$t_{DSU}$	Data Input Setup Time before SCLOCK Edge	100			ns
$t_{DHD}$	Data Input Hold Time after SCLOCK Edge	100			ns
$t_{DF}$	Data Output Fall Time		10	25	ns
$t_{DR}$	Data Output Rise Time		10	25	ns
$t_{SR}$	SCLOCK Rise Time		10	25	ns
$t_{SF}$	SCLOCK Fall Time		10	25	ns
$t_{SFS}$	$\overline{SS}$ High after SCLOCK Edge	0			ns

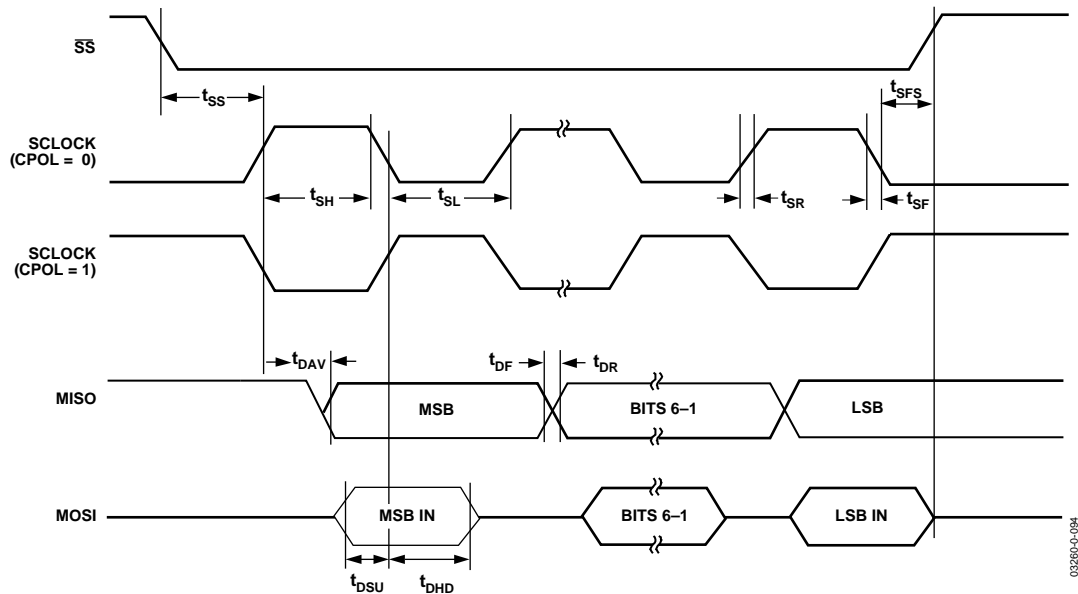


Figure 93. SPI Slave Mode Timing (CPHA = 1)