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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, PSM, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	80-PQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc841bsz62-5

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions/Comments
LOGIC INPUTS[4]				
INPUT VOLTAGES				
All Inputs Except SCLOCK, SDATA, RESET, and XTAL1				
VINL, Input Low Voltage	0.8	0.4	V max	
VINH, Input High Voltage	2.0	2.0	V min	
SDATA				
VINL, Input Low Voltage	0.8	0.8	V max	
VINH, Input High Voltage	2.0	2.0	V min	
SCLOCK and RESET ONLY[4]				
(Schmitt-Triggered Inputs)				
V_{T+}	1.3	0.95	V min	
	3.0	0.25	V max	
V_{T-}	0.8	0.4	V min	
	1.4	1.1	V max	
$V_{T+} - V_{T-}$	0.3	0.3	V min	
	0.85	0.85	V max	
CRYSTAL OSCILLATOR				
Logic Inputs, XTAL1 Only				
V_{INL}, Input Low Voltage	0.8	0.4	V typ	
V_{INH}, Input High Voltage	3.5	2.5	V typ	
XTAL1 Input Capacitance	18	18	pF typ	
XTAL2 Output Capacitance	18	18	pF typ	
MCU CLOCK RATE	16.78	8.38	MHz max	ADuC842/ADuC843 Only
	20	8.38	MHz max	ADuC841 Only
DIGITAL OUTPUTS				
Output High Voltage (V_{OH})	2.4		V min	V_{DD} = 4.5 V to 5.5 V
	4		V typ	I_{SOURCE} = 80 µA
		2.4	V min	V_{DD} = 2.7 V to 3.3 V
		2.6	V typ	I_{SOURCE} = 20 µA
Output Low Voltage (V_{OL})				
ALE, Ports 0 and 2	0.4	0.4	V max	I_{SINK} = 1.6 mA
	0.2	0.2	V typ	I_{SINK} = 1.6 mA
Port 3	0.4	0.4	V max	I_{SINK} = 4 mA
SCLOCK/SDATA	0.4	0.4	V max	I_{SINK} = 8 mA, I^2C Enabled
Floating State Leakage Current[4]	±10	±10	µA max	
	±1	±1	µA typ	
STARTUP TIME				At any core CLK
At Power-On	500	500	ms typ	
From Idle Mode	100	100	µs typ	
From Power-Down Mode				
Wake-up with $\overline{INT0}$ Interrupt	150	400	µs typ	
Wake-up with SPI/I^2C Interrupt	150	400	µs typ	
Wake-up with External RESET	150	400	µs typ	
After External RESET in Normal Mode	30	30	ms typ	
After WDT Reset in Normal Mode	3	3	ms typ	Controlled via WDCON SFR

ABSOLUTE MAXIMUM RATINGS

Table 2. T_A = 25°C, unless otherwise noted

Parameter	Rating
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
DV_{DD} to DGND, AV_{DD} to AGND	−0.3 V to +7 V
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial ADuC841BS, ADuC842BS, ADuC843BS, ADuC841BCP, ADuC842BCP, ADuC843BCP	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (ADuC84xBS)	90°C/W
θ_{JA} Thermal Impedance (ADuC84xBCP)	52°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

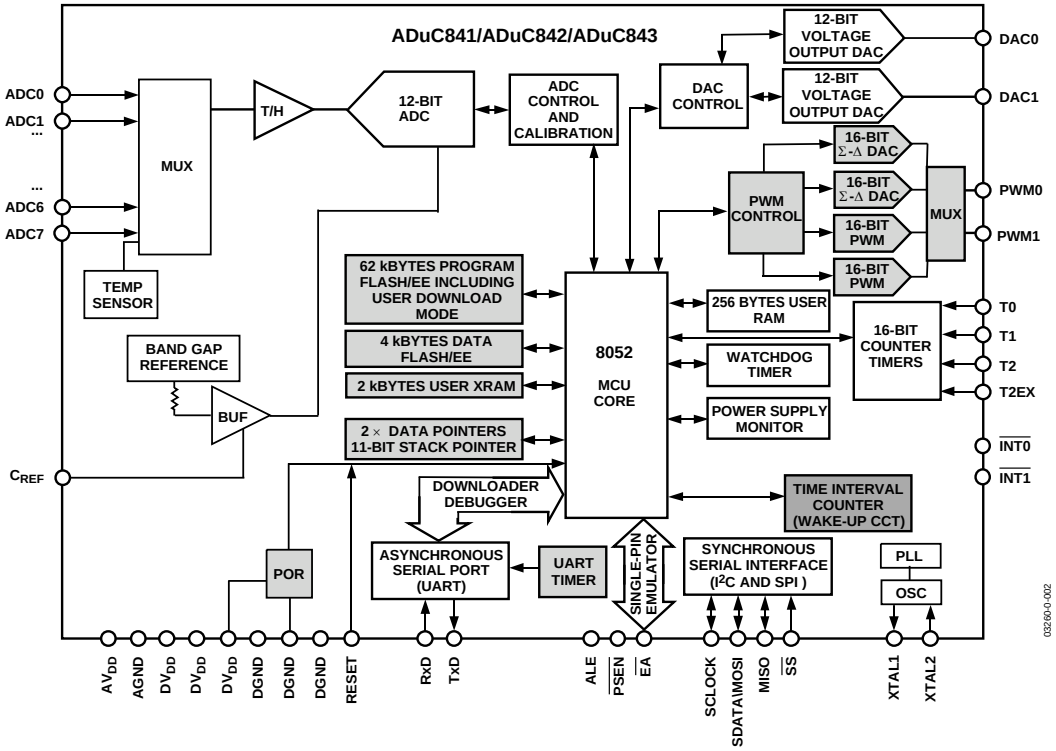

Figure 2. ADuC841/ADuC842/ADuC843 Block Diagram (Shaded Areas are Features Not Present on the ADuC812), No DACs on ADuC843, PLL on ADuC842/ADuC843 Only.

Pin No.	Mnemonic	Type[1]	Description
22	P3.4/T0/PWMC/PWM0/EXTCLK	I/O	Input/Output Port 3 (P3.4). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. Timer/Counter 0 Input (T0). PWM Clock Input (PWMC). PWM 0 Voltage Output (PWM0). PWM outputs can be configured to use Port 2.6 and Port 2.7 or Port 3.4 and Port 3.3. Input for External Clock Signal (EXTCLK). This pin function must be enabled via the CFG842 register.
23	P3.5/T1/$\overline{\text{CONVST}}$	I/O	Input/Output Port 3 (P3.5). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. Timer/Counter 1 Input (T1). Active Low Convert Start Logic Input for the ADC Block When the External Convert Start Function is Enabled ($\overline{\text{CONVST}}$). A low to high transition on this input puts the track-and-hold into hold mode and starts the conversion.
24	P3.6/$\overline{\text{WR}}$	I/O	Input/Output Port 3 (P3.6). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. Write Control Signal, Logic Output ($\overline{\text{WR}}$). Latches the data byte from Port 0 into the external data memory.
25	P3.7/$\overline{\text{RD}}$	I/O	Input/Output Port 3 (P3.7). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. Read Control Signal, Logic Output ($\overline{\text{RD}}$). Enables the external data memory to Port 0.
26	SCLOCK	I/O	Serial Clock Pin for I^2C-Compatible Clock or for SPI Serial Interface Clock.
27	SDATA/MOSI	I/O	User Selectable, I^2C Compatible, or SPI Data Input/Output Pin (SDATA). SPI Master Output/Slave Input Data I/O Pin for SPI Interface (MOSI).
28	P2.0/A8/A16	I/O	Input/Output Port 2 (P2.0). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A8). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A16). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
29	P2.1/A9/A17	I/O	Input/Output Port 2 (P2.1). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A9). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A17). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
30	P2.2/A10/A18	I/O	Input/Output Port 2 (P2.2). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A10). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A18). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.

Pin No.	Mnemonic	Type[1]	Description
31	P2.3/A11/A19	I/O	Input/Output Port 2 (P2.3). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A11). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A19). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
32	XTAL1	I	Input to the Inverting Oscillator Amplifier.
33	XTAL2	O	Output of the Inverting Oscillator Amplifier.
36	P2.4/A12/A20	I/O	Input/Output Port 2 (P2.4). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A12). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A20). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
37	P2.5/A13/A21	I/O	Input/Output Port 2 (P2.5). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A13). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A21). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
38	P2.6/PWM0/A14/A22	I/O	Input/Output Port 2 (P2.6). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. PWM 0 Voltage Output (PWM0). PWM outputs can be configured to use Port 2.6 and Port 2.7 or Port 3.4 and Port 3.3. External Memory Addresses (A14). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A22). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
39	P2.7/PWM1/A15/A23	I/O	Input/Output Port 2 (P2.7). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. PWM 1 Voltage Output (PWM1). See the CFG841/CFG842 register for further information. External Memory Addresses (A15). Port 2 emits the middle-order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A23). Port 2 emits the high-order address bytes during accesses to the external 24-bit external data memory space.
40	$\overline{EA}$	I	External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations. The devices do not support external code memory. Do not leave this pin floating.
41	$\overline{PSEN}$	O	Program Store Enable, Logic Output. This pin remains low during internal program execution. $\overline{PSEN}$ enables serial download mode when pulled low through a resistor on power-up or reset. On reset, this pin momentarily becomes an input and the status of the pin is sampled. If there is no pull-down resistor in place, the pin goes momentarily high and then user code executes. If a pull-down resistor is in place, the embedded serial download/debug kernel executes.
42	ALE	O	Address Latch Enable, Logic Output. This output latches the low byte and page byte for 24-bit address space accesses of the address into external data memory.

Pin No.	Mnemonic	Type[1]	Description
33	P2.3/A11/A19	I/O	Input/Output Port 2 (P2.3). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A11). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A19). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
34	XTAL1	I	Input to the Inverting Oscillator Amplifier.
35	XTAL2	O	Output of the Inverting Oscillator Amplifier.
39	P2.4/A12/A20	I/O	Input/Output Port 2 (P2.4). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A12). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A20). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
40	P2.5/A13/A21	I/O	Input/Output Port 2 (P2.5). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A13). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A21). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
41	P2.6/A14/A22	I/O	Input/Output Port 2 (P2.6). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A14). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A22). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
42	P2.7/A15/A23	I/O	Input/Output Port 2 (P2.7). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A15). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A23). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
43	$\overline{EA}$	I	External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations. The devices do not support external code memory. Do not leave this pin floating.
44	$\overline{PSEN}$	O	Program Store Enable, Logic Output. This pin remains low during internal program execution. $\overline{PSEN}$ enables serial download mode when pulled low through a resistor on power-up or reset. On reset, this pin momentarily becomes an input and the status of the pin is sampled. If there is no pull-down resistor in place, the pin goes momentarily high and then user code executes. If a pull-down resistor is in place, the embedded serial download/debug kernel executes.
45	ALE	O	Address Latch Enable, Logic Output. This output latches the low byte and page byte for 24-bit address space accesses of the address into external data memory.

Pin No.	Mnemonic	Type[1]	Description
46	P0.0/A0	I/O	Input/Output Port 0 (P0.0). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A0). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-ups when emitting 1s.
47	P0.1/A1	I/O	Input/Output Port 0 (P0.1). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A1). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
48	P0.2/A2	I/O	Input/Output Port 0 (P0.2). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A2). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
49	P0.3/A3	I/O	Input/Output Port 0 (P0.3). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A3). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
52	P0.4/A4	I/O	Input/Output Port 0 (P0.4). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A4). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
53	P0.5/A5	I/O	Input/Output Port 0 (P0.5). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A5). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
54	P0.6/A6	I/O	Input/Output Port 0 (P0.6). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A6). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
55	P0.7/A7	I/O	Input/Output Port 0 (P0.7). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A7). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
56	P1.0/ADC0/T2	I	Input Port 1 (P1.0). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit. Single-Ended Analog Input (ADC0). Channel selection is via ADCCON2 SFR. Timer 2 Digital Input (T2). Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1-to-0 transition of the T2 input.
	EPAD		Exposed Pad. The LFCSP has an exposed pad that must be soldered to the metal plate on the printed circuit board (PCB) for mechanical reasons and to DGND.

[1] P = power, G = ground, I = input, O = output, and NC = no connect.

ADCCON3—(ADC Control SFR 3)

The ADCCON3 register controls the operation of various calibration modes and also indicates the ADC busy status.

SFR Address	F5H
SFR Power-On Default	00H
Bit Addressable	No

Table 10. ADCCON3 SFR Bit Designations

Bit No.	Name	Description
7	BUSY	ADC Busy Status Bit. A read-only status bit that is set during a valid ADC conversion or during a calibration cycle. Busy is automatically cleared by the core at the end of conversion or calibration.
6	RSVD	Reserved. This bit should always be written as 0.
5	AVGS1	Number of Average Selection Bits.
4	AVGS0	This bit selects the number of ADC readings that are averaged during a calibration cycle. AVGS1 AVGS0 Number of Averages 0 0 15 0 1 1 1 0 31 1 1 63
3	RSVD	Reserved. This bit should always be written as 0.
2	RSVD	This bit should always be written as 1 by the user when performing calibration.
1	TYPICAL	Calibration Type Select Bit. This bit selects between offset (zero-scale) and gain (full-scale) calibration. Set to 0 for offset calibration. Set to 1 for gain calibration.
0	SCAL	Start Calibration Cycle Bit. When set, this bit starts the selected calibration cycle. It is automatically cleared when the calibration cycle is completed.

Table 12. Some Single-Supply Op Amps

Op Amp Model	Characteristics
OP281/OP481	Micropower
OP191/OP291/OP491	I/O Good up to V_{DD}, Low Cost
OP196/OP296/OP496	I/O to V_{DD}, Micropower, Low Cost
OP183/OP283	High Gain-Bandwidth Product
OP162/OP262/OP462	High GBP, Micro Package
AD820/AD822/AD824	FET Input, Low Cost
AD823	FET Input, High GBP

Keep in mind that the ADC transfer function is 0 V to V_{REF}, and that any signal range lost to amplifier saturation near ground impacts dynamic range. Though the op amps in Table 12 are capable of delivering output signals that very closely approach ground, no amplifier can deliver signals all the way to ground when powered by a single supply. Therefore, if a negative supply is available, you might consider using it to power the front end amplifiers. If you do, however, be sure to include the Schottky diodes shown in Figure 31 (or at least the lower of the two diodes) to protect the analog input from undervoltage conditions. To summarize this section, use the circuit in Figure 31 to drive the analog input pins of the parts.

Voltage Reference Connections

The on-chip 2.5 V band gap voltage reference can be used as the reference source for the ADC and DACs. To ensure the accuracy of the voltage reference, you must decouple the C_{REF} pin to ground with a 0.47 µF capacitor, as shown in Figure 32. Note that this is different from the ADuC812/ADuC831/ADuC832.

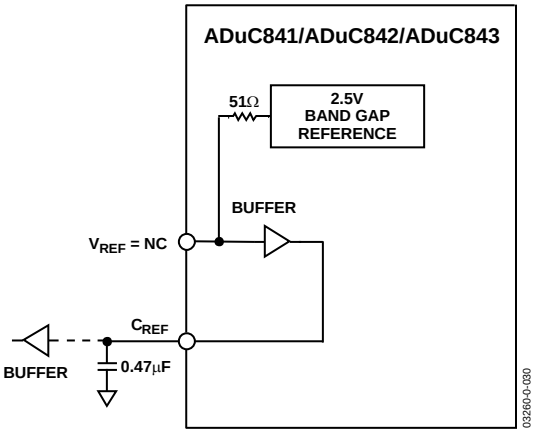

Figure 32. Decoupling V_{REF} and C_{REF}

If the internal voltage reference is to be used as a reference for external circuitry, the C_{REF} output should be used. However, a buffer must be used in this case to ensure that no current is drawn from the C_{REF} pin itself. The voltage on the C_{REF} pin is that of an internal node within the buffer block, and its voltage is critical for ADC and DAC accuracy. The parts power up with their internal voltage reference in the off state.

If an external voltage reference is preferred, it should be connected to the C_{REF} pin as shown in Figure 33. Bit 6 of the ADCCON1 SFR must be set to 1 to switch in the external reference voltage.

To ensure accurate ADC operation, the voltage applied to C_{REF} must be between 1 V and AV_{DD}. In situations where analog input signals are proportional to the power supply (such as in some strain gage applications), it may be desirable to connect the C_{REF} pin directly to AV_{DD}. Operation of the ADC or DACs with a reference voltage below 1 V, however, may incur loss of accuracy, eventually resulting in missing codes or non-monotonicity. For that reason, do not use a reference voltage lower than 1 V.

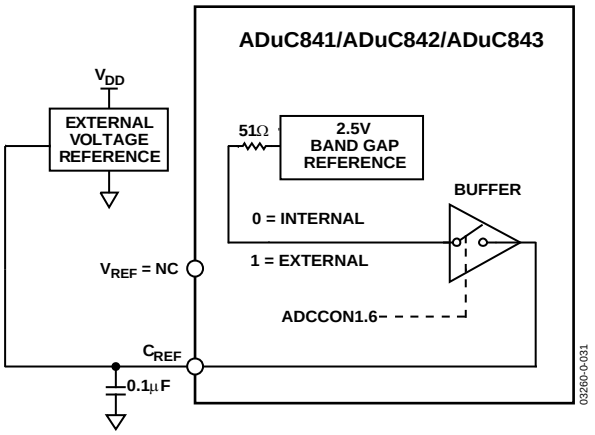

Figure 33. Using an External Voltage Reference

Configuring the ADC

The parts' successive approximation ADC is driven by a divided down version of the master clock. To ensure adequate ADC operation, this ADC clock must be between 400 kHz and 8.38 MHz. Frequencies within this range can be achieved easily with master clock frequencies from 400 kHz to well above 16 MHz, with the four ADC clock divide ratios to choose from. For example, set the ADC clock divide ratio to 8 (that is, ADCCLK = 16.777216 MHz/8 = 2 MHz) by setting the appropriate bits in ADCCON1 (ADCCON1.5 = 1, ADCCON1.4 = 0). The total ADC conversion time is 15 ADC clocks, plus 1 ADC clock for synchronization, plus the selected acquisition time (1, 2, 3, or 4 ADC clocks). For the preceding example, with a 3-clock acquisition time, total conversion time is 19 ADC clocks (or 9.05 µs for a 2 MHz ADC clock).

In continuous conversion mode, a new conversion begins each time the previous one finishes. The sample rate is then simply the inverse of the total conversion time described previously. In the preceding example, the continuous conversion mode sample rate is 110.3 kHz.

CFG841	**ADuC841 Config SFR**
SFR Address	AFH
Power-On Default	10H[1]
Bit Addressable	No

Table 15. CFG841 SFR Bit Designations

Bit No.	Name	Description
7	EXSP	Extended SP Enable. When set to 1 by the user, the stack rolls over from SPH/SP = 00FFH to 0100H. When set to 0 by the user, the stack rolls over from SP = FFH to SP = 00H.
6	PWPO	PWM Pin Out Selection. Set to 1 by the user to select P3.4 and P3.3 as the PWM output pins. Set to 0 by the user to select P2.6 and P2.7 as the PWM output pins.
5	DBUF	DAC Output Buffer. Set to 1 by the user to bypass the DAC output buffer. Set to 0 by the user to enable the DAC output buffer.
4	EPM2	Flash/EE Controller and PWM Clock Frequency Configuration Bits. Frequency should be configured such that F_{OSC}/Divide Factor = 32 kHz + 50%.
3	EPM1	EPM2 EPM1 EPM0 Divide Factor
2	EPM0	0 0 0 32 0 0 1 64 0 1 0 128 0 1 1 256 1 0 0 512 1 0 1 1024
1	MSPI	Set to 1 by the user to move the SPI functionality of MISO, MOSI, and SCLOCK to P3.3, P3.4, and P3.5, respectively. Set to 0 by the user to leave the SPI functionality as usual on MISO, MOSI, and SCLOCK pins.
0	XRAMEN	XRAM Enable Bit. When set to 1 by the user, the internal XRAM is mapped into the lower two kBytes of the external address space. When set to 0 by the user, the internal XRAM is not accessible, and the external data memory is mapped into the lower two kBytes of external data memory.

[1] Note that the Flash/EE controller bits EPM2, EPM1, EPM0 are set to their correct values depending on the crystal frequency at power-up. The user should not modify these bits so all instructions to the CFG841 register should use the ORL, XRL, or ANL instructions. Value of 10H is for 11.0592 MHz crystal.

Using the DAC

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier, the functional equivalent of which is illustrated in Figure 42. Features of this architecture include inherent guaranteed monotonicity and excellent differential linearity.

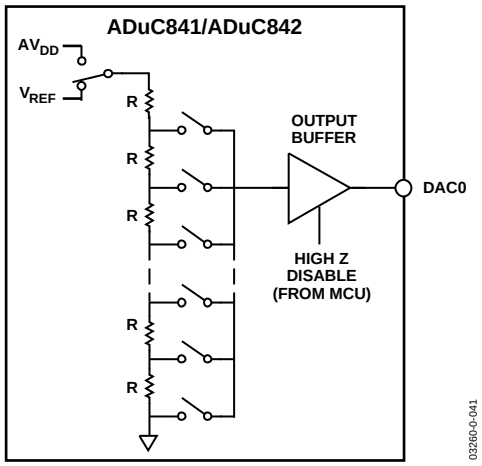

Figure 42. Resistor String DAC Functional Equivalent

As shown in Figure 42, the reference source for each DAC is user selectable in software. It can be either AV_{DD} or V_{REF}. In 0 V-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0 V-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal V_{REF} or, if an external reference is applied, the voltage at the C_{REF} pin. The DAC output buffer amplifier features a true rail-to-rail output stage implementation. This means that unloaded, each output is capable of swinging to within less than 100 mV of both AVDD and ground. Moreover, the DAC's linearity specification (when driving a 10 kΩ resistive load to ground) is guaranteed through the full transfer function except Codes 0 to 100, and, in 0 V-to-AVDD mode only, Codes 3995 to 4095. Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 43. The dotted line in Figure 43 indicates the ideal transfer function, and the solid line represents what the transfer function might look like with endpoint nonlinearities due to saturation of the output amplifier. Note that Figure 43 represents a transfer function in 0 V-to-V_{DD} mode only. In 0 V-to-V_{REF} mode (with $V_{REF} < V_{DD}$), the lower nonlinearity would be similar, but the upper portion of the transfer function would follow the ideal line right to the end (V_{REF} in this case, not V_{DD}), showing no signs of endpoint linearity errors.

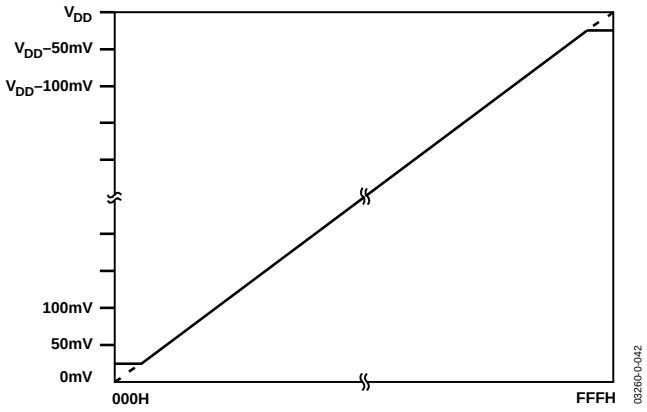

Figure 43. Endpoint Nonlinearities Due to Amplifier Saturation

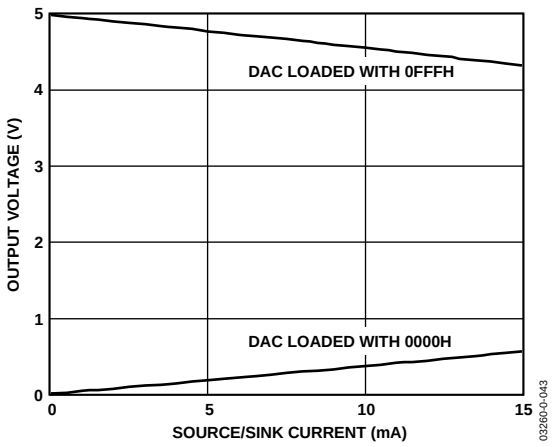

Figure 44. Source and Sink Current Capability with $V_{REF} = V_{DD} = 5$ V

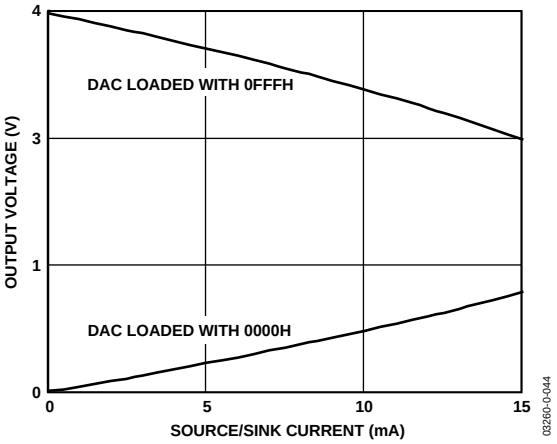

Figure 45. Source and Sink Current Capability with $V_{REF} = V_{DD} = 3$ V

POWER SUPPLY MONITOR

As its name suggests, the power supply monitor, once enabled, monitors the DV_{DD} supply on the ADuC841/ADuC842/ADuC843. It indicates when any of the supply pins drops below one of two user selectable voltage trip points, 2.93 V and 3.08 V. For correct operation of the power supply monitor function, AV_{DD} must be equal to or greater than 2.7 V. Monitor function is controlled via the PSMCON SFR. If enabled via the IEIP2 SFR, the monitor interrupts the core using the PSMI bit in the PSMCON SFR. This bit is not cleared until the failing power supply has returned above the trip point for at least 250 ms. This monitor function allows the user to save working registers to avoid possible data loss due to the low supply condition, and also ensures that normal code execution does not resume until a safe supply level has been well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

Note that the 5 V part has an internal POR trip level of 4.5 V, which means that there are no usable PSM levels on the 5 V part. The 3 V part has a POR trip level of 2.45 V, allowing all PSM trip points to be used.

PSMCON	**Power Supply Monitor Control Register**
SFR Address	DFH
Power-On Default	DEH
Bit Addressable	No

Table 23. PSMCON SFR Bit Designations

Bit No.	Name	Description
7	----	Reserved.
6	CMPD	DV_{DD} Comparator Bit. This is a read-only bit that directly reflects the state of the DV_{DD} comparator. Read 1 indicates that the DV_{DD} supply is above its selected trip point. Read 0 indicates that the DV_{DD} supply is below its selected trip point.
5	PSMI	Power Supply Monitor Interrupt Bit. This bit is set high by the MicroConverter if either CMPA or CMPD is low, indicating low analog or digital supply. The PSMI bit can be used to interrupt the processor. Once CMPD and/or CMPA return (and remain) high, a 250 ms counter is started. When this counter times out, the PSMI interrupt is cleared. PSMI can also be written by the user. However, if either comparator output is low, it is not possible for the user to clear PSMI.
4	TPD1	DV_{DD} Trip Point Selection Bits.
3	TPD0	These bits select the DV_{DD} trip point voltage as follows: TPD1 TPD0 Selected DV_{DD} Trip Point (V) 0 0 Reserved 0 1 3.08 1 0 2.93 1 1 Reserved
2	----	Reserved.
1	----	Reserved.
0	PSMEN	Power Supply Monitor Enable Bit. Set to 1 by the user to enable the power supply monitor circuit. Cleared to 0 by the user to disable the power supply monitor circuit.

WATCHDOG TIMER

The purpose of the watchdog timer is to generate a device reset or interrupt within a reasonable amount of time if the ADuC841/ADuC842/ADuC843 enter an erroneous state, possibly due to a programming error or electrical noise. The watchdog function can be disabled by clearing the WDE (watchdog enable) bit in the watchdog control (WDCON) SFR. When enabled, the watchdog circuit generates a system reset or interrupt (WDS) if the user program fails to set the watchdog (WDE) bit within a predetermined amount of time (see PRE3-0 bits in Table 24. The watchdog timer is clocked directly from the 32 kHz external crystal on the ADuC842/ADuC843. On the ADuC841, the watchdog timer is clocked by an internal R/C oscillator at 32 kHz ±10%. The WDCON SFR can be written only by user software if the double write sequence described in WDWR below is initiated on every write access to the WDCON SFR.

WDCON Watchdog Timer	Control Register
SFR Address	C0H
Power-On Default	10H
Bit Addressable	Yes

Table 24. WDCON SFR Bit Designations

Bit No.	Name	Description
7	PRE3	Watchdog Timer Prescale Bits.
6	PRE2	The watchdog timeout period is given by the equation $t_{WD} = (2^{PRE} \times (2^9/f_{XTAL}))$
5	PRE1	(0 – PRE – 7; f_{XTAL} = 32.768 kHz (ADuC842/ADuC843), or 32kHz ± 10% (ADuC841))
4	PRE0	PRE3 PRE2 PRE1 PRE0 Timeout Period (ms) Action 0 0 0 0 15.6 Reset or Interrupt 0 0 0 1 31.2 Reset or Interrupt 0 0 1 0 62.5 Reset or Interrupt 0 0 1 1 125 Reset or Interrupt 0 1 0 0 250 Reset or Interrupt 0 1 0 1 500 Reset or Interrupt 0 1 1 0 1000 Reset or Interrupt 0 1 1 1 2000 Reset or Interrupt 1 0 0 0 0.0 Immediate Reset PRE3–0 > 1000 Reserved
3	WDIR	Watchdog Interrupt Response Enable Bit. If this bit is set by the user, the watchdog generates an interrupt response instead of a system reset when the watchdog timeout period has expired. This interrupt is not disabled by the CLR $\overline{EA}$ instruction, and it is also a fixed, high priority interrupt. If the watchdog is not being used to monitor the system, it can be used alternatively as a timer. The prescaler is used to set the timeout period in which an interrupt is generated.
2	WDS	Watchdog Status Bit. Set by the watchdog controller to indicate that a watchdog timeout has occurred. Cleared by writing a 0 or by an external hardware reset. It is not cleared by a watchdog reset.
1	WDE	Watchdog Enable Bit. Set by the user to enable the watchdog and clear its counters. If this bit is not set by the user within the watchdog timeout period, the watchdog generates a reset or interrupt, depending on WDIR. Cleared under the following conditions: user writes 0, watchdog reset (WDIR = 0); hardware reset; PSM interrupt.

0	WDWR	Watchdog Write Enable Bit.
		To write data to the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and the very next instruction must be a write instruction to the WDCON SFR.
		For example:
		`CLR EA ;disable interrupts while writing`
		`;to WDT`
		`SETB WDWR ;allow write to WDCON`
		`MOV WDCON,#72H ;enable WDT for 2.0s timeout`
		`SETB EA ;enable interrupts again (if rqd)`

In general-purpose I/O port mode, Port 2 pins that have 1s written to them are pulled high by the internal pull-ups (Figure 60) and, in that state, can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. Port 2 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 1.6 mA.

P2.6 and P2.7 can also be used as PWM outputs. When they are selected as the PWM outputs via the CFG841/CFG842 SFR, the PWM outputs overwrite anything written to P2.6 or P2.7.

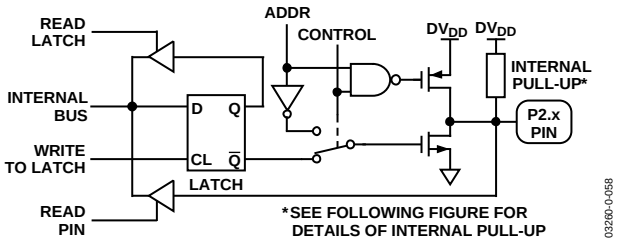

Figure 59. Port 2 Bit Latch and I/O Buffer

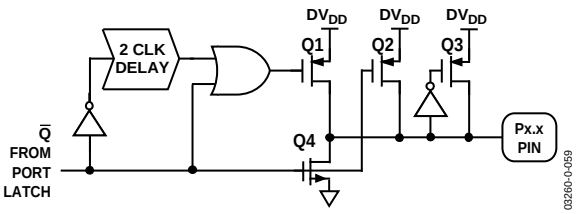

Figure 60. Internal Pull-Up Configuration

Port 3

Port 3 is a bidirectional port with internal pull-ups directly controlled via the P3 SFR. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and, in that state, can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-ups.

Port 3 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 4 mA. Port 3 pins also have various secondary functions as described in Table 27. The alternate functions of Port 3 pins can be activated only if the corresponding bit latch in the P3 SFR contains a 1. Otherwise, the port pin is stuck at 0.

Table 27. Port 3 Alternate Pin Functions

Pin No.	Alternate Function
P3.0	RxD (UART Input Pin) (or Serial Data I/O in Mode 0)
P3.1	TxD (UART Output Pin) (or Serial Clock Output in Mode 0)
P3.2	$\overline{INT0}$ (External Interrupt 0)
P3.3	$\overline{INT1}$ (External Interrupt 1)/PWM 1/MISO
P3.4	T0 (Timer/Counter 0 External Input) PWM External Clock/PWM 0
P3.5	T1 (Timer/Counter 1 External Input)
P3.6	$\overline{WR}$ (External Data Memory Write Strobe)
P3.7	$\overline{RD}$ (External Data Memory Read Strobe)

P3.3 and P3.4 can also be used as PWM outputs. When they are selected as the PWM outputs via the CFG841/CFG842 SFR, the PWM outputs overwrite anything written to P3.4 or P3.3.

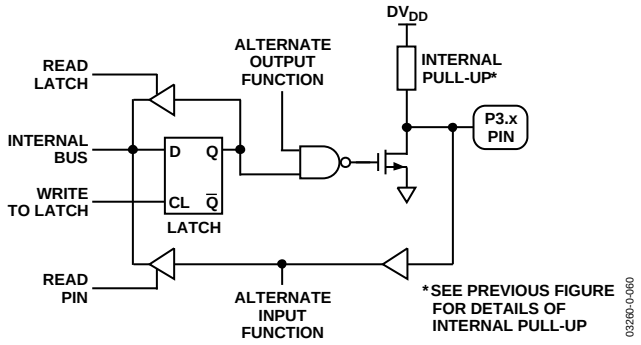

Figure 61. Port 3 Bit Latch and I/O Buffer

Additional Digital I/O

In addition to the port pins, the dedicated SPI/I²C pins (SCLOCK and SDATA/MOSI) also feature both input and output functions. Their equivalent I/O architectures are illustrated in Figure 62 and Figure 64, respectively, for SPI operation and in Figure 63 and Figure 65 for I²C operation. Notice that in I²C mode (SPE = 0), the strong pull-up FET (Q1) is disabled, leaving only a weak pull-up (Q2) present. By contrast, in SPI mode (SPE = 1) the strong pull-up FET (Q1) is controlled directly by SPI hardware, giving the pin push-pull capability.

In I²C mode (SPE = 0), two pull-down FETs (Q3 and Q4) operate in parallel to provide an extra 60% or 70% of current sinking capability. In SPI mode (SPE = 1), however, only one of the pull-down FETs (Q3) operates on each pin, resulting in sink capabilities identical to that of Port 0 and Port 2 pins. On the input path of SCLOCK, notice that a Schmitt trigger conditions the signal going to the SPI hardware to prevent false triggers (double triggers) on slow incoming edges. For incoming signals from the SCLOCK and SDATA pins going to I²C hardware, a filter conditions the signals to reject glitches of up to 50 ns in duration.

Notice also that direct access to the SCLOCK and SDATA/MOSI pins is afforded through the SFR interface in I²C master mode. Therefore, if you are not using the SPI or I²C functions, you can use these two pins to give additional high current digital outputs.

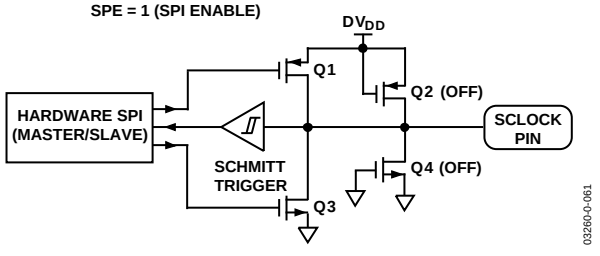

Figure 62. SCLOCK Pin I/O Functional Equivalent in SPI Mode

TIMER/COUNTER 0 AND 1 OPERATING MODES

The following sections describe the operating modes for Timer/Counters 0 and 1. Unless otherwise noted, assume that these modes of operation are the same for both Timer 0 and Timer 1.

Mode 0 (13-Bit Timer/Counter)

Mode 0 configures an 8-bit timer/counter. Figure 66 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single-cycle core.

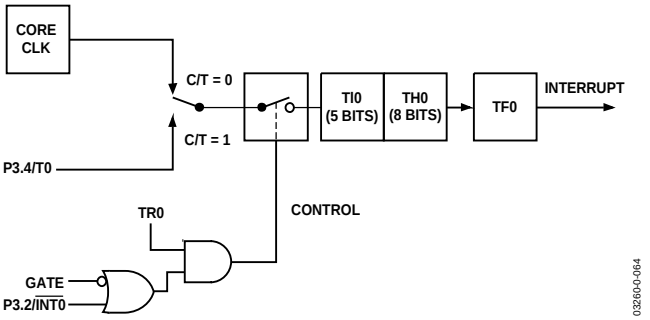

Figure 66. Timer/Counter 0, Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulse-width measurements. TR0 is a control bit in the special function register TCON; Gate is in TMOD. The 13-bit register consists of all 8 bits of TH0 and the lower five bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the Mode 1 timer register is running with all 16 bits. Mode 1 is shown in Figure 67.

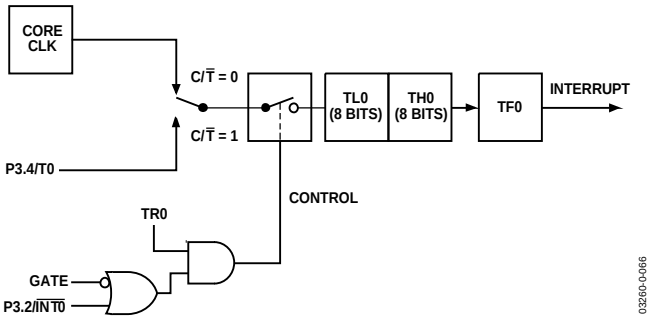

Figure 67. Timer/Counter 0, Mode 1

Mode 2 (8-Bit Timer/Counter with Autoreload)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload, as shown in Figure 68. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

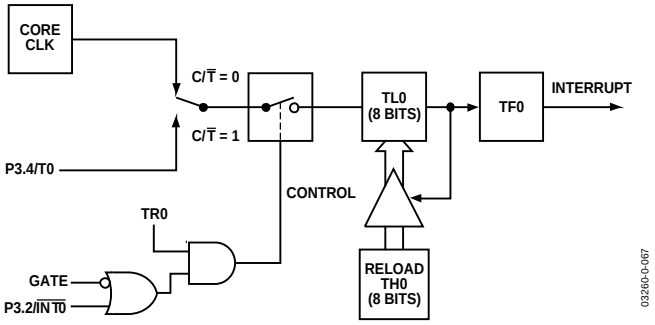

Figure 68. Timer/Counter 0, Mode 2

Mode 3 (Two 8-Bit Timer/Counters)

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 69. TL0 uses the Timer 0 control bits: C/$\overline{T}$, Gate, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can still be used by the serial interface as a baud rate generator. In fact, it can be used in any application not requiring an interrupt from Timer 1 itself.

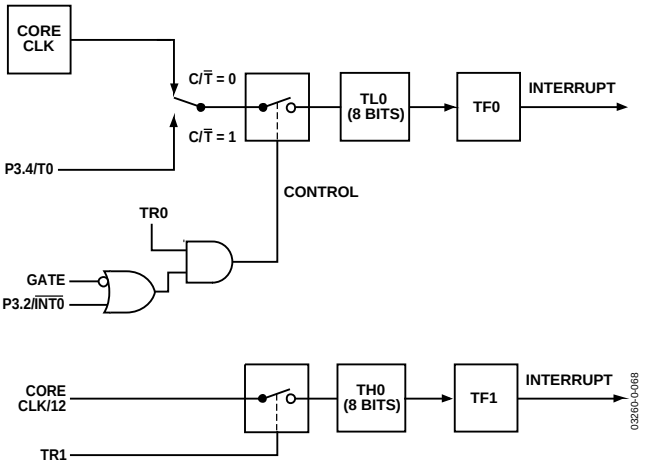

Figure 69. Timer/Counter 0, Mode 3

T2CON	Timer/Counter 2 Control Register
SFR Address	C8H
Power-On Default	00H
Bit Addressable	Yes

Table 31. T2CON SFR Bit Designations

Bit No.	Name	Description
7	TF2	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 cannot be set when either RCLK = 1 or TCLK = 1. Cleared by user software.
6	EXF2	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. Cleared by user software.
5	RCLK	Receive Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the receive clock.
4	TCLK	Transmit Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the transmit clock.
3	EXEN2	Timer 2 External Enable Flag. Set by the user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by the user for Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 Start/Stop Control Bit. Set by the user to start Timer 2. Cleared by the user to stop Timer 2.
1	CNT2	Timer 2 Timer or Counter Function Select Bit. Set by the user to select counter function (input from external T2 pin). Cleared by the user to select timer function (input from on-chip core clock).
0	CAP2	Timer 2 Capture/Reload Select Bit. Set by the user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by the user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Timer/Counter 2 Data Registers

Timer/Counter 2 also has two pairs of 8-bit data registers associated with it. These are used as both timer data registers and as timer capture/reload registers.

TH2 and TL2

Timer 2, data high byte and low byte.
SFR Address = CDH, CCH, respectively.

RCAP2H and RCAP2L

Timer 2, capture/reload byte and low byte.
SFR Address = CBH, CAH, respectively.

INTERRUPT SYSTEM

The ADuC841/ADuC842/ADuC843 provide a total of nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

IE	Interrupt Enable Register
IP	Interrupt Priority Register
IEIP2	Secondary Interrupt Enable Register

IE	**Interrupt Enable Register**
SFR Address	A8H
Power-On Default	00H
Bit Addressable	Yes

Table 36. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Set by the user to enable, or cleared to disable all interrupt sources.
6	EADC	Set by the user to enable, or cleared to disable ADC interrupts.
5	ET2	Set by the user to enable, or cleared to disable Timer 2 interrupts.
4	ES	Set by the user to enable, or cleared to disable UART serial port interrupts.
3	ET1	Set by the user to enable, or cleared to disable 0 Timer 1 interrupts.
2	EX1	Set by the user to enable, or cleared to disable External Interrupt 1.
1	ET0	Set by the user to enable, or cleared to disable Timer 0 interrupts.
0	EX0	Set by the user to enable, or cleared to disable External Interrupt 0 .

IP	**Interrupt Priority Register**
SFR Address	B8H
Power-On Default	00H
Bit Addressable	Yes

Table 37. IP SFR Bit Designations

Bit No.	Name	Description
7	----	Reserved.
6	PADC	Written by the user to select the ADC interrupt priority (1 = High; 0 = Low).
5	PT2	Written by the user to select the Timer 2 interrupt priority (1 = High; 0 = Low).
4	PS	Written by the user to select the UART serial port interrupt priority (1 = High; 0 = Low).
3	PT1	Written by the user to select the Timer 1 interrupt priority (1 = High; 0 = Low).
2	PX1	Written by the user to select External Interrupt 1 priority (1 = High; 0 = Low).
1	PT0	Written by the user to select the Timer 0 interrupt priority (1 = High; 0 = Low).
0	PX0	Written by the user to select External Interrupt 0 priority (1 = High; 0 = Low).

IEIP2	Secondary Interrupt Enable Register
SFR Address	A9H
Power-On Default	A0H
Bit Addressable	No

Table 38. IEIP2 SFR Bit Designations

Bit No.	Name	Description
7	----	Reserved.
6	PTI	Priority for time interval interrupt.
5	PPSM	Priority for power supply monitor interrupt.
4	PSI	Priority for SPI/I²C interrupt.
3	----	This bit must contain zero.
2	ETI	Set by the user to enable, or cleared to disable time interval counter interrupts.
1	EPSMI	Set by the user to enable, or cleared to disable power supply monitor interrupts.
0	ESI	Set by the user to enable, or cleared to disable SPI or I²C serial port interrupts.

Interrupt Priority

The interrupt enable registers are written by the user to enable individual interrupt sources, while the interrupt priority registers allow the user to select one of two priority levels for each interrupt. An interrupt of a high priority may interrupt the service routine of a low priority interrupt, and if two interrupts of different priority occur at the same time, the higher level interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed as shown in Table 39.

Table 39. Priority within an Interrupt Level

Source	Priority	Description
PSMI	1 (Highest)	Power Supply Monitor Interrupt.
WDS	2	Watchdog Timer Interrupt.
IE0	2	External Interrupt 0.
ADCI	3	ADC Interrupt.
TF0	4	Timer/Counter 0 Interrupt.
IE1	5	External Interrupt 1.
TF1	6	Timer/Counter 1 Interrupt.
ISPI/I2CI	7	SPI Interrupt/I²C Interrupt.
RI + TI	8	Serial Interrupt.
TF2 + EXF2	9	Timer/Counter 2 Interrupt.
TII	11(Lowest)	Time Interval Counter Interrupt.

Interrupt Vectors

When an interrupt occurs, the program counter is pushed onto the stack, and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown in Table 40.

Table 40. Interrupt Vector Addresses

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH
ADCI	0033H
ISPI/I2CI	003BH
PSMI	0043H
TII	0053H
WDS	005BH

HARDWARE DESIGN CONSIDERATIONS

This section outlines some of the key hardware design considerations that must be addressed when integrating the ADuC841/ADuC842/ADuC843 into any hardware system.

Clock Oscillator

The clock source for the parts can be generated by the internal PLL or by an external clock input. To use the internal PLL, connect a 32.768 kHz parallel resonant crystal between XTAL1 and XTAL2, and connect a capacitor from each pin to ground as shown in Figure 75. The parts contain an internal capacitance of 18 pF on the XTAL1 and XTAL2 pins, which is sufficient for most watch crystals. This crystal allows the PLL to lock correctly to give an f_{VCO} of 16.777216 MHz. If no crystal is present, the PLL free runs, giving an fVCO of 16.7 MHz ±20%. In this mode, the CD bits are limited to CD = 1, giving a max core clock of 8.38 MHz. This is useful if an external clock input is required. The part powers up and the PLL free runs; the user then writes to the CFG842 SFR in software to enable the external clock input on P3.4. Note that double the required clock must be provided externally since the part runs at CD = 1. A better solution is to use the ADuC841 with the external clock.

For the ADuC841, connect the crystal in the same manner; external capacitors should be connected as per the crystal manufacturer's recommendations. A minimum capacitance of 20 pF is recommended on XTAL1 and XTAL2. The ADuC841 does not operate if no crystal is present.

An external clock may be connected as shown in Figure 76 and Figure 77.

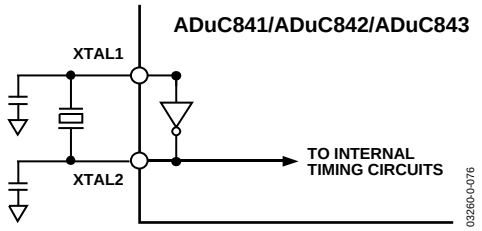

Figure 75. External Parallel Resonant Crystal Connections

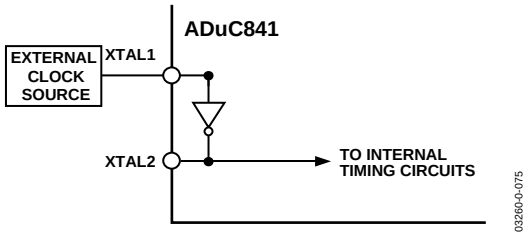

Figure 76. Connecting an External Clock Source (ADuC841)

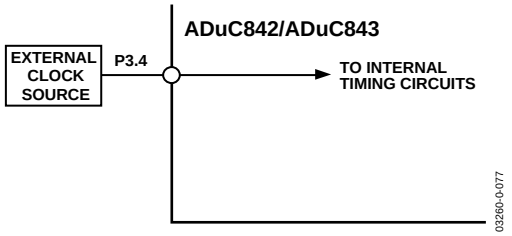

Figure 77. Connecting an External Clock Source (ADuC842/ADuC843)

Whether using the internal PLL or an external clock source, the specified operational clock speed range of the devices is 400 kHz to 16.777216 MHz, (20 MHz, ADuC841). The core itself is static, and functions all the way down to dc. But at clock speeds slower that 400 kHz, the ADC can no longer function correctly. Therefore, to ensure specified operation, use a clock frequency of at least 400 kHz and no more than 20 MHz.

External Memory Interface

In addition to its internal program and data memories, the parts can access up to 16 MBytes of external data memory (SRAM). Note that the parts cannot access external program memory.

Figure 78 shows a hardware configuration for accessing up to 64 kBytes of external RAM. This interface is standard to any 8051 compatible MCU.

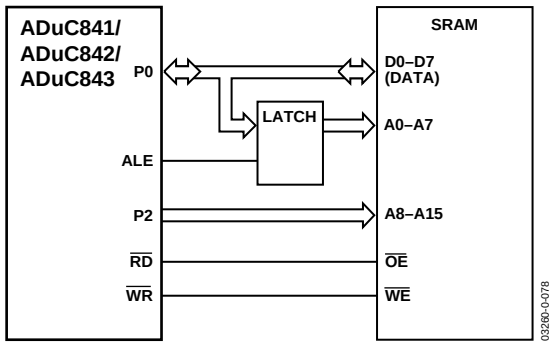

Figure 78. External Data Memory Interface (64 kBytes Address Space)

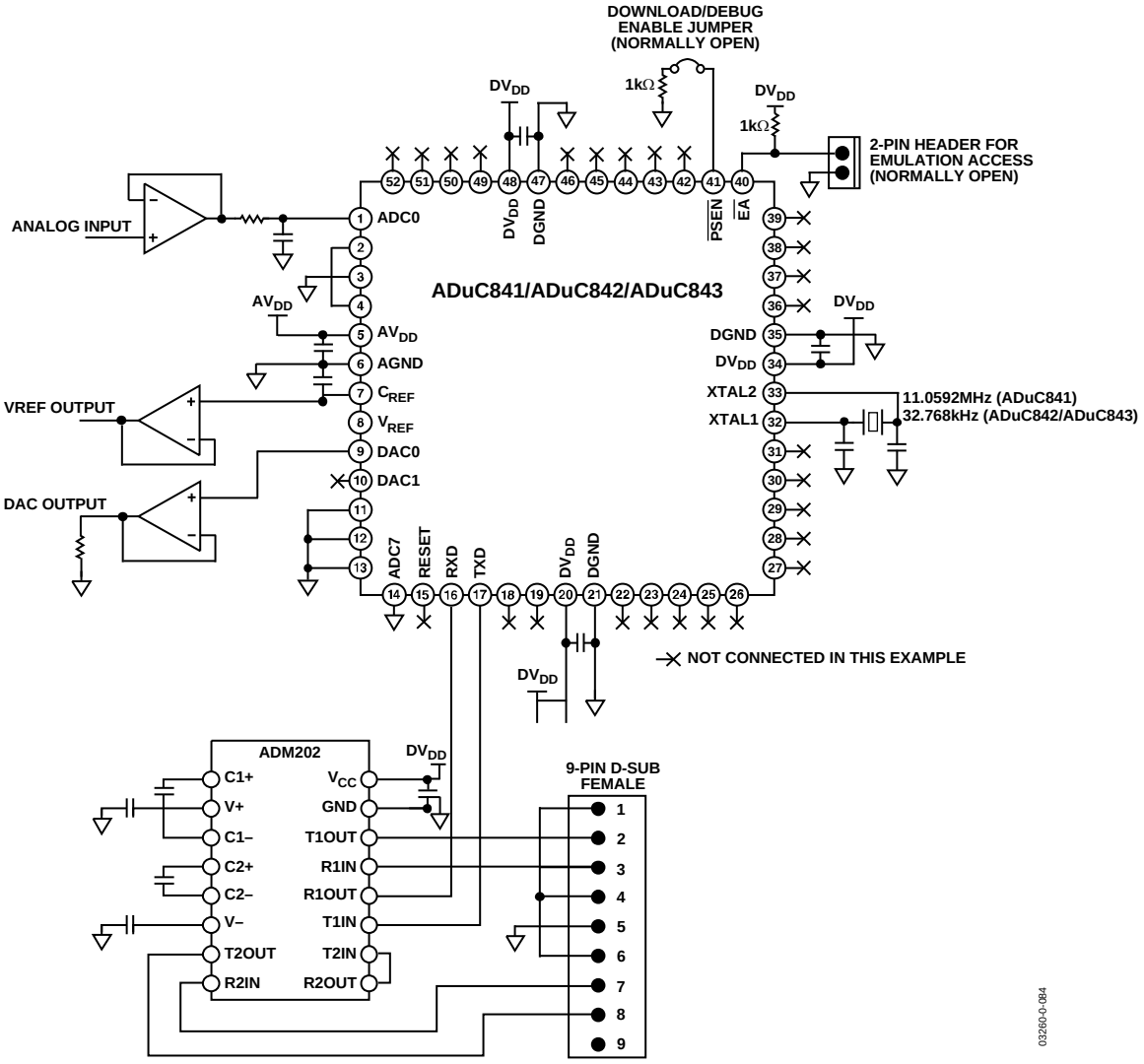

Figure 85. Example System (PQFP Package), DACs Not Present on ADuC843

OTHER HARDWARE CONSIDERATIONS

To facilitate in-circuit programming, plus in-circuit debug and emulation options, users need to implement some simple connection points in their hardware to allow easy access to download, debug, and emulation modes.

In-Circuit Serial Download Access

Nearly all ADuC841/ADuC842/ADuC843 designs want to take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the ADuC841/ADuC842/ADuC843's UART, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is illustrated in Figure 85 with a simple ADM202 based circuit. If users would rather not design an RS-232 chip onto a board, refer to Application Note uC006, *A 4-Wire UART-to-PC Interface*, (at www.analog.com/microconverter) for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the part.

In addition to the basic UART connections, users also need a way to trigger the chip into download mode. This is accomplished via a 1 kΩ pull-down resistor that can be jumpered onto the $\overline{\text{PSEN}}$ pin, as shown in Figure 85. To get the part into download mode, simply connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available), and it is then ready to serially receive a new program. With the jumper removed, the device comes up in normal mode (and runs the program) whenever power is cycled or RESET is toggled.

TIMING SPECIFICATIONS[1, 2, 3]

Table 42. AV_{DD} =2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted

Parameter		32.768 kHz External Crystal			
ADuC842/ADuC843 **CLOCK INPUT** (External Clock Driven XTAL1)		**Min**	**Typ**	**Max**	**Unit**
t_{CK}	XTAL1 Period		30.52		µs
t_{CKL}	XTAL1 Width Low		6.26		µs
t_{CKH}	XTAL1 Width High		6.26		µs
t_{CKR}	XTAL1 Rise Time		9		ns
t_{CKF}	XTAL1 Fall Time		9		ns
$1/t_{CORE}$	ADuC842/ADuC843 Core Clock Frequency[4]	0.131		16.78	MHz
t_{CORE}	ADuC842/ADuC843 Core Clock Period[5]		0.476		µs
t_{CYC}	ADuC842/ADuC843 Machine Cycle Time[6]	0.059	0.476	7.63	µs

[1] AC inputs during testing are driven at DV_{DD} – 0.5 V for a Logic 1 and 0.45 V for Logic 0. Timing measurements are made at V_{IH} min for Logic 1 and V_{IL} max for Logic 0, as shown in Figure 87.
[2] For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs, as shown in Figure 87.
[3] C_{LOAD} for all outputs = 80 pF, unless otherwise noted.
[4] ADuC842/ADuC843 internal PLL locks onto a multiple (512 times) of the 32.768 kHz external crystal frequency to provide a stable 16.78 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.
[5] This number is measured at the default Core_Clk operating frequency of 2.09 MHz.
[6] ADuC842/ADuC843 machine cycle time is nominally defined as 1/Core_CLK.

Parameter		Variable External Crystal			
ADuC841 CLOCK INPUT (External Clock Driven XTAL1)		**Min**	**Typ**	**Max**	**Unit**
t_{CK}	XTAL1 Period	62.5		1000	ns
t_{CKL}	XTAL1 Width Low	20			ns
t_{CKH}	XTAL1 Width High	20			ns
t_{CKR}	XTAL1 Rise Time			20	ns
t_{CKF}	XTAL1 Fall Time			20	ns
$1/t_{CORE}$	ADuC841 Core Clock Frequency	0.131		20	MHz
t_{CORE}	ADuC841 Core Clock Period		0.476		µs
t_{CYC}	ADuC841 Machine Cycle Time	0.05	0.476	7.63	µs

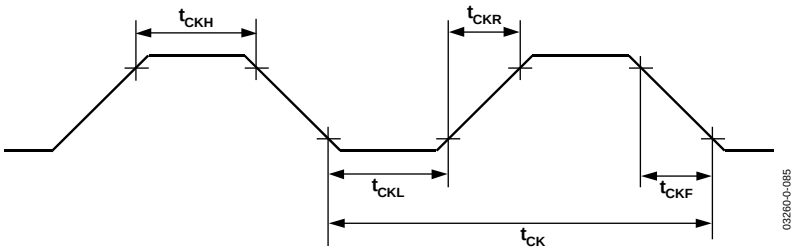

Figure 86. XTAL1 Input

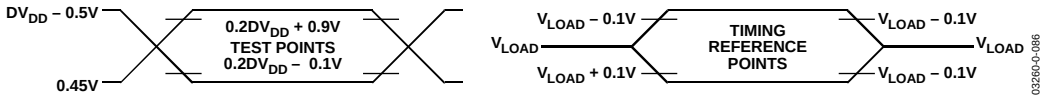

Figure 87. Timing Waveform Characteristics