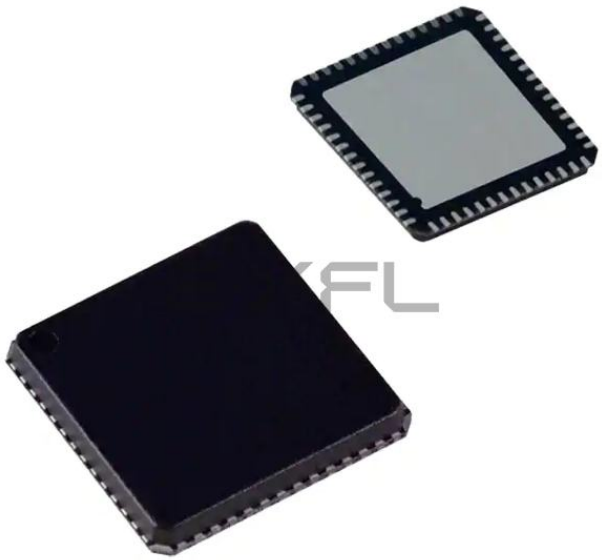

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8052 |
| Core Size | 8-Bit |
| Speed | 8.38MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | DMA, PSM, PWM, Temp Sensor, WDT |
| Number of I/O | 32 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2.25K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 56-VFQFN Exposed Pad, CSP |
| Supplier Device Package | 56-LFCSP-VQ (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/aduc842bcpz8-3 |

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## REVISION HISTORY

**4/16—Rev. 0 to Rev. A**

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Added Table 4; Renumbered Sequentially ... 14
Changes to Using the DAC Section ... 47
Updated Outline Dimensions ... 94
Changes to Ordering Guide ... 95

**11/03—Revision 0: Initial Version**

# SPECIFICATIONS[1]

**Table 1. $AV_{DD}$ = $DV_{DD}$ = 2.7 V to 3.6 V or 4.75 V to 5.25 V; $V_{REF}$ = 2.5 V internal reference, $f_{CORE}$ = 16.78 MHz @ 5 V 8.38 MHz @ 3 V; all specifications $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted**

| Parameter | $V_{DD}$ = 5 V | $V_{DD}$ = 3 V | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| **ADC CHANNEL SPECIFICATIONS** | | | | |
| DC ACCURACY[2, 3] | | | | $f_{SAMPLE}$ = 120 kHz, see the Typical Performance Characteristics for typical performance at other values of $f_{SAMPLE}$ |
| Resolution | 12 | 12 | Bits | |
| Integral Nonlinearity | ±1 | ±1 | LSB max | 2.5 V internal reference |
| | ±0.3 | ±0.3 | LSB typ | |
| Differential Nonlinearity | +1/−0.9 | +1/−0.9 | LSB max | 2.5 V internal reference |
| | ±0.3 | ±0.3 | LSB typ | |
| Integral Nonlinearity[4] | ±2 | ±1.5 | LSB max | 1 V external reference |
| Differential Nonlinearity[4] | +1.5/−0.9 | +1.5/−0.9 | LSB max | 1 V external reference |
| Code Distribution | 1 | 1 | LSB typ | ADC input is a dc voltage |
| CALIBRATED ENDPOINT ERRORS[5, 6] | | | | |
| Offset Error | ±3 | ±2 | LSB max | |
| Offset Error Match | ±1 | ±1 | LSB typ | |
| Gain Error | ±3 | ±2 | LSB max | |
| Gain Error Match | ±1 | ±1 | LSB typ | |
| DYNAMIC PERFORMANCE | | | | $f_{IN}$ = 10 kHz sine wave<br>$f_{SAMPLE}$ = 120 kHz |
| Signal-to-Noise Ratio (SNR)[7] | 71 | 71 | dB typ | |
| Total Harmonic Distortion (THD) | −85 | −85 | dB typ | |
| Peak Harmonic or Spurious Noise | −85 | −85 | dB typ | |
| Channel-to-Channel Crosstalk[8] | −80 | −80 | dB typ | |
| ANALOG INPUT | | | | |
| Input Voltage Range | 0 to $V_{REF}$ | 0 to $V_{REF}$ | V | |
| Leakage Current | ±1 | ±1 | µA max | |
| Input Capacitance | 32 | 32 | pF typ | |
| TEMPERATURE SENSOR[9] | | | | |
| Voltage Output at 25°C | 700 | 700 | mV typ | |
| Voltage TC | −1.4 | −1.4 | mV/°C typ | |
| Accuracy | ±1.5 | ±1.5 | °C typ | Internal/External 2.5 V $V_{REF}$ |
| **DAC CHANNEL SPECIFICATIONS**<br>**Internal Buffer Enabled**<br>ADuC841/ADuC842 **Only** | | | | DAC load to AGND<br>$R_L$ = 10 kΩ, $C_L$ = 100 pF |
| DC ACCURACY[10] | | | | |
| Resolution | 12 | 12 | Bits | |
| Relative Accuracy | ±3 | ±3 | LSB typ | |
| Differential Nonlinearity[11] | −1 | −1 | LSB max | Guaranteed 12-bit monotonic |
| | ±1/2 | ±1/2 | LSB typ | |
| Offset Error | ±50 | ±50 | mV max | $V_{REF}$ range |
| Gain Error | ±1 | ±1 | % max | $AV_{DD}$ range |
| | ±1 | ±1 | % typ | $V_{REF}$ range |
| Gain Error Mismatch | 0.5 | 0.5 | % typ | % of full-scale on DAC1 |
| ANALOG OUTPUTS | | | | |
| Voltage Range_0 | 0 to $V_{REF}$ | 0 to $V_{REF}$ | V typ | DAC $V_{REF}$ = 2.5 V |
| Voltage Range_1 | 0 to $V_{DD}$ | 0 to $V_{DD}$ | V typ | DAC $V_{REF}$ = $V_{DD}$ |
| Output Impedance | 0.5 | 0.5 | Ω typ | |

| Parameter | $V_{DD}$ = 5 V | $V_{DD}$ = 3 V | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| DAC AC CHARACTERISTICS | | | | |
| Voltage Output Settling Time | 15 | 15 | µs typ | Full-scale settling time to within ½ LSB of final value |
| Digital-to-Analog Glitch Energy | 10 | 10 | nV-sec typ | 1 LSB change at major carry |
| **DAC CHANNEL SPECIFICATIONS[12, 13]** | | | | |
| **Internal Buffer Disabled ADuC841/ADuC842 Only** | | | | |
| DC ACCURACY[10] | | | | |
| Resolution | 12 | 12 | Bits | |
| Relative Accuracy | ±3 | ±3 | LSB typ | |
| Differential Nonlinearity[11] | –1 | –1 | LSB max | Guaranteed 12-bit monotonic |
| | ±1/2 | ±1/2 | LSB typ | |
| Offset Error | ±5 | ±5 | mV max | $V_{REF}$ range |
| Gain Error | ±0.5 | ±0.5 | % typ | $V_{REF}$ range |
| Gain Error Mismatch[4] | 0.5 | 0.5 | % typ | % of full-scale on DAC1 |
| ANALOG OUTPUTS | | | | |
| Voltage Range_0 | 0 to $V_{REF}$ | 0 to $V_{REF}$ | V typ | DAC $V_{REF}$ = 2.5 V |
| REFERENCE INPUT/OUTPUT REFERENCE OUTPUT[14] | | | | |
| Output Voltage ($V_{REF}$) | 2.5 | 2.5 | V | |
| Accuracy | ±10 | ±10 | mV Max | Of $V_{REF}$ measured at the $C_{REF}$ pin $T_A$ = 25°C |
| Power Supply Rejection | 65 | 67 | dB typ | |
| Reference Temperature Coefficient | ±15 | ±15 | ppm/°C typ | |
| Internal $V_{REF}$ Power-On Time | 2 | 2 | ms typ | |
| EXTERNAL REFERENCE INPUT[15] | | | | |
| Voltage Range ($V_{REF}$) [4] | 1 | 1 | V min | |
| | $V_{DD}$ | $V_{DD}$ | V max | |
| Input Impedance | 20 | 20 | kΩ typ | |
| Input Leakage | 1 | 1 | µA max | Internal band gap deselected via ADCCON1.6 |
| POWER SUPPLY MONITOR (PSM) | | | | |
| $DV_{DD}$ Trip Point Selection Range | | 2.93 | V min | Two trip points selectable in this range programmed via TPD1–0 in PSMCON, 3 V part only |
| | | 3.08 | V max | |
| $DV_{DD}$ Power Supply Trip Point Accuracy | | ±2.5 | % max | |
| WATCHDOG TIMER (WDT) [4] | | | | |
| Timeout Period | 0 | 0 | ms min | Nine timeout periods selectable in this range |
| | 2000 | 2000 | ms max | |
| FLASH/EE MEMORY RELIABILITY CHARACTERISTICS[16] | | | | |
| Endurance[17] | 100,000 | 100,000 | Cycles min | |
| Data Retention[18] | 100 | 100 | Years min | |
| DIGITAL INPUTS | | | | |
| Input Leakage Current (Port 0, $\overline{EA}$) | ±10 | ±10 | µA max | $V_{IN}$ = 0 V or $V_{DD}$ |
| | ±1 | ±1 | µA typ | $V_{IN}$ = 0 V or $V_{DD}$ |
| Logic 1 Input Current | | | | |
| (All Digital Inputs), SDATA, SCLOCK | ±10 | ±10 | µA max | $V_{IN}$ = $V_{DD}$ |
| | ±1 | ±1 | µA typ | $V_{IN}$ = $V_{DD}$ |
| Logic 0 Input Current (Ports 1, 2, 3) SDATA, SCLOCK | –75 | –25 | µA max | |
| | –40 | –15 | µA typ | $V_{IL}$ = 450 mV |
| Logic 1 to Logic 0 Transition Current (Ports 2 and 3) | –660 | –250 | µA max | $V_{IL}$ = 2 V |
| | –400 | –140 | µA typ | $V_{IL}$ = 2 V |
| RESET | ±10 | ±10 | µA max | $V_{IN}$ = 0 V |
| | 10 | 5 | µA min | $V_{IN}$ = 5 V, 3 V Internal Pull Down |
| | 105 | 35 | µA max | $V_{IN}$ = 5 V, 3 V Internal Pull Down |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 22 | P3.4/T0/PWMC/PWM0/EXTCLK | I/O | Input/Output Port 3 (P3.4). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.<br>Timer/Counter 0 Input (T0).<br>PWM Clock Input (PWMC).<br>PWM 0 Voltage Output (PWM0). PWM outputs can be configured to use Port 2.6 and Port 2.7 or Port 3.4 and Port 3.3.<br>Input for External Clock Signal (EXTCLK). This pin function must be enabled via the CFG842 register. |
| 23 | P3.5/T1/$\overline{\text{CONVST}}$ | I/O | Input/Output Port 3 (P3.5). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.<br>Timer/Counter 1 Input (T1).<br>Active Low Convert Start Logic Input for the ADC Block When the External Convert Start Function is Enabled ($\overline{\text{CONVST}}$). A low to high transition on this input puts the track-and-hold into hold mode and starts the conversion. |
| 24 | P3.6/$\overline{\text{WR}}$ | I/O | Input/Output Port 3 (P3.6). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.<br>Write Control Signal, Logic Output ($\overline{\text{WR}}$). Latches the data byte from Port 0 into the external data memory. |
| 25 | P3.7/$\overline{\text{RD}}$ | I/O | Input/Output Port 3 (P3.7). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.<br>Read Control Signal, Logic Output ($\overline{\text{RD}}$). Enables the external data memory to Port 0. |
| 26 | SCLOCK | I/O | Serial Clock Pin for $I^2C$-Compatible Clock or for SPI Serial Interface Clock. |
| 27 | SDATA/MOSI | I/O | User Selectable, $I^2C$ Compatible, or SPI Data Input/Output Pin (SDATA).<br>SPI Master Output/Slave Input Data I/O Pin for SPI Interface (MOSI). |
| 28 | P2.0/A8/A16 | I/O | Input/Output Port 2 (P2.0). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors.<br>External Memory Addresses (A8). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space.<br>External Memory Addresses (A16). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space. |
| 29 | P2.1/A9/A17 | I/O | Input/Output Port 2 (P2.1). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors.<br>External Memory Addresses (A9). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space.<br>External Memory Addresses (A17). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space. |
| 30 | P2.2/A10/A18 | I/O | Input/Output Port 2 (P2.2). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors.<br>External Memory Addresses (A10). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space.<br>External Memory Addresses (A18). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 46 | P0.0/A0 | I/O | Input/Output Port 0 (P0.0). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs.<br>External Memory Address (A0). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-ups when emitting 1s. |
| 47 | P0.1/A1 | I/O | Input/Output Port 0 (P0.1). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs.<br>External Memory Address (A1). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s. |
| 48 | P0.2/A2 | I/O | Input/Output Port 0 (P0.2). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs.<br>External Memory Address (A2). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s. |
| 49 | P0.3/A3 | I/O | Input/Output Port 0 (P0.3). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs.<br>External Memory Address (A3). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s. |
| 52 | P0.4/A4 | I/O | Input/Output Port 0 (P0.4). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs.<br>External Memory Address (A4). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s. |
| 53 | P0.5/A5 | I/O | Input/Output Port 0 (P0.5). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs.<br>External Memory Address (A5). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s. |
| 54 | P0.6/A6 | I/O | Input/Output Port 0 (P0.6). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs.<br>External Memory Address (A6). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s. |
| 55 | P0.7/A7 | I/O | Input/Output Port 0 (P0.7). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs.<br>External Memory Address (A7). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s. |
| 56 | P1.0/ADC0/T2 | I | Input Port 1 (P1.0). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit.<br>Single-Ended Analog Input (ADC0). Channel selection is via ADCCON2 SFR.<br>Timer 2 Digital Input (T2). Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1-to-0 transition of the T2 input. |
| | EPAD | | Exposed Pad. The LFCSP has an exposed pad that must be soldered to the metal plate on the printed circuit board (PCB) for mechanical reasons and to DGND. |

[1] P = power, G = ground, I = input, O = output, and NC = no connect.

# TYPICAL PERFORMANCE CHARACTERISTICS

The typical performance plots presented in this section illustrate typical performance of the ADuC841/ADuC842/ADuC843 under various operating conditions.

Figure 5 and Figure 6 show typical ADC integral nonlinearity (INL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and is operating at a sampling rate of 152 kHz; the typical worst-case errors in both plots are just less than 0.3 LSB. Figure 7 and Figure 8 also show ADC INL at a higher sampling rate of 400 kHz. Figure 9 and Figure 10 show the variation in worst-case positive (WCP) INL and worst-case negative (WCN) INL versus external reference input voltage.

Figure 11 and Figure 12 show typical ADC differential nonlinearity (DNL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and is operating at a sampling rate of 152 kHz; the typical worst-case errors in both plots are just less than 0.2 LSB. Figure 13 and Figure 14 show the variation in worst-case positive (WCP) DNL and worst-case negative (WCN) DNL versus external reference input voltage.

Figure 15 shows a histogram plot of 10,000 ADC conversion results on a dc input with $V_{DD}$ = 5 V. The plot illustrates an excellent code distribution pointing to the low noise performance of the on-chip precision ADC.

Figure 16 shows a histogram plot of 10,000 ADC conversion results on a dc input for $V_{DD}$ = 3 V. The plot again illustrates a very tight code distribution of 1 LSB with the majority of codes appearing in one output pin.

Figure 17 and Figure 18 show typical FFT plots for the parts. These plots were generated using an external clock input. The ADC is using its internal reference (2.5 V), sampling a full-scale, 10 kHz sine wave test tone input at a sampling rate of 149.79 kHz. The resulting FFTs shown at 5 V and 3 V supplies illustrate an excellent 100 dB noise floor, 71 dB signal-to-noise ratio (SNR), and THD greater than –80 dB.

Figure 19 and Figure 20 show typical dynamic performance versus external reference voltages. Again, excellent ac performance can be observed in both plots with some roll-off being observed as $V_{REF}$ falls below 1 V.

Figure 21 shows typical dynamic performance versus sampling frequency. SNR levels of 71 dB are obtained across the sampling range of the parts.

Figure 22 shows the voltage output of the on-chip temperature sensor versus temperature. Although the initial voltage output at 25°C can vary from part to part, the resulting slope of −1. 4 mV/°C is constant across all parts.

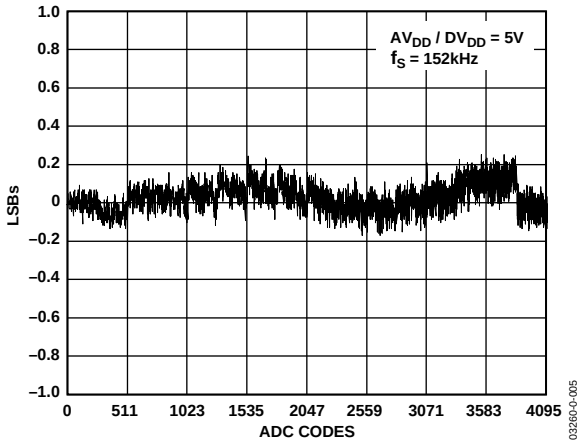


*Figure 5. Typical INL Error, $V_{DD}$ = 5 V, $f_s$ = 152 kHz*

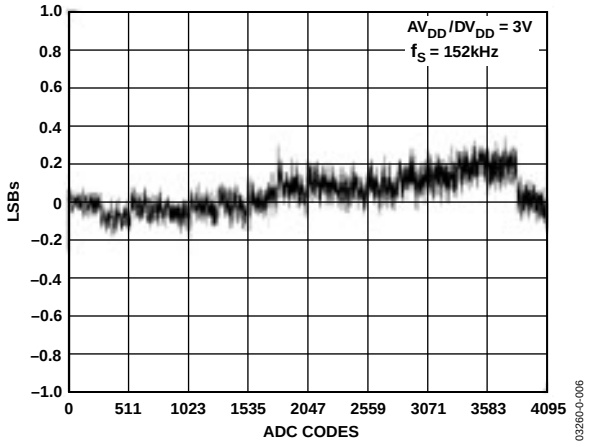


*Figure 6. Typical INL Error, $V_{DD}$ = 3 V, $f_s$ = 152 kHz*

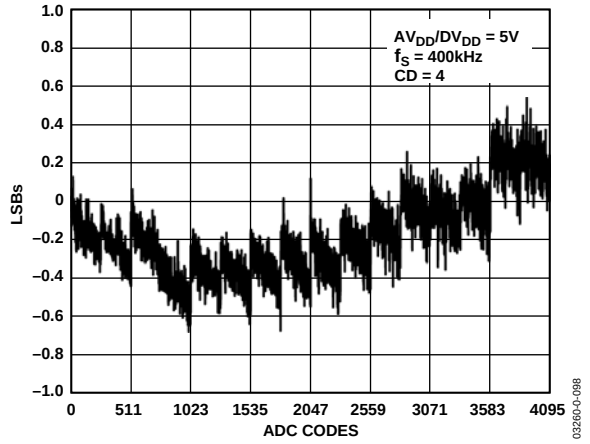


Figure 7. Typical INL Error, $V_{DD}$ = 5 V, $f_S$ = 400 kHz

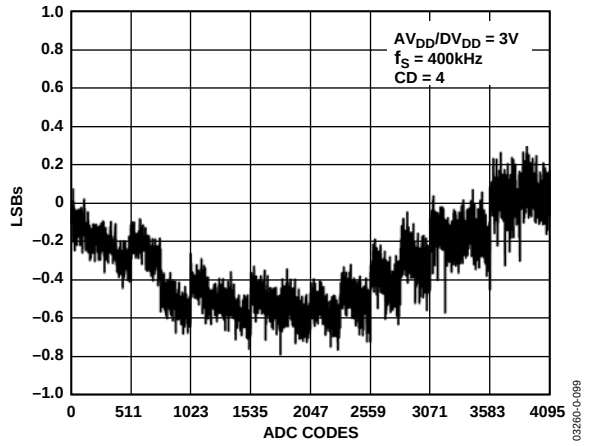


Figure 8. Typical INL Error, $V_{DD}$ = 3 V, $f_S$ = 400 kHz

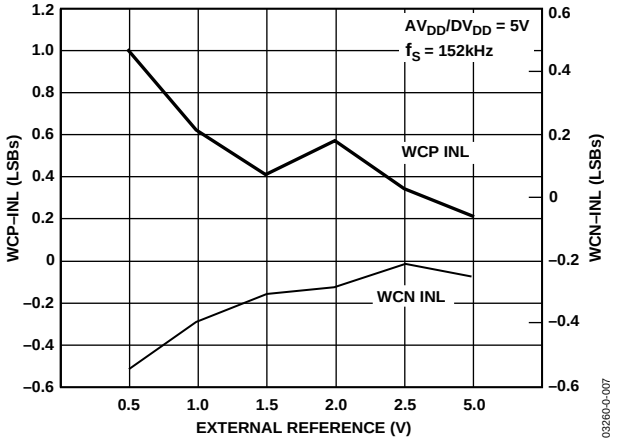


Figure 9. Typical Worst-Case INL Error vs. $V_{REF}$, $V_{DD}$ = 5 V

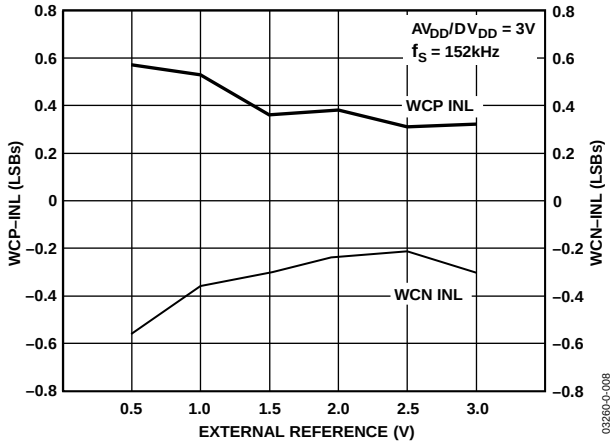


Figure 10. Typical Worst-Case INL Error vs. $V_{REF}$, $V_{DD}$ = 3 V

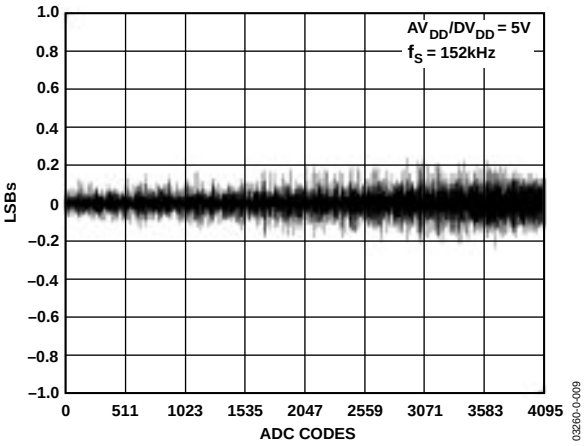


Figure 11. Typical DNL Error, $V_{DD}$ = 5 V

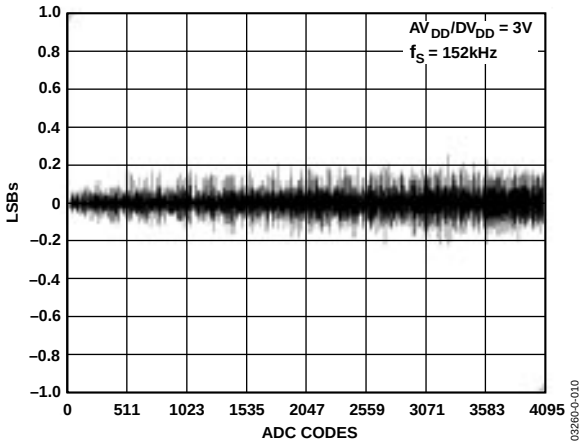


Figure 12. Typical DNL Error, $V_{DD}$ = 3 V

# FUNCTIONAL DESCRIPTION

## 8052 INSTRUCTION SET

Table 5 documents the number of clock cycles required for each instruction. Most instructions are executed in one or two clock cycles, resulting in a 16 MIPS peak performance when operating at PLLCON = 00H on the ADuC842/ADuC843. On the ADuC841, 20 MIPS peak performance is possible with a 20 MHz external crystal.

**Table 5. Instructions**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| **Arithmetic** | | | |
| ADD A,Rn | Add register to A | 1 | 1 |
| ADD A,@Ri | Add indirect memory to A | 1 | 2 |
| ADD A,dir | Add direct byte to A | 2 | 2 |
| ADD A,#data | Add immediate to A | 2 | 2 |
| ADDC A,Rn | Add register to A with carry | 1 | 1 |
| ADDC A,@Ri | Add indirect memory to A with carry | 1 | 2 |
| ADDC A,dir | Add direct byte to A with carry | 2 | 2 |
| ADD A,#data | Add immediate to A with carry | 2 | 2 |
| SUBB A,Rn | Subtract register from A with borrow | 1 | 1 |
| SUBB A,@Ri | Subtract indirect memory from A with borrow | 1 | 2 |
| SUBB A,dir | Subtract direct from A with borrow | 2 | 2 |
| SUBB A,#data | Subtract immediate from A with borrow | 2 | 2 |
| INC A | Increment A | 1 | 1 |
| INC Rn | Increment register | 1 | 1 |
| INC @Ri | Increment indirect memory | 1 | 2 |
| INC dir | Increment direct byte | 2 | 2 |
| INC DPTR | Increment data pointer | 1 | 3 |
| DEC A | Decrement A | 1 | 1 |
| DEC Rn | Decrement register | 1 | 1 |
| DEC @Ri | Decrement indirect memory | 1 | 2 |
| DEC dir | Decrement direct byte | 2 | 2 |
| MUL AB | Multiply A by B | 1 | 9 |
| DIV AB | Divide A by B | 1 | 9 |
| DA A | Decimal adjust A | 1 | 2 |
| **Logic** | | | |
| ANL A,Rn | AND register to A | 1 | 1 |
| ANL A,@Ri | AND indirect memory to A | 1 | 2 |
| ANL A,dir | AND direct byte to A | 2 | 2 |
| ANL A,#data | AND immediate to A | 2 | 2 |
| ANL dir,A | AND A to direct byte | 2 | 2 |
| ANL dir,#data | AND immediate data to direct byte | 3 | 3 |
| ORL A,Rn | OR register to A | 1 | 1 |
| ORL A,@Ri | OR indirect memory to A | 1 | 2 |
| ORL A,dir | OR direct byte to A | 2 | 2 |
| ORL A,#data | OR immediate to A | 2 | 2 |
| ORL dir,A | OR A to direct byte | 2 | 2 |
| ORL dir,#data | OR immediate data to direct byte | 3 | 3 |
| XRL A,Rn | Exclusive-OR register to A | 1 | 1 |
| XRL A,@Ri | Exclusive-OR indirect memory to A | 2 | 2 |
| XRL A,#data | Exclusive-OR immediate to A | 2 | 2 |
| XRL dir,A | Exclusive-OR A to direct byte | 2 | 2 |

## ACCUMULATOR SFR (ACC)

ACC is the accumulator register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions refer to the accumulator as A.

### *B SFR (B)*

The B register is used with the ACC for multiplication and division operations. For other instructions, it can be treated as a general-purpose scratchpad register.

### *Stack Pointer (SP and SPH)*

The SP SFR is the stack pointer and is used to hold an internal RAM address that is called the top of the stack. The SP register is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the SP register is initialized to 07H after a reset, which causes the stack to begin at location 08H.

As mentioned earlier, the parts offer an extended 11-bit stack pointer. The 3 extra bits used to make up the 11-bit stack pointer are the 3 LSBs of the SPH byte located at B7H.

### *Data Pointer (DPTR)*

The data pointer is made up of three 8-bit registers named DPP (page byte), DPH (high byte), and DPL (low byte). These are used to provide memory addresses for internal and external code access and for external data access. They may be manipulated as a 16-bit register (DPTR = DPH, DPL), although INC DPTR instructions automatically carry over to DPP, or as three independent 8-bit registers (DPP, DPH, DPL). The parts support dual data pointers. Refer to the Dual Data Pointer section.

### *Program Status Word (PSW)*

The PSW SFR contains several bits reflecting the current status of the CPU, as detailed in Table 6.

| | |
|---|---|
| SFR Address | D0H |
| Power-On Default | 00H |
| Bit Addressable | Yes |

**Table 6. PSW SFR Bit Designations**

| Bit | Name | Description | | |
|---|---|---|---|---|
| 7 | CY | Carry Flag. | | |
| 6 | AC | Auxiliary Carry Flag. | | |
| 5 | F0 | General-Purpose Flag. | | |
| 4 | RS1 | Register Bank Select Bits. | | |
| 3 | RS0 | RS1 | RS0 | Selected Bank |
| | | 0 | 0 | 0 |
| | | 0 | 1 | 1 |
| | | 1 | 0 | 2 |
| | | 1 | 1 | 3 |
| 2 | OV | Overflow Flag. | | |
| 1 | F1 | General-Purpose Flag. | | |
| 0 | P | Parity Bit. | | |

### *Power Control SFR (PCON)*

The PCON SFR contains bits for power-saving options and general-purpose status flags, as shown in Table 7.

| | |
|---|---|
| SFR Address | 87H |
| Power-On Default | 00H |
| Bit Addressable | No |

**Table 7. PCON SFR Bit Designations**

| Bit No. | Name | Description |
|---|---|---|
| 7 | SMOD | Double UART Baud Rate. |
| 6 | SERIPD | $I^2C$/SPI Power-Down Interrupt Enable. |
| 5 | INT0PD | $\overline{INT0}$ Power-Down Interrupt Enable. |
| 4 | ALEOFF | Disable ALE Output. |
| 3 | GF1 | General-Purpose Flag Bit. |
| 2 | GF0 | General-Purpose Flag Bit. |
| 1 | PD | Power-Down Mode Enable. |
| 0 | IDL | Idle Mode Enable. |

### *ADCCON2—(ADC Control SFR 2)*

The ADCCON2 register controls ADC channel selection and conversion modes as detailed below.

| | |
|---|---|
| SFR Address | D8H |
| SFR Power-On Default | 00H |
| Bit Addressable | Yes |

**Table 9. ADCCON2 SFR Bit Designations**

| Bit No. | Name | Description |
|---|---|---|
| 7 | ADCI | ADC Interrupt Bit.<br>Set by hardware at the end of a single ADC conversion cycle or at the end of a DMA block conversion.<br>Cleared by hardware when the PC vectors to the ADC interrupt service routine. Otherwise, the ADCI bit is cleared by user code. |
| 6 | DMA | DMA Mode Enable Bit.<br>Set by the user to enable a preconfigured ADC DMA mode operation. A more detailed description of this mode is given in the ADC DMA Mode section. The DMA bit is automatically set to 0 at the end of a DMA cycle. Setting this bit causes the ALE output to cease; it starts again when DMA is started and operates correctly after DMA is complete. |
| 5 | CCONV | Continuous Conversion Bit.<br>Set by the user to initiate the ADC into a continuous mode of conversion. In this mode, the ADC starts converting based on the timing and channel configuration already set up in the ADCCON SFRs; the ADC automatically starts another conversion once a previous conversion has completed. |
| 4 | SCONV | Single Conversion Bit.<br>Set to initiate a single conversion cycle. The SCONV bit is automatically reset to 0 on completion of the single conversion cycle. |
| 3<br>2<br>1<br>0 | CS3<br>CS2<br>CS1<br>CS0 | Channel Selection Bits.<br>Allow the user to program the ADC channel selection under software control. When a conversion is initiated, the converted channel is the one pointed to by these channel selection bits. In DMA mode, the channel selection is derived from the channel ID written to the external memory. |

| CS3 | CS2 | CS1 | CS0 | CH# | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | |
| 0 | 0 | 0 | 1 | 1 | |
| 0 | 0 | 1 | 0 | 2 | |
| 0 | 0 | 1 | 1 | 3 | |
| 0 | 1 | 0 | 0 | 4 | |
| 0 | 1 | 0 | 1 | 5 | |
| 0 | 1 | 1 | 0 | 6 | |
| 0 | 1 | 1 | 1 | 7 | |
| 1 | 0 | 0 | 0 | Temp Monitor | Requires minimum of 1 µs to acquire. |
| 1 | 0 | 0 | 1 | DAC0 | Only use with internal DAC output buffer on. |
| 1 | 0 | 1 | 0 | DAC1 | Only use with internal DAC output buffer on. |
| 1 | 0 | 1 | 1 | AGND | |
| 1 | 1 | 0 | 0 | $V_{REF}$ | |
| 1 | 1 | 1 | 1 | DMA STOP | Place in XRAM location to finish DMA sequence; refer to the ADC DMA Mode section. |

All other combinations reserved.

If using the temperature sensor as the ADC input, the ADC should be configured to use an ADCCLK of MCLK/32 and four acquisition clocks.

Increasing the conversion time on the temperature monitor channel improves the accuracy of the reading. To further improve the accuracy, an external reference with low temperature drift should also be used.

### *ADC DMA Mode*

The on-chip ADC has been designed to run at a maximum conversion speed of 2.38 µs (420 kHz sampling rate). When converting at this rate, the ADuC841/ADuC842/ADuC843 MicroConverter® has 2 µs to read the ADC result and to store the result in memory for further postprocessing; otherwise the next ADC sample could be lost. In an interrupt driven routine, the MicroConverter would also have to jump to the ADC interrupt service routine, which also increases the time required to store the ADC results. In applications where the parts cannot sustain the interrupt rate, an ADC DMA mode is provided.

To enable DMA mode, Bit 6 in ADCCON2 (DMA) must be set, which allows the ADC results to be written directly to a 16 MByte external static memory SRAM (mapped into data memory space) without any interaction from the core of the part. This mode allows the part to capture a contiguous sample stream at full ADC update rates (420 kHz).

**Typical DMA Mode Configuration Example**

Setting the parts to DMA mode consists of the following steps:

1. The ADC must be powered down. This is done by ensuring that MD1 and MD0 are both set to 0 in ADCCON1.
2. The DMA address pointer must be set to the start address of where the ADC results are to be written. This is done by writing to the DMA mode address pointers DMAL, DMAH, and DMAP. DMAL must be written to first, followed by DMAH, and then by DMAP.
3. The external memory must be preconfigured. This consists of writing the required ADC channel IDs into the top four bits of every second memory location in the external SRAM, starting at the first address specified by the DMA address pointer. Because the ADC DMA mode operates independently from the ADuC841/ADuC842/ADuC843 core, it is necessary to provide it with a stop command. This is done by duplicating the last channel ID to be converted followed by 1111 into the next channel selection field. A typical preconfiguration of external memory is shown in Figure 34.

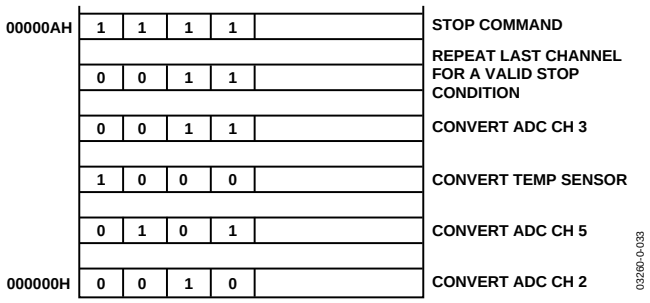


*Figure 34. Typical DMA External Memory Preconfiguration*

4. The DMA is initiated by writing to the ADC SFRs in the following sequence:
   a. ADCCON2 is written to enable the DMA mode, that is, MOV ADCCON2, #40H; DMA mode enabled.
   b. ADCCON1 is written to configure the conversion time and power-up of the ADC. It can also enable Timer 2 driven conversions or external triggered conversions if required.
   c. ADC conversions are initiated. This is done by starting single conversions, starting Timer 2, running for Timer 2 conversions, or receiving an external trigger.

When the DMA conversions are complete, the ADC interrupt bit, ADCI, is set by hardware, and the external SRAM contains the new ADC conversion results as shown in Figure 35. Note that no result is written to the last two memory locations.

When the DMA mode logic is active, it takes the responsibility of storing the ADC results away from both the user and the core logic of the part. As the DMA interface writes the results of the ADC conversions to external memory, it takes over the external memory interface from the core. Thus, any core instructions that access the external memory while DMA mode is enabled does not get access to the external memory. The core executes the instructions, and they take the same time to execute, but they cannot access the external memory.

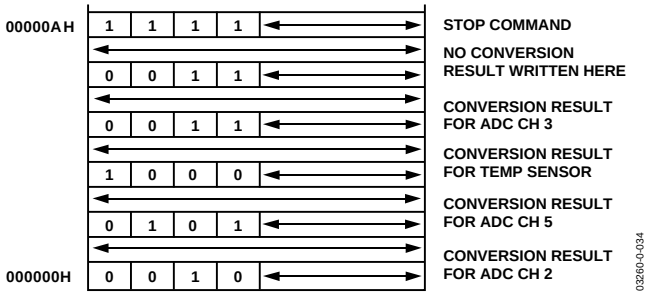


*Figure 35. Typical External Memory Configuration Post ADC DMA Operation*

### *ADuC842/ADuC843 Configuration SFR (CFG842)*

The CFG842 SFR contains the necessary bits to configure the internal XRAM, external clock select, PWM output selection, DAC buffer, and the extended SP for both the ADuC842 and the ADuC843. By default, it configures the user into 8051 mode, that is, extended SP is disabled and internal XRAM is disabled. On the ADuC841, this register is the CFG841 register and is described on the next page.

| CFG842 | ADuC842/ADuC843 Config SFR |
|---|---|
| SFR Address | AFH |
| Power-On Default | 00H |
| Bit Addressable | No |

**Table 14. CFG842 SFR Bit Designations**

| Bit No. | Name | Description |
|---|---|---|
| 7 | EXSP | Extended SP Enable.<br>When set to 1 by the user, the stack rolls over from SPH/SP = 00FFH to 0100H.<br>When set to 0 by the user, the stack rolls over from SP = FFH to SP = 00H. |
| 6 | PWPO | PWM Pin Out Selection.<br>Set to 1 by the user to select P3.4 and P3.3 as the PWM output pins.<br>Set to 0 by the user to select P2.6 and P2.7 as the PWM output pins. |
| 5 | DBUF | DAC Output Buffer.<br>Set to 1 by the user to bypass the DAC output buffer.<br>Set to 0 by the user to enable the DAC output buffer. |
| 4 | EXTCLK | Set by the user to 1 to select an external clock input on P3.4.<br>Set by the user to 0 to use the internal PLL clock. |
| 3 | RSVD | Reserved. This bit should always contain 0. |
| 2 | RSVD | Reserved. This bit should always contain 0. |
| 1 | MSPI | Set to 1 by the user to move the SPI functionality of MISO, MOSI, and SCLOCK to P3.3, P3.4, and P3.5, respectively.<br>Set to 0 by the user to leave the SPI functionality as usual on MISO, MOSI, and SCLOCK pins. |
| 0 | XRAMEN | XRAM Enable Bit.<br>When set to 1 by the user, the internal XRAM is mapped into the lower 2 kBytes of the external address space.<br>When set to 0 by the user, the internal XRAM is not accessible, and the external data memory is mapped into the lower 2 kBytes of external data memory. |

The endpoint nonlinearities illustrated in Figure 43 become worse as a function of output loading. Most of the part's specifications assume a 10 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom (respectively) of Figure 43 become larger. Larger current demands can significantly limit output voltage swing. Figure 44 and Figure 45 illustrate this behavior. Note that the upper trace in each of these figures is valid only for an output range selection of 0 V-to-$AV_{DD}$. In 0 V-to-$V_{REF}$ mode, DAC loading does not cause high-side voltage drops as long as the reference voltage remains below the upper trace in the corresponding figure. For example, if $AV_{DD}$ = 3 V and $V_{REF}$ = 2.5 V, the high-side voltage is not be affected by loads less than 5 mA. But somewhere around 7 mA, the upper curve in Figure 45 drops below 2.5 V ($V_{REF}$), indicating that at these higher currents the output is not capable of reaching $V_{REF}$.

To reduce the effects of the saturation of the output amplifier at values close to ground and to give reduced offset and gain errors, the internal buffer can be bypassed. This is done by setting the DBUF bit in the CFG841/CFG842 register. This allows a full rail-to-rail output from the DAC, which should then be buffered externally using a dual-supply op amp in order to get a rail-to-rail output. This external buffer should be located as close as physically possible to the DAC output pin on the PCB. Note that the unbuffered mode works only in the 0 V to $V_{REF}$ range.

To drive significant loads with the DAC outputs, external buffering may be required (even with the internal buffer enabled), as illustrated in Figure 46. Table 12 lists some recommended op amps.

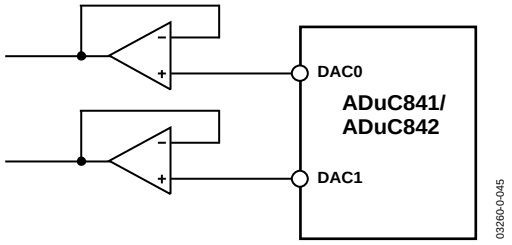


*Figure 46. Buffering the DAC Outputs*

The DAC output buffer also features a high impedance disable function. In the chip's default power-on state, both DACs are disabled, and their outputs are in a high impedance state (or three-state) where they remain inactive until enabled in software. This means that if a zero output is desired during power-up or power-down transient conditions, then a pull-down resistor must be added to each DAC output. Assuming this resistor is in place, the DAC outputs remain at ground potential whenever the DAC is disabled.

| Bit No. | Name | Description |
|---|---|---|
| 2 | I2CRS | $I^2C$ Reset Bit (Slave Mode Only).<br>Set by the user to reset the $I^2C$ interface.<br>Cleared by the user code for normal $I^2C$ operation. |
| 1 | I2CTX | $I^2C$ Direction Transfer Bit (Slave Mode Only).<br>Set by the MicroConverter if the interface is transmitting.<br>Cleared by the MicroConverter if the interface is receiving. |
| 0 | I2CI | $I^2C$ Interrupt Bit (Slave Mode Only).<br>Set by the MicroConverter after a byte has been transmitted or received.<br>Cleared automatically when user code reads the I2CDAT SFR (see I2CDAT below). |

| | |
|---|---|
| **I2CADD** | **$I^2C$ Address Register** |
| Function | Holds the first $I^2C$ peripheral address for the part. It may be overwritten by user code. Application Note uC001 at www.analog.com/microconverter describes the format of the $I^2C$ standard 7-bit address in detail. |
| SFR Address | 9BH |
| Power-On Default | 55H |
| Bit Addressable | No |
| **I2CADD1** | **$I^2C$ Address Register** |
| Function | Holds the second $I^2C$ peripheral address for the part. It may be overwritten by user code. |
| SFR Address | 91H |
| Power-On Default | 7FH |
| Bit Addressable | No |
| **I2CADD2** | **$I^2C$ Address Register** |
| Function | Holds the third $I^2C$ peripheral address for the part. It may be overwritten by user code. |
| SFR Address | 92H |
| Power-On Default | 7FH |
| Bit Addressable | No |
| **I2CADD3** | **$I^2C$ Address Register** |
| Function | Holds the fourth $I^2C$ peripheral address for the part. It may be overwritten by user code. |
| SFR Address | 93H |
| Power-On Default | 7FH |
| Bit Addressable | No |
| **I2CDAT** | **$I^2C$ Data Register** |
| Function | Written by the user to transmit data over the $I^2C$ interface or read by user code to read data just received by the $I^2C$ interface. Accessing I2CDAT automatically clears any pending $I^2C$ interrupt and the I2CI bit in the I2CCON SFR. User software should access I2CDAT only once per interrupt cycle. |
| SFR Address | 9AH |
| Power-On Default | 00H |
| Bit Addressable | No |

The main features of the MicroConverter $I^2C$ interface are

- Only two bus lines are required: a serial data line (SDATA) and a serial clock line (SCLOCK).
- An $I^2C$ master can communicate with multiple slave devices. Because each slave device has a unique 7-bit address, single master/slave relationships can exist at all times even in a multislave environment.
- Ability to respond to four separate addresses when operating in slave mode.

## WATCHDOG TIMER

The purpose of the watchdog timer is to generate a device reset or interrupt within a reasonable amount of time if the ADuC841/ADuC842/ADuC843 enter an erroneous state, possibly due to a programming error or electrical noise. The watchdog function can be disabled by clearing the WDE (watchdog enable) bit in the watchdog control (WDCON) SFR. When enabled, the watchdog circuit generates a system reset or interrupt (WDS) if the user program fails to set the watchdog (WDE) bit within a predetermined amount of time (see PRE3-0 bits in Table 24. The watchdog timer is clocked directly from the 32 kHz external crystal on the ADuC842/ADuC843. On the ADuC841, the watchdog timer is clocked by an internal R/C oscillator at 32 kHz ±10%. The WDCON SFR can be written only by user software if the double write sequence described in WDWR below is initiated on every write access to the WDCON SFR.

| WDCON Watchdog Timer | Control Register |
|---|---|
| SFR Address | C0H |
| Power-On Default | 10H |
| Bit Addressable | Yes |

**Table 24. WDCON SFR Bit Designations**

| Bit No. | Name | Description |
|---|---|---|
| 7 | PRE3 | Watchdog Timer Prescale Bits. |
| 6 | PRE2 | The watchdog timeout period is given by the equation $t_{WD} = (2^{PRE} \times (2^9/f_{XTAL}))$ |
| 5 | PRE1 | (0 – PRE – 7; $f_{XTAL}$ = 32.768 kHz (ADuC842/ADuC843), or 32kHz ± 10% (ADuC841)) |
| 4 | PRE0 | PRE3 PRE2 PRE1 PRE0 Timeout Period (ms) Action<br>0 0 0 0 15.6 Reset or Interrupt<br>0 0 0 1 31.2 Reset or Interrupt<br>0 0 1 0 62.5 Reset or Interrupt<br>0 0 1 1 125 Reset or Interrupt<br>0 1 0 0 250 Reset or Interrupt<br>0 1 0 1 500 Reset or Interrupt<br>0 1 1 0 1000 Reset or Interrupt<br>0 1 1 1 2000 Reset or Interrupt<br>1 0 0 0 0.0 Immediate Reset<br>PRE3–0 > 1000 Reserved |
| 3 | WDIR | Watchdog Interrupt Response Enable Bit.<br>If this bit is set by the user, the watchdog generates an interrupt response instead of a system reset when the watchdog timeout period has expired. This interrupt is not disabled by the CLR $\overline{EA}$ instruction, and it is also a fixed, high priority interrupt. If the watchdog is not being used to monitor the system, it can be used alternatively as a timer. The prescaler is used to set the timeout period in which an interrupt is generated. |
| 2 | WDS | Watchdog Status Bit.<br>Set by the watchdog controller to indicate that a watchdog timeout has occurred.<br>Cleared by writing a 0 or by an external hardware reset. It is not cleared by a watchdog reset. |
| 1 | WDE | Watchdog Enable Bit.<br>Set by the user to enable the watchdog and clear its counters. If this bit is not set by the user within the watchdog timeout period, the watchdog generates a reset or interrupt, depending on WDIR.<br>Cleared under the following conditions: user writes 0, watchdog reset (WDIR = 0); hardware reset; PSM interrupt. |
| 0 | WDWR | Watchdog Write Enable Bit.<br>To write data to the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and the very next instruction must be a write instruction to the WDCON SFR.<br>For example:<br>`CLR EA ;disable interrupts while writing`<br>`;to WDT`<br>`SETB WDWR ;allow write to WDCON`<br>`MOV WDCON,#72H ;enable WDT for 2.0s timeout`<br>`SETB EA ;enable interrupts again (if rqd)` |

## TIMER/COUNTER 0 AND 1 OPERATING MODES

The following sections describe the operating modes for Timer/Counters 0 and 1. Unless otherwise noted, assume that these modes of operation are the same for both Timer 0 and Timer 1.

### *Mode 0 (13-Bit Timer/Counter)*

Mode 0 configures an 8-bit timer/counter. Figure 66 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single-cycle core.

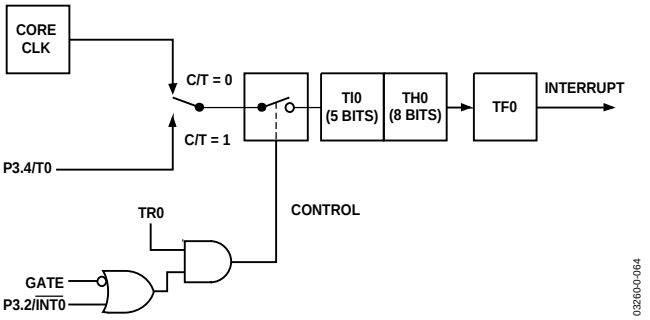


*Figure 66. Timer/Counter 0, Mode 0*

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulse-width measurements. TR0 is a control bit in the special function register TCON; Gate is in TMOD. The 13-bit register consists of all 8 bits of TH0 and the lower five bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

### *Mode 1 (16-Bit Timer/Counter)*

Mode 1 is the same as Mode 0, except that the Mode 1 timer register is running with all 16 bits. Mode 1 is shown in Figure 67.

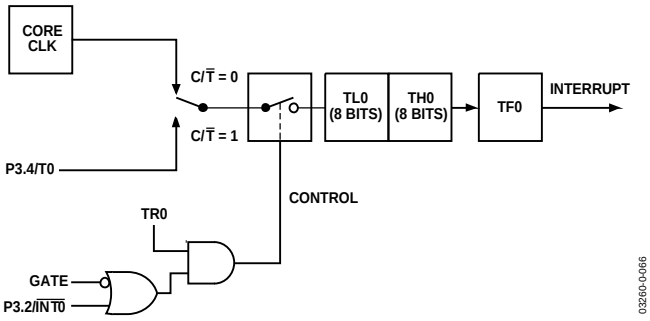


*Figure 67. Timer/Counter 0, Mode 1*

### *Mode 2 (8-Bit Timer/Counter with Autoreload)*

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload, as shown in Figure 68. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

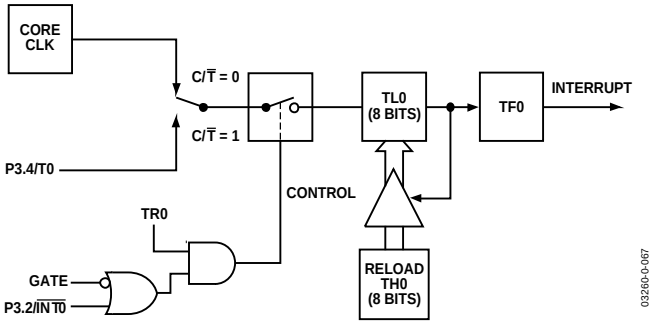


*Figure 68. Timer/Counter 0, Mode 2*

### *Mode 3 (Two 8-Bit Timer/Counters)*

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 69. TL0 uses the Timer 0 control bits: C/$\overline{T}$, Gate, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can still be used by the serial interface as a baud rate generator. In fact, it can be used in any application not requiring an interrupt from Timer 1 itself.

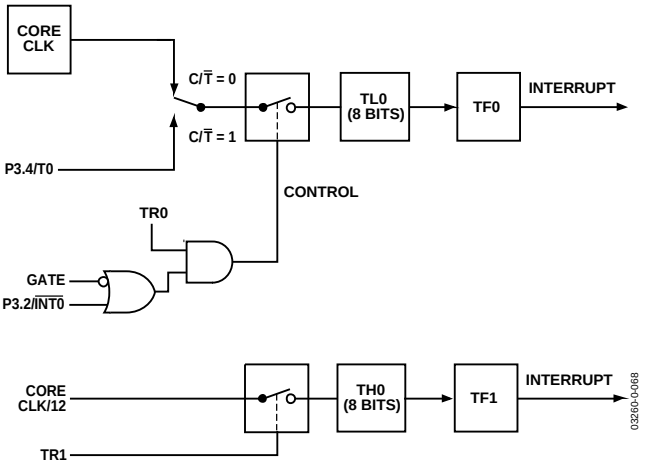


*Figure 69. Timer/Counter 0, Mode 3*

## INTERRUPT SYSTEM

The ADuC841/ADuC842/ADuC843 provide a total of nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

| | |
|---|---|
| **IE** | Interrupt Enable Register |
| **IP** | Interrupt Priority Register |
| **IEIP2** | Secondary Interrupt Enable Register |

| **IE** | **Interrupt Enable Register** |
|---|---|
| SFR Address | A8H |
| Power-On Default | 00H |
| Bit Addressable | Yes |

**Table 36. IE SFR Bit Designations**

| Bit No. | Name | Description |
|---|---|---|
| 7 | EA | Set by the user to enable, or cleared to disable all interrupt sources. |
| 6 | EADC | Set by the user to enable, or cleared to disable ADC interrupts. |
| 5 | ET2 | Set by the user to enable, or cleared to disable Timer 2 interrupts. |
| 4 | ES | Set by the user to enable, or cleared to disable UART serial port interrupts. |
| 3 | ET1 | Set by the user to enable, or cleared to disable 0 Timer 1 interrupts. |
| 2 | EX1 | Set by the user to enable, or cleared to disable External Interrupt 1. |
| 1 | ET0 | Set by the user to enable, or cleared to disable Timer 0 interrupts. |
| 0 | EX0 | Set by the user to enable, or cleared to disable External Interrupt 0 . |

| **IP** | **Interrupt Priority Register** |
|---|---|
| SFR Address | B8H |
| Power-On Default | 00H |
| Bit Addressable | Yes |

**Table 37. IP SFR Bit Designations**

| Bit No. | Name | Description |
|---|---|---|
| 7 | ---- | Reserved. |
| 6 | PADC | Written by the user to select the ADC interrupt priority (1 = High; 0 = Low). |
| 5 | PT2 | Written by the user to select the Timer 2 interrupt priority (1 = High; 0 = Low). |
| 4 | PS | Written by the user to select the UART serial port interrupt priority (1 = High; 0 = Low). |
| 3 | PT1 | Written by the user to select the Timer 1 interrupt priority (1 = High; 0 = Low). |
| 2 | PX1 | Written by the user to select External Interrupt 1 priority (1 = High; 0 = Low). |
| 1 | PT0 | Written by the user to select the Timer 0 interrupt priority (1 = High; 0 = Low). |
| 0 | PX0 | Written by the user to select External Interrupt 0 priority (1 = High; 0 = Low). |

If access to more than 64 kBytes of RAM is desired, a feature unique to the ADuC841/ADuC842/ADuC843 allows addressing up to 16 MBytes of external RAM simply by adding an additional latch as illustrated in Figure 79.

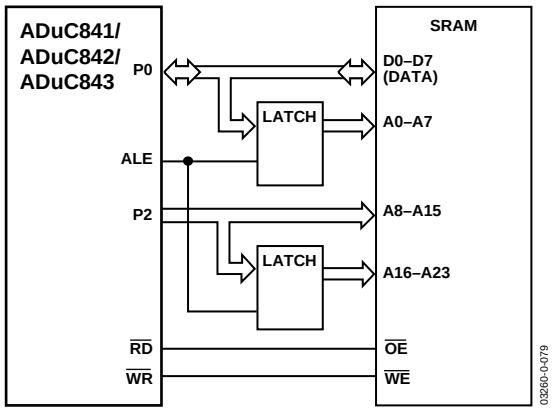


*Figure 79. External Data Memory Interface (16 MBytes Address Space)*

In either implementation, Port 0 (P0) serves as a multiplexed address/data bus. It emits the low byte of the data pointer (DPL) as an address, which is latched by a pulse of ALE prior to data being placed on the bus by the ADuC841/ADuC842/ADuC843 (write operation) or by the SRAM (read operation). Port 2 (P2) provides the data pointer page byte (DPP) to be latched by ALE, followed by the data pointer high byte (DPH). If no latch is connected to P2, DPP is ignored by the SRAM, and the 8051 standard of 64 kBytes external data memory access is maintained.

### *Power Supplies*

The operational power supply voltage of the parts depends on whether the part is the 3 V version or the 5 V version. The specifications are given for power supplies within 2.7 V to 3.6 V or ±5% of the nominal 5 V level.

Note that Figure 80 and Figure 81 refer to the PQFP package. For the CSP package, connect the extra $DV_{DD}$, DGND, $AV_{DD}$, and AGND in the same manner. Also, the paddle on the bottom of the package should be soldered to a metal plate to provide mechanical stability. This metal plate should not be connected to ground.

Separate analog and digital power supply pins ($AV_{DD}$ and $DV_{DD}$, respectively) allow $AV_{DD}$ to be kept relatively free of the noisy digital signals that are often present on the system $DV_{DD}$ line. However, though you can power $AV_{DD}$ and $DV_{DD}$ from two separate supplies if desired, you must ensure that they remain within ±0.3 V of one another at all times to avoid damaging the chip (as per the Absolute Maximum Ratings section). Therefore, it is recommended that unless $AV_{DD}$ and $DV_{DD}$ are connected directly together, back-to-back Schottky diodes should be connected between them, as shown in Figure 80.

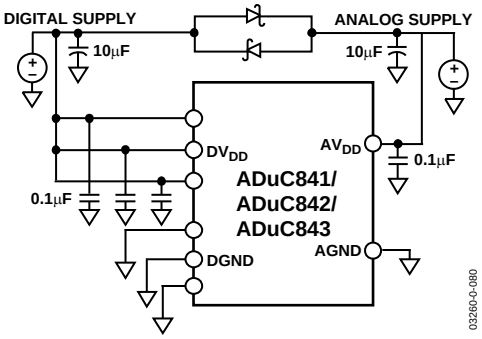


*Figure 80. External Dual-Supply Connections*

As an alternative to providing two separate power supplies, the user can help keep $AV_{DD}$ quiet by placing a small series resistor and/or ferrite bead between it and $DV_{DD}$, and then decoupling $AV_{DD}$ separately to ground. An example of this configuration is shown in Figure 81. With this configuration, other analog circuitry (such as op amps and voltage reference) can be powered from the $AV_{DD}$ supply line as well. The user still needs to include back-to-back Schottky diodes between $AV_{DD}$ and $DV_{DD}$ to protect them from power-up and power-down transient conditions that could momentarily separate the two supply voltages.

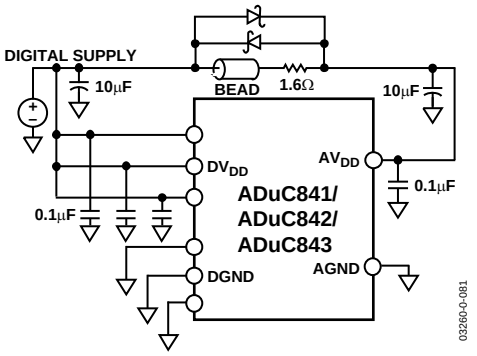


*Figure 81. External Single-Supply Connections*

Notice that in both Figure 80 and Figure 81, a large value (10 µF) reservoir capacitor sits on $DV_{DD}$ and a separate 10 µF capacitor sits on $AV_{DD}$. Also, local small-value (0.1 µF) capacitors are located at each $V_{DD}$ pin of the chip. As per standard design practice, be sure to include all of these capacitors, and ensure the smaller capacitors are close to each $AV_{DD}$ pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, note that at all times, the analog and digital ground pins on the part must be referenced to the same system ground reference point.

**5 V Part**

For $DV_{DD}$ below 4.5 V, the internal POR holds the part in reset. As $DV_{DD}$ rises above 4.5 V, an internal timer times out for approximately 128 ms before the part is released from reset. The user must ensure that the power supply has reached a stable 4.75 V minimum level by this time. Likewise on power-down, the internal POR holds the part in reset until the power supply has dropped below 1 V. Figure 83 illustrates the operation of the internal POR in detail.

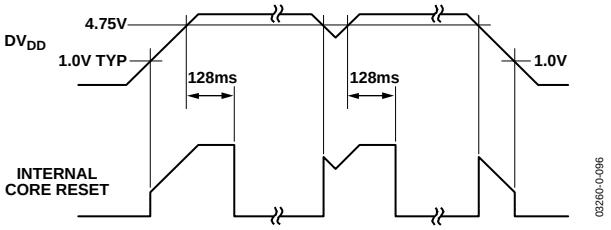


*Figure 83. Internal POR Operation*

### *Grounding and Board Layout Recommendations*

As with all high resolution data converters, special attention must be paid to grounding and PC board layout of ADuC841/ADuC842/ADuC843 based designs to achieve optimum performance from the ADC and the DACs. Although the parts have separate pins for analog and digital ground (AGND and DGND), the user must not tie these to two separate ground planes unless the two ground planes are connected together very close to the part, as illustrated in the simplified example of Figure 84a. In systems where digital and analog ground planes are connected together somewhere else (for example, at the system's power supply), they cannot be connected again near the part since a ground loop would result. In these cases, tie all the part's AGND and DGND pins to the analog ground plane, as illustrated in Figure 84b. In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board such that digital return currents do not flow near analog circuitry and vice versa. The part can then be placed between the digital and analog sections, as illustrated in Figure 84c.

In all of these scenarios, and in more complicated real-life applications, keep in mind the flow of current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths that the currents took to reach their destinations. For example, do not power components on the analog side of Figure 84b with $DV_{DD}$ since that would force return currents from $DV_{DD}$ to flow through AGND. Also, try to avoid digital currents flowing under analog circuitry, which could happen if the user places a noisy digital chip on the left half of the board in Figure 84c. Whenever possible, avoid large discontinuities in the ground plane(s) (like those formed by a long trace on the same layer), since they force return signals to travel a longer path. And of course, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the part's digital inputs, a series resistor should be added to each relevant line to keep rise and fall times longer than 5 ns at the part's input pins. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the part and from affecting the accuracy of ADC conversions.

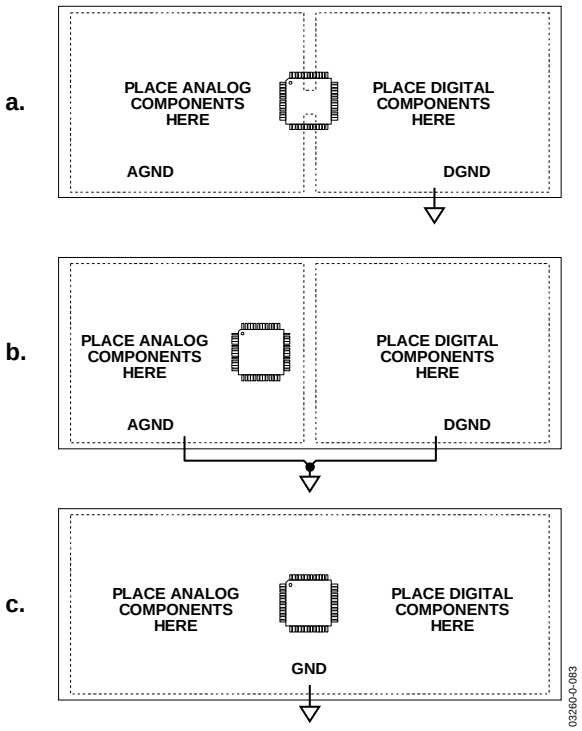


*Figure 84. System Grounding Schemes*

## ORDERING GUIDE

| Model[1] | Supply Voltage $V_{DD}$ | User Program Code Space | Temperature Range | Package Description | Package Option |
|---|---|---|---|---|---|
| ADuC841BSZ62-5 | 5 | 62 | –40°C to +85°C | 52-Lead Plastic Quad Flat Package [MQFP] | S-52-2 |
| ADuC841BSZ62-3 | 3 | 62 | –40°C to +85°C | 52-Lead Plastic Quad Flat Package [MQFP] | S-52-2 |
| ADuC841BCPZ62-5 | 5 | 62 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC841BCPZ62-3 | 3 | 62 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC841BCPZ8-5 | 5 | 8 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC841BCPZ8-3 | 3 | 8 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC842BSZ62-5 | 5 | 62 | –40°C to +85°C | 52-Lead Plastic Quad Flat Package [MQFP] | S-52-2 |
| ADuC842BSZ62-3 | 3 | 62 | –40°C to +85°C | 52-Lead Plastic Quad Flat Package [MQFP] | S-52-2 |
| ADuC842BCPZ62-5 | 5 | 62 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC842BCPZ62-3 | 3 | 62 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC842BCPZ32-5 | 5 | 32 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC842BCPZ32-3 | 3 | 32 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC842BCPZ8-5 | 5 | 8 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC842BCPZ8-3 | 3 | 8 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADUC843BSZ62-5 | 5 | 62 | –40°C to +85°C | 52-Lead Plastic Quad Flat Package [MQFP] | S-52-2 |
| ADuC843BSZ62-3 | 3 | 62 | –40°C to +85°C | 52-Lead Plastic Quad Flat Package [MQFP] | S-52-2 |
| ADuC843BCP62Z-5 | 5 | 62 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC843BCPZ62-3 | 3 | 62 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC843BCP32Z-5 | 5 | 32 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC843BCPZ32-3 | 3 | 32 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC843BCPZ8-5 | 5 | 8 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| ADuC843BCPZ8-3 | 3 | 8 | –40°C to +85°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| EVAL-ADuC841QSZ | 5 | | | QuickStart Development System for the ADuC841 | |
| EVAL-ADuC841QSPZ | 5 | | | QuickStart Plus Development System | |
| EVAL-ADuC842QSZ | 5 | | | QuickStart Development System for the ADuC842 and ADuC843 | |
| EVAL-ADuC842QSPZ | 5 | | | QuickStart Plus Development System | |
| USB-EA-CONVZ | | | | USB to EA Emulator | |

[1] The only difference between the ADuC842 and ADuC843devices is the voltage output DACs on the ADuC842; thus, the evaluation system for the ADuC842 is also suitable for the ADuC843.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).