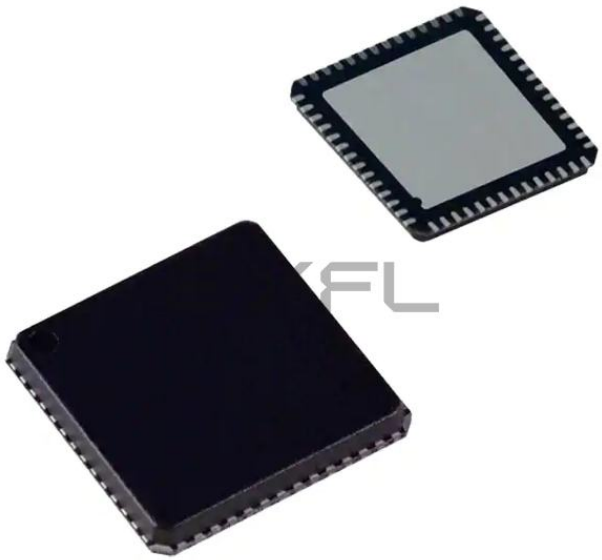

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	16.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, PSM, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc842bcpz8-5

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions/Comments
LOGIC INPUTS[4]				
INPUT VOLTAGES				
All Inputs Except SCLOCK, SDATA, RESET, and XTAL1				
VINL, Input Low Voltage	0.8	0.4	V max	
VINH, Input High Voltage	2.0	2.0	V min	
SDATA				
VINL, Input Low Voltage	0.8	0.8	V max	
VINH, Input High Voltage	2.0	2.0	V min	
SCLOCK and RESET ONLY[4]				
(Schmitt-Triggered Inputs)				
V_{T+}	1.3	0.95	V min	
	3.0	0.25	V max	
V_{T-}	0.8	0.4	V min	
	1.4	1.1	V max	
$V_{T+} - V_{T-}$	0.3	0.3	V min	
	0.85	0.85	V max	
CRYSTAL OSCILLATOR				
Logic Inputs, XTAL1 Only				
V_{INL}, Input Low Voltage	0.8	0.4	V typ	
V_{INH}, Input High Voltage	3.5	2.5	V typ	
XTAL1 Input Capacitance	18	18	pF typ	
XTAL2 Output Capacitance	18	18	pF typ	
MCU CLOCK RATE	16.78	8.38	MHz max	ADuC842/ADuC843 Only
	20	8.38	MHz max	ADuC841 Only
DIGITAL OUTPUTS				
Output High Voltage (V_{OH})	2.4		V min	V_{DD} = 4.5 V to 5.5 V
	4		V typ	I_{SOURCE} = 80 µA
		2.4	V min	V_{DD} = 2.7 V to 3.3 V
		2.6	V typ	I_{SOURCE} = 20 µA
Output Low Voltage (V_{OL})				
ALE, Ports 0 and 2	0.4	0.4	V max	I_{SINK} = 1.6 mA
	0.2	0.2	V typ	I_{SINK} = 1.6 mA
Port 3	0.4	0.4	V max	I_{SINK} = 4 mA
SCLOCK/SDATA	0.4	0.4	V max	I_{SINK} = 8 mA, I^2C Enabled
Floating State Leakage Current[4]	±10	±10	µA max	
	±1	±1	µA typ	
STARTUP TIME				At any core CLK
At Power-On	500	500	ms typ	
From Idle Mode	100	100	µs typ	
From Power-Down Mode				
Wake-up with $\overline{INT0}$ Interrupt	150	400	µs typ	
Wake-up with SPI/I^2C Interrupt	150	400	µs typ	
Wake-up with External RESET	150	400	µs typ	
After External RESET in Normal Mode	30	30	ms typ	
After WDT Reset in Normal Mode	3	3	ms typ	Controlled via WDCON SFR

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions/Comments
POWER REQUIREMENTS[19, 20]				
Power Supply Voltages				
AV_{DD}/DV_{DD} – AGND		2.7	V min	AV_{DD}/DV_{DD} = 3 V nom
		3.6	V max	
	4.75		V min	AV_{DD}/DV_{DD} = 5 V nom
	5.25		V max	
Power Supply Currents **Normal** Mode[21]				
DV_{DD} Current[4]	10	4.5	mA typ	Core CLK = 2.097 MHz
AV_{DD} Current	1.7	1.7	mA max	Core CLK = 2.097 MHz
DV_{DD} Current	38	12	mA max	Core CLK = 16.78MHz/8.38 MHz 5 V/3 V
	33	10	mA typ	Core CLK = 16.78MHz/8.38 MHz 5 V/3 V
AV_{DD} Current	1.7	1.7	mA max	Core CLK = 16.78MHz/8.38 MHz 5 V/3 V
DV_{DD} Current[4]	45	N/A	mA max	Core CLK = 20MHz **ADuC841 Only**
Power Supply Currents **Idle** Mode[21]				
DV_{DD} Current	4.5	2.2	mA typ	Core CLK = 2.097 MHz
AV_{DD} Current	3	2	µA typ	Core CLK = 2.097 MHz
DV_{DD} Current[4]	12	5	mA max	Core CLK = 16.78 MHz/8.38 MHz 5 V/3 V
	10	3.5	mA typ	Core CLK = 16.78 MHz/8.38 MHz 5 V/3 V
AV_{DD} Current	3	2	µA typ	Core CLK = 16.78 MHz/8.38 MHz 5 V/3 V
Power Supply Currents **Power-Down** Mode[21]				Core CLK = any frequency
DV_{DD} Current	28	18	µA max	Oscillator Off / TIMECON.1 = 0
	20	10	µA typ	
AV_{DD} Current	2	1	µA typ	Core CLK = any frequency, **ADuC841 Only**
DV_{DD} Current[4]	3	1	mA max	TIMECON.1 = 1
DV_{DD} Current[4]	50	22	µA max	Core CLK = any frequency
	40	15	µA typ	**ADuC842/ADuC843 Only,** oscillator on
Typical Additional Power Supply Currents				
PSM Peripheral	15	10	µA typ	AV_{DD} = DV_{DD}
ADC[4]	1.0	1.0	mA min	MCLK Divider = 32
	2.8	1.8	mA max	MCLK Divider = 2
DAC	150	130	µA typ	

See footnotes on the next page.

[1] Temperature Range –40°C to +85°C.
[2] ADC linearity is guaranteed during normal MicroConverter core operation.
[3] ADC LSB size = $V_{REF}/2^{12}$, that is, for internal V_{REF} = 2.5 V, 1 LSB = 610 µV, and for external V_{REF} = 1 V, 1 LSB = 244 µV.
[4] These numbers are not production tested but are supported by design and/or characterization data on production release.
[5] Offset and gain error and offset and gain error match are measured after factory calibration.
[6] Based on external ADC system components, the user may need to execute a system calibration to remove additional external channel errors to achieve these specifications.
[7] SNR calculation includes distortion and noise components.
[8] Channel-to-channel crosstalk is measured on adjacent channels.
[9] The temperature monitor gives a measure of the die temperature directly; air temperature can be inferred from this result.
[10] DAC linearity is calculated using:
Reduced code range of 100 to 4095, 0 V to V_{REF} range.
Reduced code range of 100 to 3945, 0 V to V_{DD} range.
DAC output load = 10 kΩ and 100 pF.
[11] DAC differential nonlinearity specified on 0 V to V_{REF} and 0 V to V_{DD} ranges.
[12] DAC specification for output impedance in the unbuffered case depends on DAC code.
[13] DAC specifications for I_{SINK}, voltage output settling time, and digital-to-analog glitch energy depend on external buffer implementation in unbuffered mode. DAC in unbuffered mode tested with OP270 external buffer, which has a low input leakage current.
[14] Measured with C_{REF} pin decoupled with 0.47 µF capacitor to ground. Power-up time for the internal reference is determined by the value of the decoupling capacitor chosen for the C_{REF} pin.
[15] When using an external reference device, the internal band gap reference input can be bypassed by setting the ADCCON1.6 bit.
[16] Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and the Flash/EE data memory.
[17] Endurance is qualified to 100,000 cycles as per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, and +85°C. Typical endurance at 25°C is 700,000 cycles.
[18] Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22 method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature as shown in Figure 38 in the Flash/EE Memory Reliability section.
[19] Power supply current consumption is measured in normal, idle, and power-down modes under the following conditions:

Normal Mode:	Reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON (ADuC842/ADuC843), core executing internal software loop.
Idle Mode:	Reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON (ADuC842/ADuC843), PCON.0 = 1, core execution suspended in idle mode.
Power-Down Mode:	Reset = 0.4 V, all Port 0 pins = 0.4 V, All other digital I/O and Port 1 pins are open circuit, Core Clk changed via CD bits in PLLCON (ADuC842/ADuC843), PCON.0 = 1, core execution suspended in power-down mode, OSC turned on or off via OSC_PD bit (PLLCON.7) in PLLCON SFR (ADuC842/ADuC843).

[20] DV_{DD} power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.
[21] Power supply currents are production tested at 5.25 V and 3.3 V for a 5 V and 3 V part, respectively.

Pin No.	Mnemonic	Type[1]	Description
31	P2.3/A11/A19	I/O	Input/Output Port 2 (P2.3). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A11). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A19). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
32	XTAL1	I	Input to the Inverting Oscillator Amplifier.
33	XTAL2	O	Output of the Inverting Oscillator Amplifier.
36	P2.4/A12/A20	I/O	Input/Output Port 2 (P2.4). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A12). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A20). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
37	P2.5/A13/A21	I/O	Input/Output Port 2 (P2.5). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A13). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A21). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
38	P2.6/PWM0/A14/A22	I/O	Input/Output Port 2 (P2.6). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. PWM 0 Voltage Output (PWM0). PWM outputs can be configured to use Port 2.6 and Port 2.7 or Port 3.4 and Port 3.3. External Memory Addresses (A14). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A22). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
39	P2.7/PWM1/A15/A23	I/O	Input/Output Port 2 (P2.7). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. PWM 1 Voltage Output (PWM1). See the CFG841/CFG842 register for further information. External Memory Addresses (A15). Port 2 emits the middle-order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A23). Port 2 emits the high-order address bytes during accesses to the external 24-bit external data memory space.
40	$\overline{EA}$	I	External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations. The devices do not support external code memory. Do not leave this pin floating.
41	$\overline{PSEN}$	O	Program Store Enable, Logic Output. This pin remains low during internal program execution. $\overline{PSEN}$ enables serial download mode when pulled low through a resistor on power-up or reset. On reset, this pin momentarily becomes an input and the status of the pin is sampled. If there is no pull-down resistor in place, the pin goes momentarily high and then user code executes. If a pull-down resistor is in place, the embedded serial download/debug kernel executes.
42	ALE	O	Address Latch Enable, Logic Output. This output latches the low byte and page byte for 24-bit address space accesses of the address into external data memory.

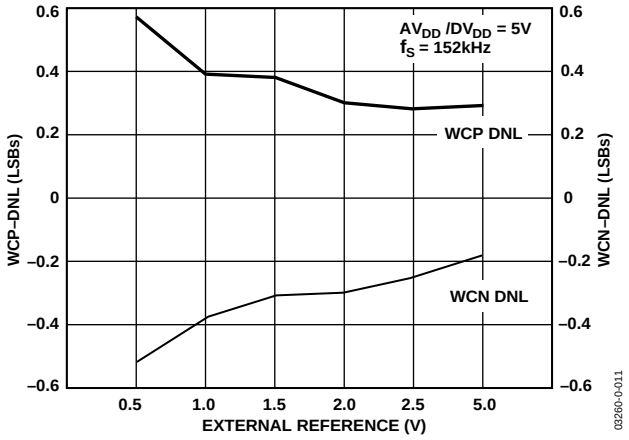

Figure 13. Typical Worst-Case DNL Error vs. V_{REF}, V_{DD} = 5 V

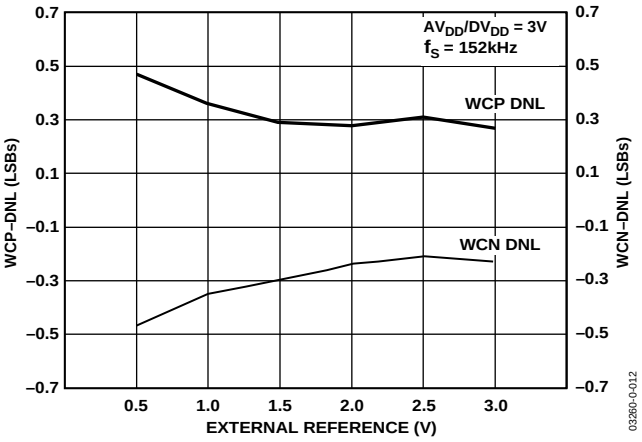

Figure 14. Typical Worst-Case DNL Error vs. V_{REF}, V_{DD} = 3 V

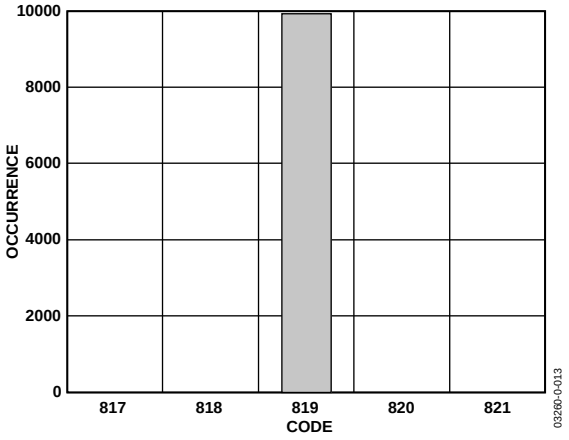

Figure 15. Code Histogram Plot, V_{DD} = 5 V

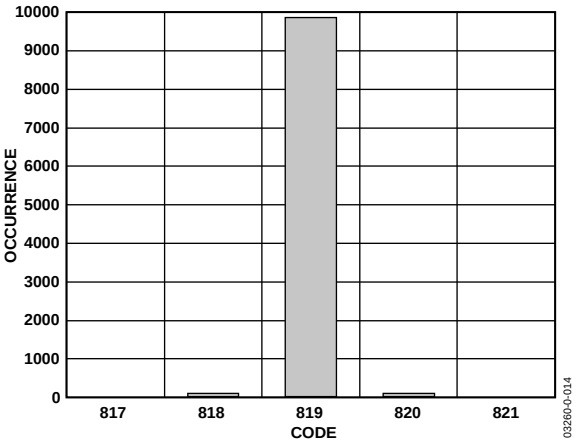

Figure 16. Code Histogram Plot, V_{DD} = 3 V

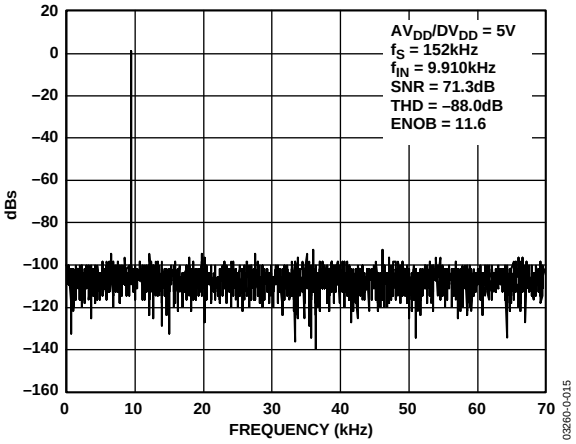

Figure 17. Dynamic Performance at V_{DD} = 5 V

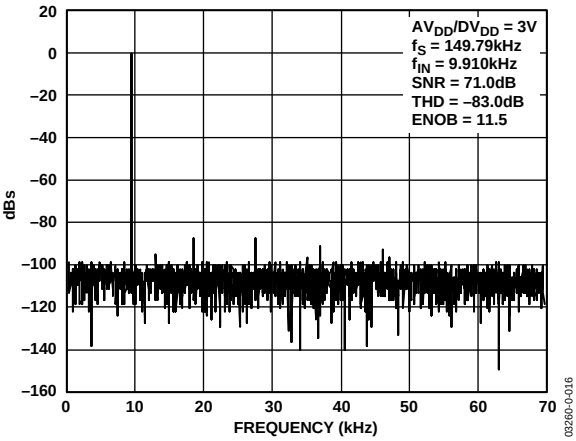

Figure 18. Dynamic Performance at V_{DD} = 3 V

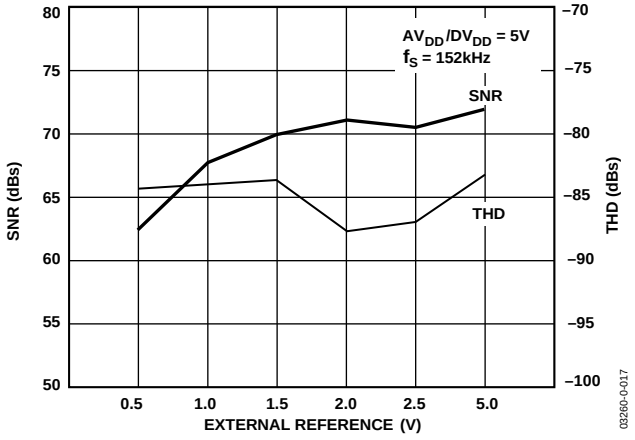

Figure 19. Typical Dynamic Performance vs. V_{REF}, V_{DD} = 5 V

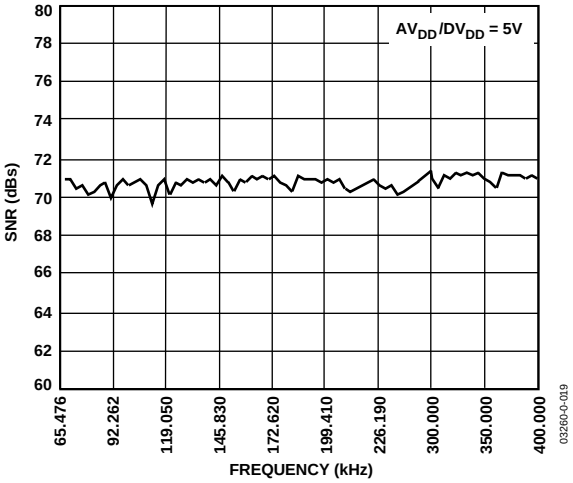

Figure 21. Typical Dynamic Performance vs. Sampling Frequency

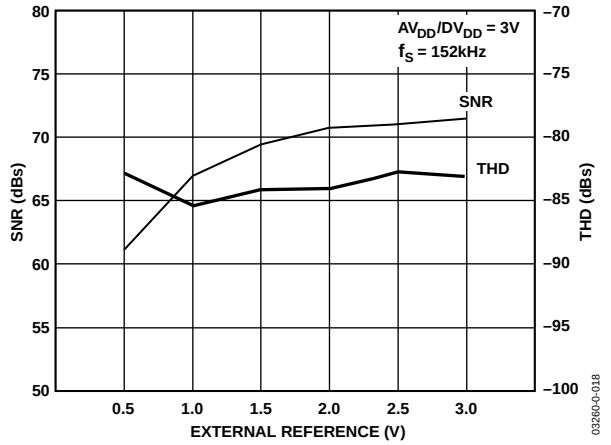

Figure 20. Typical Dynamic Performance vs. V_{REF}, V_{DD} = 3 V

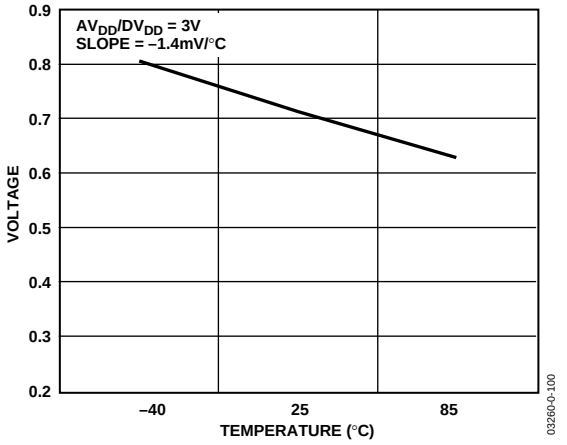

Figure 22. Typical Temperature Sensor Output vs. Temperature

GENERAL DESCRIPTION (*continued*)

The parts also incorporate additional analog functionality with two 12-bit DACs, power supply monitor, and a band gap reference. On-chip digital peripherals include two 16-bit Σ-Δ. DACs, a dual output 16-bit PWM, a watchdog timer, a time interval counter, three timers/counters, and three serial I/O ports (SPI, I²C, and UART).

On the ADuC812 and the ADuC832, the I²C and SPI interfaces share some of the same pins. For backwards compatibility, this is also the case for the ADuC841/ADuC842/ADuC843.

However, there is also the option to allow SPI operate separately on P3.3, P3.4, and P3.5, while I²C uses the standard pins. The I²C interface has also been enhanced to offer repeated start, general call, and quad addressing.

On-chip factory firmware supports in-circuit serial download and debug modes (via UART) as well as single-pin emulation mode via the $\overline{EA}$ pin. A functional block diagram of the parts is shown on the first page.

ADCCON3—(ADC Control SFR 3)

The ADCCON3 register controls the operation of various calibration modes and also indicates the ADC busy status.

SFR Address	F5H
SFR Power-On Default	00H
Bit Addressable	No

Table 10. ADCCON3 SFR Bit Designations

Bit No.	Name	Description
7	BUSY	ADC Busy Status Bit. A read-only status bit that is set during a valid ADC conversion or during a calibration cycle. Busy is automatically cleared by the core at the end of conversion or calibration.
6	RSVD	Reserved. This bit should always be written as 0.
5	AVGS1	Number of Average Selection Bits.
4	AVGS0	This bit selects the number of ADC readings that are averaged during a calibration cycle. AVGS1 AVGS0 Number of Averages 0 0 15 0 1 1 1 0 31 1 1 63
3	RSVD	Reserved. This bit should always be written as 0.
2	RSVD	This bit should always be written as 1 by the user when performing calibration.
1	TYPICAL	Calibration Type Select Bit. This bit selects between offset (zero-scale) and gain (full-scale) calibration. Set to 0 for offset calibration. Set to 1 for gain calibration.
0	SCAL	Start Calibration Cycle Bit. When set, this bit starts the selected calibration cycle. It is automatically cleared when the calibration cycle is completed.

If using the temperature sensor as the ADC input, the ADC should be configured to use an ADCCLK of MCLK/32 and four acquisition clocks.

Increasing the conversion time on the temperature monitor channel improves the accuracy of the reading. To further improve the accuracy, an external reference with low temperature drift should also be used.

ADC DMA Mode

The on-chip ADC has been designed to run at a maximum conversion speed of 2.38 µs (420 kHz sampling rate). When converting at this rate, the ADuC841/ADuC842/ADuC843 MicroConverter® has 2 µs to read the ADC result and to store the result in memory for further postprocessing; otherwise the next ADC sample could be lost. In an interrupt driven routine, the MicroConverter would also have to jump to the ADC interrupt service routine, which also increases the time required to store the ADC results. In applications where the parts cannot sustain the interrupt rate, an ADC DMA mode is provided.

To enable DMA mode, Bit 6 in ADCCON2 (DMA) must be set, which allows the ADC results to be written directly to a 16 MByte external static memory SRAM (mapped into data memory space) without any interaction from the core of the part. This mode allows the part to capture a contiguous sample stream at full ADC update rates (420 kHz).

Typical DMA Mode Configuration Example

Setting the parts to DMA mode consists of the following steps:

1. The ADC must be powered down. This is done by ensuring that MD1 and MD0 are both set to 0 in ADCCON1.
2. The DMA address pointer must be set to the start address of where the ADC results are to be written. This is done by writing to the DMA mode address pointers DMAL, DMAH, and DMAP. DMAL must be written to first, followed by DMAH, and then by DMAP.
3. The external memory must be preconfigured. This consists of writing the required ADC channel IDs into the top four bits of every second memory location in the external SRAM, starting at the first address specified by the DMA address pointer. Because the ADC DMA mode operates independently from the ADuC841/ADuC842/ADuC843 core, it is necessary to provide it with a stop command. This is done by duplicating the last channel ID to be converted followed by 1111 into the next channel selection field. A typical preconfiguration of external memory is shown in Figure 34.

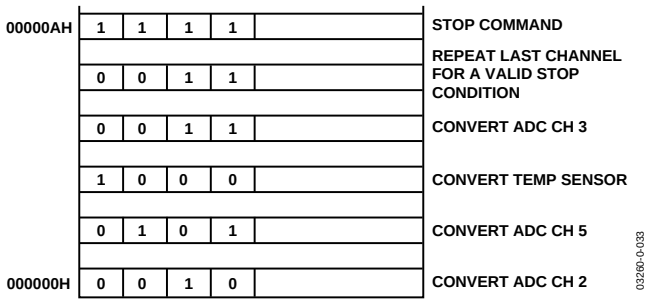

Figure 34. Typical DMA External Memory Preconfiguration

4. The DMA is initiated by writing to the ADC SFRs in the following sequence:
   a. ADCCON2 is written to enable the DMA mode, that is, MOV ADCCON2, #40H; DMA mode enabled.
   b. ADCCON1 is written to configure the conversion time and power-up of the ADC. It can also enable Timer 2 driven conversions or external triggered conversions if required.
   c. ADC conversions are initiated. This is done by starting single conversions, starting Timer 2, running for Timer 2 conversions, or receiving an external trigger.

When the DMA conversions are complete, the ADC interrupt bit, ADCI, is set by hardware, and the external SRAM contains the new ADC conversion results as shown in Figure 35. Note that no result is written to the last two memory locations.

When the DMA mode logic is active, it takes the responsibility of storing the ADC results away from both the user and the core logic of the part. As the DMA interface writes the results of the ADC conversions to external memory, it takes over the external memory interface from the core. Thus, any core instructions that access the external memory while DMA mode is enabled does not get access to the external memory. The core executes the instructions, and they take the same time to execute, but they cannot access the external memory.

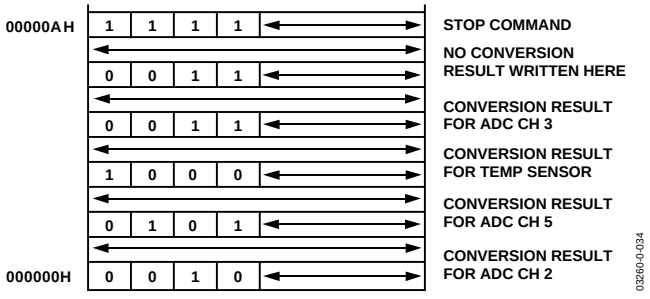

Figure 35. Typical External Memory Configuration Post ADC DMA Operation

The DMA logic operates from the ADC clock and uses pipelining to perform the ADC conversions and to access the external memory at the same time. The time it takes to perform one ADC conversion is called a DMA cycle. The actions performed by the logic during a typical DMA cycle are shown in Figure 36.

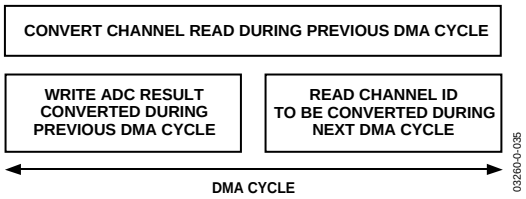

Figure 36. DMA Cycle

Figure 36 shows that during one DMA cycle, the following actions are performed by the DMA logic:

1. An ADC conversion is performed on the channel whose ID was read during the previous cycle.
2. The 12-bit result and the channel ID of the conversion performed in the previous cycle is written to the external memory.
3. The ID of the next channel to be converted is read from external memory.

For the previous example, the complete flow of events is shown in Figure 36. Because the DMA logic uses pipelining, it takes three cycles before the first correct result is written out.

Micro Operation during ADC DMA Mode

During ADC DMA mode, the MicroConverter core is free to continue code execution, including general housekeeping and communication tasks. However, note that MCU core accesses to Ports 0 and 2 (which of course are being used by the DMA controller) are gated off during the ADC DMA mode of operation. This means that even though the instruction that accesses the external Ports 0 or 2 appears to execute, no data is seen at these external ports as a result. Note that during DMA to the internally contained XRAM, Ports 0 and 2 are available for use.

The only case in which the MCU can access XRAM during DMA is when the internal XRAM is enabled and the section of RAM to which the DMA ADC results are being written to lies in an external XRAM. Then the MCU can access the internal XRAM only. This is also the case for use of the extended stack pointer.

The MicroConverter core can be configured with an interrupt to be triggered by the DMA controller when it has finished filling the requested block of RAM with ADC results, allowing the service routine for this interrupt to postprocess data without any real-time timing constraints.

ADC Offset and Gain Calibration Coefficients

The ADuC841/ADuC842/ADuC843 have two ADC calibration coefficients, one for offset calibration and one for gain calibration. Both the offset and gain calibration coefficients are 14-bit words, and are each stored in two registers located in the special function register (SFR) area. The offset calibration coefficient is divided into ADCOFSH (six bits) and ADCOFSL (8 bits), and the gain calibration coefficient is divided into ADCGAINH (6 bits) and ADCGAINL (8 bits).

The offset calibration coefficient compensates for dc offset errors in both the ADC and the input signal. Increasing the offset coefficient compensates for positive offset, and effectively pushes the ADC transfer function down. Decreasing the offset coefficient compensates for negative offset, and effectively pushes the ADC transfer function up. The maximum offset that can be compensated is typically ±5% of V_{REF}, which equates to typically ±125 mV with a 2.5 V reference.

Similarly, the gain calibration coefficient compensates for dc gain errors in both the ADC and the input signal. Increasing the gain coefficient compensates for a smaller analog input signal range and scales the ADC transfer function up, effectively increasing the slope of the transfer function. Decreasing the gain coefficient compensates for a larger analog input signal range and scales the ADC transfer function down, effectively decreasing the slope of the transfer function. The maximum analog input signal range for which the gain coefficient can compensate is $1.025 \times V_{REF}$, and the minimum input range is $0.975 \times V_{REF}$, which equates to typically ±2.5% of the reference voltage.

CALIBRATING THE ADC

Two hardware calibration modes are provided, which can be easily initiated by user software. The ADCCON3 SFR is used to calibrate the ADC. Bit 1 (typical) and CS3 to CS0 (ADCCON2) set up the calibration modes.

Device calibration can be initiated to compensate for significant changes in operating condition frequency, analog input range, reference voltage, and supply voltages. In this calibration mode, offset calibration uses internal AGND selected via ADCCON2 register Bits CS3 to CS0 (1011), and gain calibration uses internal V_{REF} selected by Bits CS3 to CS0 (1100). Offset calibration should be executed first, followed by gain calibration. System calibration can be initiated to compensate for both internal and external system errors. To perform system calibration by using an external reference, tie the system ground and reference to any two of the six selectable inputs. Enable external reference mode (ADCCON1.6). Select the channel connected to AGND via Bits CS3 to CS0 and perform system offset calibration. Select the channel connected to V_{REF} via Bits CS3 to CS0 and perform system gain calibration.

A 4 kByte Flash/EE data memory space is also provided on-chip. This may be used as a general-purpose nonvolatile scratchpad area. User access to this area is via a group of six SFRs. This space can be programmed at a byte level, although it must first be erased in 4-byte pages.

Flash/EE Memory Reliability

The Flash/EE program and data memory arrays on the parts are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events, defined as

1. Initial page erase sequence.
2. Read/verify sequence a single Flash/EE.
3. Byte program sequence memory.
4. Second read/verify sequence endurance cycle.

In reliability qualification, every byte in both the program and data Flash/EE memory is cycled from 00H to FFH until a first fail is recorded, signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specifications table, the parts' Flash/EE memory endurance qualification has been carried out in accordance with JEDEC Retention Lifetime Specification A117 over the industrial temperature range of –40°C to +25°C and +25°C to +85°C. The results allow the specification of a minimum endurance figure over supply and over temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the parts have been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit, described previously, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time the Flash/EE memory is reprogrammed. Also note that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J as shown in Figure 38.

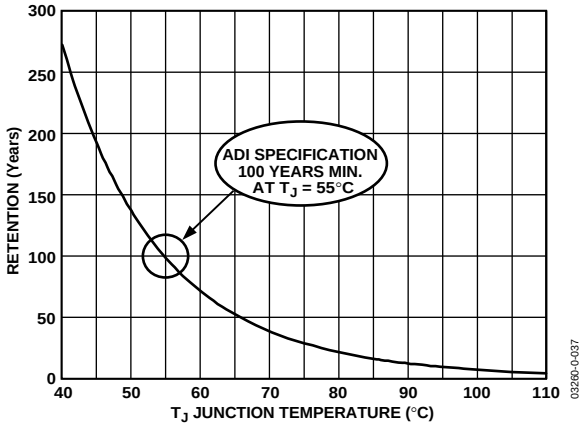

Figure 38. Flash/EE Memory Data Retention

Using the Flash/EE Program Memory

The 62 kByte Flash/EE program memory array is mapped into the lower 62 kBytes of the 64 kByte program space addressable by the parts, and is used to hold user code in typical applications. The program Flash/EE memory array can be programmed in three ways:

Serial Downloading (In-Circuit Programming)

The parts facilitate code download via the standard UART serial port. The parts enter serial download mode after a reset or power cycle if the $\overline{\text{PSEN}}$ pin is pulled low through an external 1 kΩ resistor. Once in serial download mode, the user can download code to the full 62 kBytes of Flash/EE program memory while the device is in-circuit in its target application hardware.

A PC serial download executable is provided as part of the ADuC841/ADuC842 QuickStart development system. The serial download protocol is detailed in MicroConverter Application Note uC004.

Parallel Programming

Parallel programming mode is fully compatible with conventional third party flash or EEPROM device programmers. In this mode, Ports P0, P1, and P2 operate as the external data and address bus interface, ALE operates as the write enable strobe, and Port P3 is used as a general configuration port, which configures the device for various program and erase operations during parallel programming. The high voltage (12 V) supply required for flash programming is generated using on-chip charge pumps to supply the high voltage program lines. The complete parallel programming specification is available on the MicroConverter home page at www.analog.com/microconverter.

USING FLASH/EE DATA MEMORY

The 4 kBytes of Flash/EE data memory are configured as 1024 pages, each of 4 bytes. As with the other ADuC841/ADuC842/ADuC843 peripherals, the interface to this memory space is via a group of registers mapped in the SFR space. A group of four data registers (EDATA1–4) is used to hold the four bytes of data at each page. The page is addressed via the two registers, EADRH and EADRL. Finally, ECON is an 8-bit control register that may be written with one of nine Flash/EE memory access commands to trigger various read, write, erase, and verify functions. A block diagram of the SFR interface to the Flash/EE data memory array is shown in Figure 41.

ECON—Flash/EE Memory Control SFR

Programming of either Flash/EE data memory or Flash/ EE program memory is done through the Flash/EE memory control SFR (ECON). This SFR allows the user to read, write, erase, or verify the 4 kBytes of Flash/EE data memory or the 56 kBytes of Flash/EE program memory.

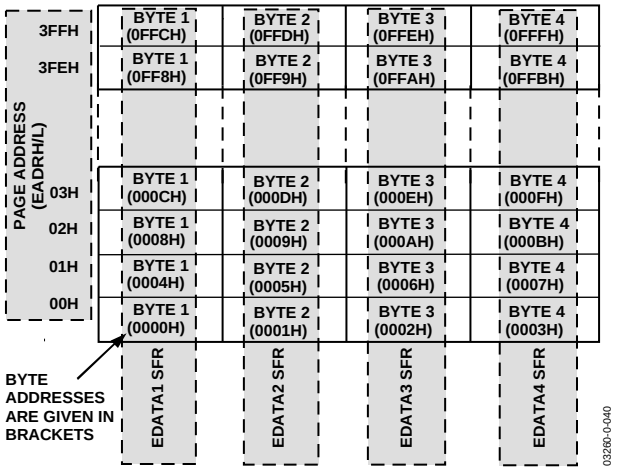

Figure 41. Flash/EE Data Memory Control and Configuration

Table 13. ECON—Flash/EE Memory Commands

ECON VALUE	Command Description (Normal Mode) (Power-On Default)	Command Description (ULOAD Mode)
01H READ	Results in 4 bytes in the Flash/EE data memory, addressed by the page address EADRH/L, being read into EDATA1–4.	Not implemented. Use the MOVC instruction.
02H WRITE	Results in 4 bytes in EDATA1–4 being written to the Flash/EE data memory at the page address given by EADRH/L (0 – EADRH/L < 0400H). Note that the 4 bytes in the page being addressed must be pre-erased.	Results in bytes 0–255 of internal XRAM being written to the 256 bytes of Flash/EE program memory at the page address given by EADRH (0 – EADRH < E0H). Note that the 256 bytes in the page being addressed must be pre-erased.
03H	Reserved.	Reserved.
04H VERIFY	Verifies that the data in EDATA1–4 is contained in the page address given by EADRH/L. A subsequent read of the ECON SFR results in 0 being read if the verification is valid, or a nonzero value being read to indicate an invalid verification.	Not implemented. Use the MOVC and MOVX instructions to verify the write in software.
05H ERASE PAGE	Results in erasing the 4-byte page of Flash/EE data memory addressed by the page address EADRH/L.	Results in the 64 byte page of Flash/EE program memory, addressed by the byte address EADRH/L, being erased. EADRL can equal any of 64 locations within the page. A new page starts whenever EADRL is equal to 00H, 40H, 80H, or C0H.
06H ERASE ALL	Results in erasing the entire 4 kBytes of Flash/EE data memory.	Results in erasing the entire 56 kBytes of ULOAD Flash/EE program memory.
81H READBYTE	Results in the byte in the Flash/EE data memory, addressed by the byte address EADRH/L, being read into EDATA1 (0 – EADRH / L – 0FFFH).	Not implemented. Use the MOVC command.
82H WRITEBYTE	Results in the byte in EDATA1 being written into Flash/EE data memory at the byte address EADRH/L	Results in the byte in EDATA1 being written into Flash/EE program memory at the byte address EADRH/L (0 – EADRH/L – DFFFH).
0FH EXULOAD	Leaves the ECON instructions to operate on the Flash/EE data memory.	Enters normal mode directing subsequent ECON instructions to operate on the Flash/EE data memory.
F0H ULOAD	Enters ULOAD mode, directing subsequent ECON instructions to operate on the Flash/EE program memory.	Leaves the ECON instructions to operate on the Flash/EE program memory.

Example: Programming the Flash/EE Data Memory

A user wants to program F3H into the second byte on Page 03H of the Flash/EE data memory space while preserving the other 3 bytes already in this page. A typical program of the Flash/EE data array involves

1. Setting EADRH/L with the page address.
2. Writing the data to be programmed to the EDATA1–4.
3. Writing the ECON SFR with the appropriate command.

Step 1: Set Up the Page Address

Address registers EADRH and EADRL hold the high byte address and the low byte address of the page to be addressed. The assembly language to set up the address may appear as

```
MOV EADRH,#0            ; Set Page Address Pointer
MOV EADRL,#03H
```

Step 2: Set Up the EDATA Registers

Write the four values to be written into the page into the four SFRs, EDATA1–4. Unfortunately, the user does not know three of them. Thus, the user must read the current page and overwrite the second byte.

```
MOV ECON,#1             ; Read Page into EDATA1-4
MOV EDATA2,#0F3H        ; Overwrite byte 2
```

Step 3: Program Page

A byte in the Flash/EE array can be programmed only if it has previously been erased. To be more specific, a byte can be programmed only if it already holds the value FFH. Because of the Flash/EE architecture, this erase must happen at a page level; therefore, a minimum of 4 bytes (1 page) are erased when an erase command is initiated. Once the page is erase, the user can program the 4 bytes in-page and then perform a verification of the data.

```
MOV ECON,#5             ; ERASE Page
MOV ECON,#2             ; WRITE Page
MOV ECON,#4             ; VERIFY Page
MOV A,ECON              ; Check if ECON=0 (OK!)
JNZ ERROR
```

Although the 4 kBytes of Flash/EE data memory are shipped from the factory pre-erased, that is, byte locations set to FFH, it is nonetheless good programming practice to include an ERASEALL routine as part of any configuration/setup code running on the parts. An ERASEALL command consists of writing 06H to the ECON SFR, which initiates an erase of the 4-kByte Flash/EE array. This command coded in 8051 assembly would appear as

```
MOV ECON,#06H           ; Erase all Command
                        ; 2 ms Duration
```

Flash/EE Memory Timing

Typical program and erase times for the parts are as follows:

Normal Mode (operating on Flash/EE data memory)

READPAGE (4 bytes)	22 machine cycles
WRITEPAGE (4 bytes)	380 µs
VERIFYPAGE (4 bytes)	22 machine cycles
ERASEPAGE (4 bytes)	2 ms
ERASEALL (4 kBytes)	2 ms
READBYTE (1 byte)	9 machine cycles
WRITEBYTE (1 byte)	200 µs

ULOAD Mode (operating on Flash/EE program memory)

WRITEPAGE (256 bytes)	16.5 ms
ERASEPAGE (64 bytes)	2 ms
ERASEALL (56 kBytes)	2 ms
WRITEBYTE (1 byte)	200 µs

Note that a given mode of operation is initiated as soon as the command word is written to the ECON SFR. The core microcontroller operation on the parts is idled until the requested program/read or erase mode is completed. In practice, this means that even though the Flash/EE memory mode of operation is typically initiated with a two machine cycle MOV instruction (to write to the ECON SFR), the next instruction is not executed until the Flash/EE operation is complete. This means that the core cannot respond to interrupt requests until the Flash/EE operation is complete, although the core peripheral functions like counter/timers continue to count and time as configured throughout this period.

Mode 4: Dual NRZ 16-Bit Σ-Δ DAC

Mode 4 provides a high speed PWM output similar to that of a Σ-Δ DAC. Typically, this mode is used with the PWM clock equal to 16.777216 MHz. In this mode, P2.6 and P2.7 are updated every PWM clock (60 ns in the case of 16 MHz). Over any 65536 cycles (16-bit PWM) PWM0 (P2.6) is high for PWM0H/L cycles and low for (65536 – PWM0H/L) cycles. Similarly, PWM1 (P2.7) is high for PWM1H/L cycles and low for (65536 – PWM1H/L) cycles.

For example, if PWM1H is set to 4010H (slightly above one quarter of FS), then P2.7 is typically low for three clocks and high for one clock (each clock is approximately 60 ns). Over every 65536 clocks, the PWM compensates for the fact that the output should be slightly above one quarter of full scale by having a high cycle followed by only two low cycles.

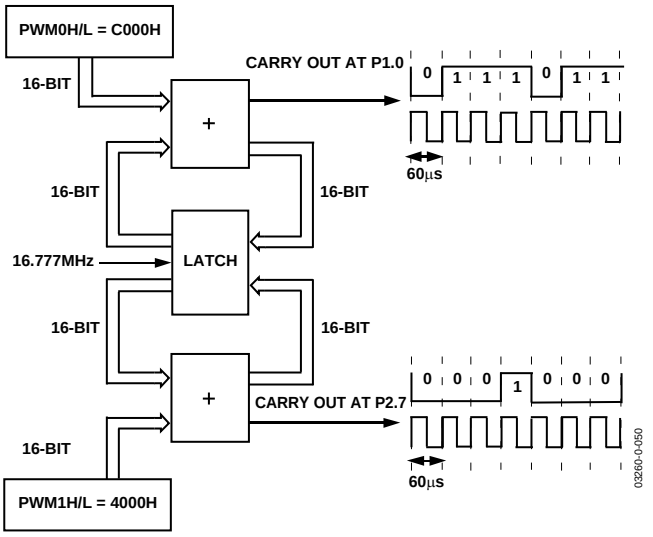

Figure 51. PWM Mode 4

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required. If, for example, only 12-bit performance is required, write 0s to the four LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 4.096 kHz. Similarly writing 0s to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 65 kHz.

Mode 5: Dual 8-Bit PWM

In Mode 5, the duty cycle of the PWM outputs and the resolution of the PWM outputs are individually programmable. The maximum resolution of the PWM output is 8 bits. The output resolution is set by the PWM1L and PWM1H SFRs for the P2.6 and P2.7 outputs, respectively. PWM0L and PWM0H sets the duty cycles of the PWM outputs at P2.6 and P2.7, respectively. Both PWMs have the same clock source and clock divider.

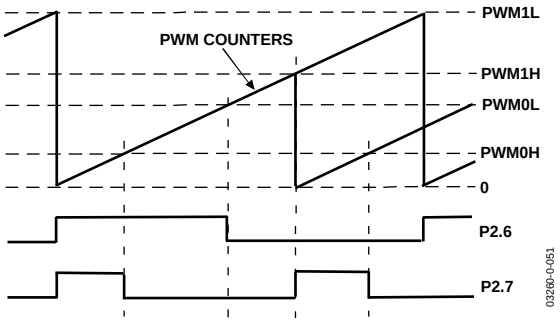

Figure 52. PWM Mode 5

Mode 6: Dual RZ 16-Bit Σ-Δ DAC

Mode 6 provides a high speed PWM output similar to that of a Σ-Δ DAC. Mode 6 operates very similarly to Mode 4. However, the key difference is that Mode 6 provides return-to-zero (RZ) Σ-Δ DAC output. Mode 4 provides non-return-to-zero Σ-Δ DAC outputs. The RZ mode ensures that any difference in the rise and fall times do not affect the Σ-Δ DAC INL. However, the RZ mode halves the dynamic range of the Σ-Δ DAC outputs from 0 V–AV_{DD} down to 0 V–AV_{DD}/2. For best results, this mode should be used with a PWM clock divider of 4.

If PWM1H is set to 4010H (slightly above one quarter of FS), P2.7 is typically low for three full clocks (3 × 60 ns), high for half a clock (30 ns), and then low again for half a clock (30 ns) before repeating itself. Over every 65536 clocks, the PWM compensates for the fact that the output should be slightly above one quarter of full scale by leaving the output high for two half clocks in four. The rate at which this happens depends on the value and degree of compensation required.

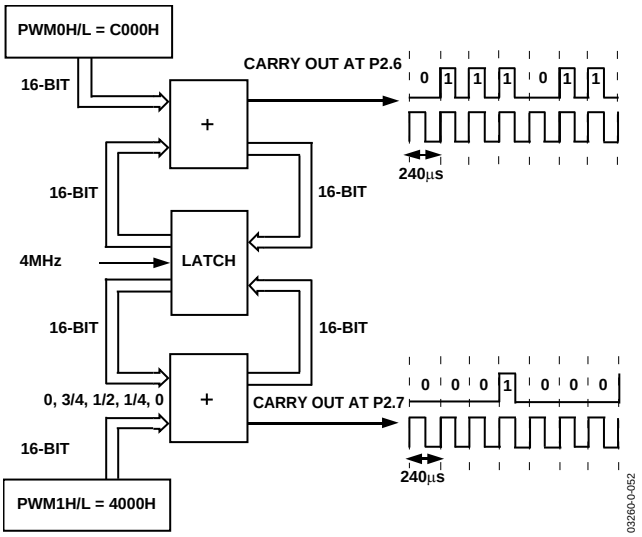

Figure 53. PWM Mode 6

WATCHDOG TIMER

The purpose of the watchdog timer is to generate a device reset or interrupt within a reasonable amount of time if the ADuC841/ADuC842/ADuC843 enter an erroneous state, possibly due to a programming error or electrical noise. The watchdog function can be disabled by clearing the WDE (watchdog enable) bit in the watchdog control (WDCON) SFR. When enabled, the watchdog circuit generates a system reset or interrupt (WDS) if the user program fails to set the watchdog (WDE) bit within a predetermined amount of time (see PRE3-0 bits in Table 24. The watchdog timer is clocked directly from the 32 kHz external crystal on the ADuC842/ADuC843. On the ADuC841, the watchdog timer is clocked by an internal R/C oscillator at 32 kHz ±10%. The WDCON SFR can be written only by user software if the double write sequence described in WDWR below is initiated on every write access to the WDCON SFR.

WDCON Watchdog Timer	Control Register
SFR Address	C0H
Power-On Default	10H
Bit Addressable	Yes

Table 24. WDCON SFR Bit Designations

Bit No.	Name	Description
7	PRE3	Watchdog Timer Prescale Bits.
6	PRE2	The watchdog timeout period is given by the equation $t_{WD} = (2^{PRE} \times (2^9/f_{XTAL}))$
5	PRE1	(0 – PRE – 7; f_{XTAL} = 32.768 kHz (ADuC842/ADuC843), or 32kHz ± 10% (ADuC841))
4	PRE0	PRE3 PRE2 PRE1 PRE0 Timeout Period (ms) Action 0 0 0 0 15.6 Reset or Interrupt 0 0 0 1 31.2 Reset or Interrupt 0 0 1 0 62.5 Reset or Interrupt 0 0 1 1 125 Reset or Interrupt 0 1 0 0 250 Reset or Interrupt 0 1 0 1 500 Reset or Interrupt 0 1 1 0 1000 Reset or Interrupt 0 1 1 1 2000 Reset or Interrupt 1 0 0 0 0.0 Immediate Reset PRE3–0 > 1000 Reserved
3	WDIR	Watchdog Interrupt Response Enable Bit. If this bit is set by the user, the watchdog generates an interrupt response instead of a system reset when the watchdog timeout period has expired. This interrupt is not disabled by the CLR $\overline{EA}$ instruction, and it is also a fixed, high priority interrupt. If the watchdog is not being used to monitor the system, it can be used alternatively as a timer. The prescaler is used to set the timeout period in which an interrupt is generated.
2	WDS	Watchdog Status Bit. Set by the watchdog controller to indicate that a watchdog timeout has occurred. Cleared by writing a 0 or by an external hardware reset. It is not cleared by a watchdog reset.
1	WDE	Watchdog Enable Bit. Set by the user to enable the watchdog and clear its counters. If this bit is not set by the user within the watchdog timeout period, the watchdog generates a reset or interrupt, depending on WDIR. Cleared under the following conditions: user writes 0, watchdog reset (WDIR = 0); hardware reset; PSM interrupt.

0	WDWR	Watchdog Write Enable Bit.
		To write data to the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and the very next instruction must be a write instruction to the WDCON SFR.
		For example:
		`CLR EA ;disable interrupts while writing`
		`;to WDT`
		`SETB WDWR ;allow write to WDCON`
		`MOV WDCON,#72H ;enable WDT for 2.0s timeout`
		`SETB EA ;enable interrupts again (if rqd)`

TIME INTERVAL COUNTER (TIC)

A TIC is provided on-chip for counting longer intervals than the standard 8051 compatible timers are capable of. The TIC is capable of timeout intervals ranging from 1/128 second to 255 hours. Furthermore, this counter is clocked by the external 32.768 kHz crystal rather than by the core clock, and it has the ability to remain active in power-down mode and time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular widely spaced readings are required.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow clocks the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled. If the part is in power-down mode, again with TIC interrupt enabled, the TII bit wakes up the device and resumes code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described in Table 25. Note also that the time based SFRs can be written initially with the current time; the TIC can then be controlled and accessed by user software. In effect, this facilitates the implementation of a real-time clock. A block diagram of the TIC is shown in Figure 56.

The TIC is clocked directly from a 32 kHz external crystal on the ADuC842/ADuC843 and by the internal 32 kHz ±10% R/C oscillator on the ADuC841. Due to this, instructions that access the TIC registers are also clocked at this speed. The user should ensure that there is sufficient time between instructions to these registers to allow them to execute correctly.

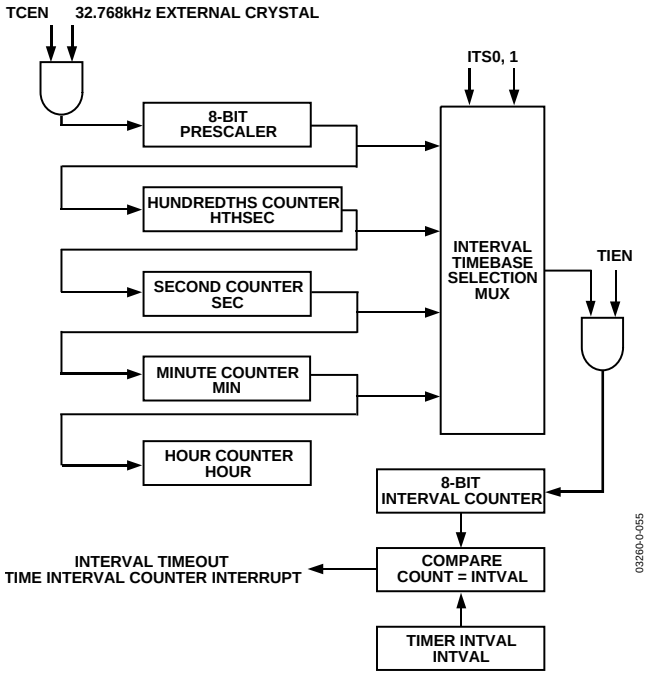

Figure 56. TIC, Simplified Block Diagram

HARDWARE DESIGN CONSIDERATIONS

This section outlines some of the key hardware design considerations that must be addressed when integrating the ADuC841/ADuC842/ADuC843 into any hardware system.

Clock Oscillator

The clock source for the parts can be generated by the internal PLL or by an external clock input. To use the internal PLL, connect a 32.768 kHz parallel resonant crystal between XTAL1 and XTAL2, and connect a capacitor from each pin to ground as shown in Figure 75. The parts contain an internal capacitance of 18 pF on the XTAL1 and XTAL2 pins, which is sufficient for most watch crystals. This crystal allows the PLL to lock correctly to give an f_{VCO} of 16.777216 MHz. If no crystal is present, the PLL free runs, giving an fVCO of 16.7 MHz ±20%. In this mode, the CD bits are limited to CD = 1, giving a max core clock of 8.38 MHz. This is useful if an external clock input is required. The part powers up and the PLL free runs; the user then writes to the CFG842 SFR in software to enable the external clock input on P3.4. Note that double the required clock must be provided externally since the part runs at CD = 1. A better solution is to use the ADuC841 with the external clock.

For the ADuC841, connect the crystal in the same manner; external capacitors should be connected as per the crystal manufacturer's recommendations. A minimum capacitance of 20 pF is recommended on XTAL1 and XTAL2. The ADuC841 does not operate if no crystal is present.

An external clock may be connected as shown in Figure 76 and Figure 77.

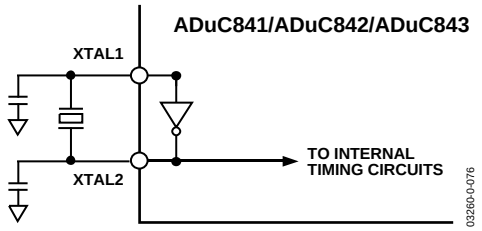

Figure 75. External Parallel Resonant Crystal Connections

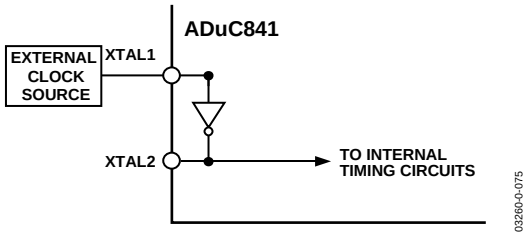

Figure 76. Connecting an External Clock Source (ADuC841)

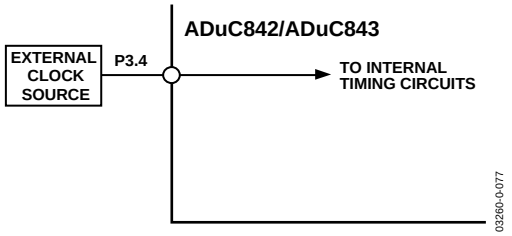

Figure 77. Connecting an External Clock Source (ADuC842/ADuC843)

Whether using the internal PLL or an external clock source, the specified operational clock speed range of the devices is 400 kHz to 16.777216 MHz, (20 MHz, ADuC841). The core itself is static, and functions all the way down to dc. But at clock speeds slower that 400 kHz, the ADC can no longer function correctly. Therefore, to ensure specified operation, use a clock frequency of at least 400 kHz and no more than 20 MHz.

External Memory Interface

In addition to its internal program and data memories, the parts can access up to 16 MBytes of external data memory (SRAM). Note that the parts cannot access external program memory.

Figure 78 shows a hardware configuration for accessing up to 64 kBytes of external RAM. This interface is standard to any 8051 compatible MCU.

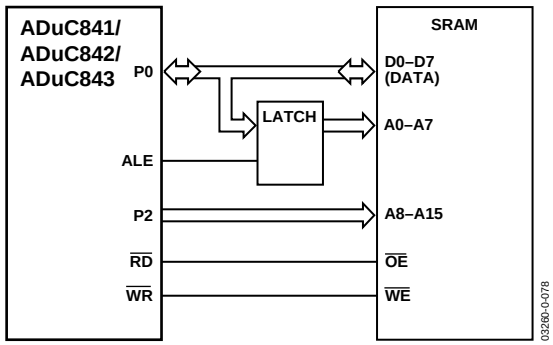

Figure 78. External Data Memory Interface (64 kBytes Address Space)

If access to more than 64 kBytes of RAM is desired, a feature unique to the ADuC841/ADuC842/ADuC843 allows addressing up to 16 MBytes of external RAM simply by adding an additional latch as illustrated in Figure 79.

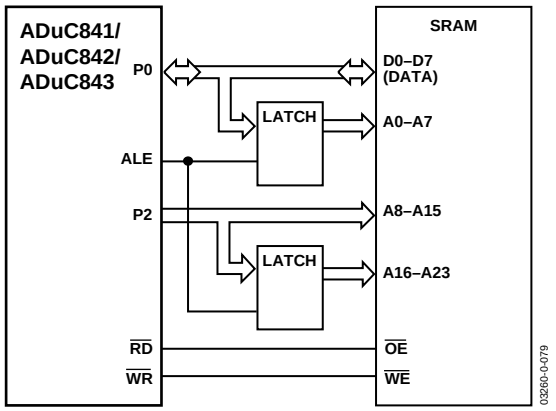

Figure 79. External Data Memory Interface (16 MBytes Address Space)

In either implementation, Port 0 (P0) serves as a multiplexed address/data bus. It emits the low byte of the data pointer (DPL) as an address, which is latched by a pulse of ALE prior to data being placed on the bus by the ADuC841/ADuC842/ADuC843 (write operation) or by the SRAM (read operation). Port 2 (P2) provides the data pointer page byte (DPP) to be latched by ALE, followed by the data pointer high byte (DPH). If no latch is connected to P2, DPP is ignored by the SRAM, and the 8051 standard of 64 kBytes external data memory access is maintained.

Power Supplies

The operational power supply voltage of the parts depends on whether the part is the 3 V version or the 5 V version. The specifications are given for power supplies within 2.7 V to 3.6 V or ±5% of the nominal 5 V level.

Note that Figure 80 and Figure 81 refer to the PQFP package. For the CSP package, connect the extra DV_{DD}, DGND, AV_{DD}, and AGND in the same manner. Also, the paddle on the bottom of the package should be soldered to a metal plate to provide mechanical stability. This metal plate should not be connected to ground.

Separate analog and digital power supply pins (AV_{DD} and DV_{DD}, respectively) allow AV_{DD} to be kept relatively free of the noisy digital signals that are often present on the system DV_{DD} line. However, though you can power AV_{DD} and DV_{DD} from two separate supplies if desired, you must ensure that they remain within ±0.3 V of one another at all times to avoid damaging the chip (as per the Absolute Maximum Ratings section). Therefore, it is recommended that unless AV_{DD} and DV_{DD} are connected directly together, back-to-back Schottky diodes should be connected between them, as shown in Figure 80.

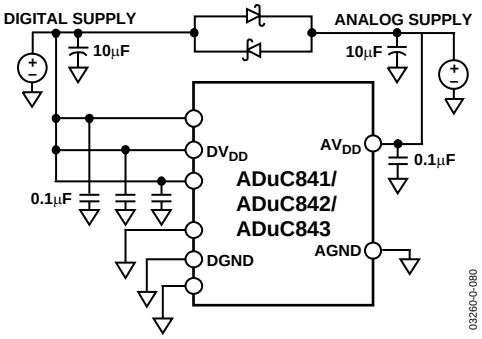

Figure 80. External Dual-Supply Connections

As an alternative to providing two separate power supplies, the user can help keep AV_{DD} quiet by placing a small series resistor and/or ferrite bead between it and DV_{DD}, and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 81. With this configuration, other analog circuitry (such as op amps and voltage reference) can be powered from the AV_{DD} supply line as well. The user still needs to include back-to-back Schottky diodes between AV_{DD} and DV_{DD} to protect them from power-up and power-down transient conditions that could momentarily separate the two supply voltages.

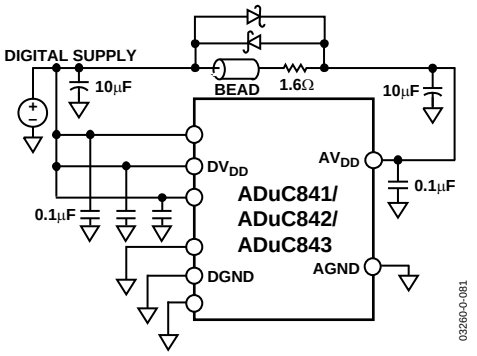

Figure 81. External Single-Supply Connections

Notice that in both Figure 80 and Figure 81, a large value (10 µF) reservoir capacitor sits on DV_{DD} and a separate 10 µF capacitor sits on AV_{DD}. Also, local small-value (0.1 µF) capacitors are located at each V_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors, and ensure the smaller capacitors are close to each AV_{DD} pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, note that at all times, the analog and digital ground pins on the part must be referenced to the same system ground reference point.

Parameter		16 MHz Core Clk		8 MHz Core Clock		
EXTERNAL DATA MEMORY READ CYCLE		**Min**	**Max**	**Min**	**Max**	**Unit**
t_{RLRH}	$\overline{RD}$ Pulse Width	60		125		ns
t_{AVLL}	Address Valid after ALE Low	60		120		ns
t_{LLAX}	Address Hold after ALE Low	145		290		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		48		100	Ns
t_{RHDX}	Data and Address Hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		150		625	ns
t_{LLDV}	ALE Low to Valid Data In		170		350	ns
t_{AVDV}	Address to Valid Data In		230		470	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	130		255		ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	190		375		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		15		35	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	60		120		ns

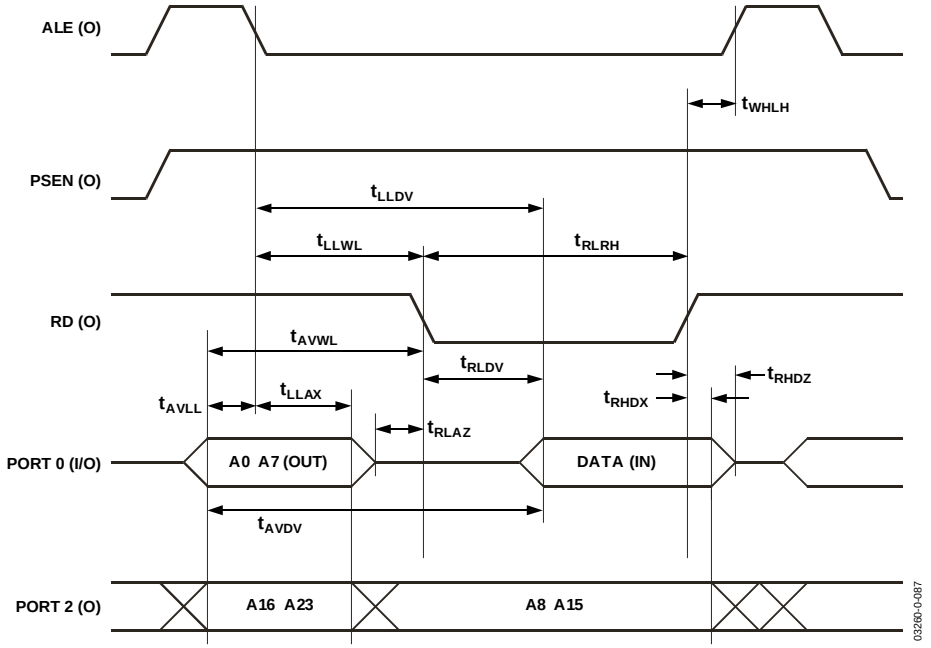

Figure 88. External Data Memory Read Cycle

Parameter					
SPI SLAVE MODE TIMING (CPHA = 0)		**Min**	**Typ**	**Max**	**Unit**
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{DOSS}	Data Output Valid after $\overline{SS}$ Edge			20	ns
t_{SFS}	$\overline{SS}$ High after SCLOCK Edge				ns

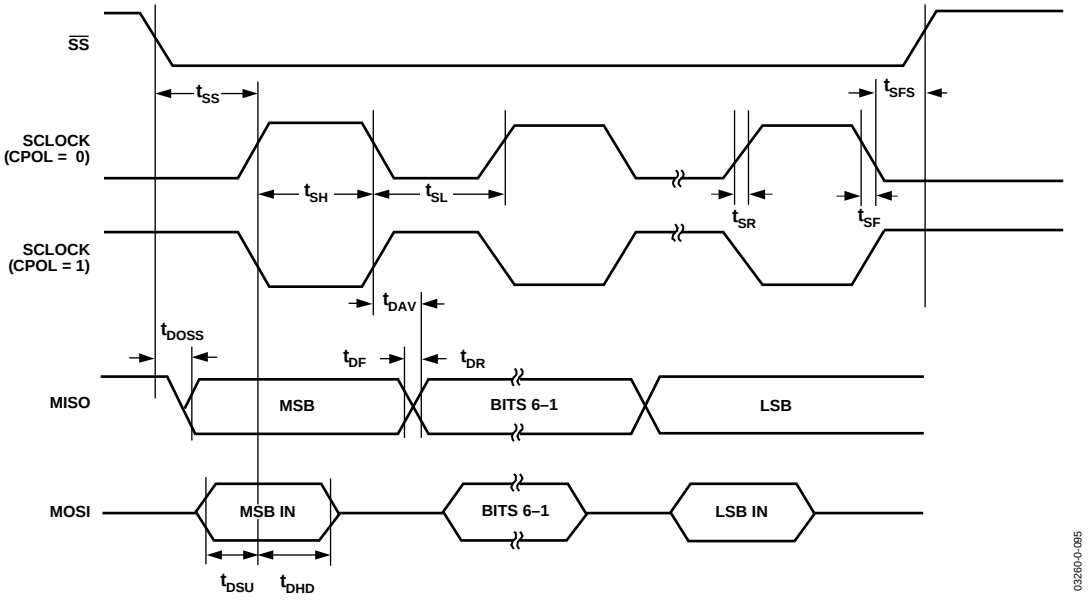

Figure 94. SPI Slave Mode Timing (CPHA = 0)

ORDERING GUIDE

Model[1]	Supply Voltage V_{DD}	User Program Code Space	Temperature Range	Package Description	Package Option
ADuC841BSZ62-5	5	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC841BSZ62-3	3	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC841BCPZ62-5	5	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC841BCPZ62-3	3	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC841BCPZ8-5	5	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC841BCPZ8-3	3	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BSZ62-5	5	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC842BSZ62-3	3	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC842BCPZ62-5	5	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BCPZ62-3	3	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BCPZ32-5	5	32	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BCPZ32-3	3	32	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BCPZ8-5	5	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BCPZ8-3	3	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADUC843BSZ62-5	5	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC843BSZ62-3	3	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC843BCP62Z-5	5	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC843BCPZ62-3	3	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC843BCP32Z-5	5	32	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC843BCPZ32-3	3	32	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC843BCPZ8-5	5	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC843BCPZ8-3	3	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
EVAL-ADuC841QSZ	5			QuickStart Development System for the ADuC841	
EVAL-ADuC841QSPZ	5			QuickStart Plus Development System	
EVAL-ADuC842QSZ	5			QuickStart Development System for the ADuC842 and ADuC843	
EVAL-ADuC842QSPZ	5			QuickStart Plus Development System	
USB-EA-CONVZ				USB to EA Emulator	

[1] The only difference between the ADuC842 and ADuC843devices is the voltage output DACs on the ADuC842; thus, the evaluation system for the ADuC842 is also suitable for the ADuC843.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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