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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	16.78MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	DMA, PSM, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	80-PQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc842bsz62-5

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REVISION HISTORY

4/16—Rev. 0 to Rev. A

Added Patent Note, Note 1	1
Changes to Figure 3 and Table 3	9
Changes to Figure 4.....	14
Added Table 4; Renumbered Sequentially	14

Changes to Using the DAC Section	47
Updated Outline Dimensions.....	94
Changes to Ordering Guide	95

11/03—Revision 0: Initial Version

ABSOLUTE MAXIMUM RATINGS

Table 2. $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Rating
AV_{DD} to DV_{DD}	$-0.3\text{ V to }+0.3\text{ V}$
AGND to DGND	$-0.3\text{ V to }+0.3\text{ V}$
DV_{DD} to DGND, AV_{DD} to AGND	$-0.3\text{ V to }+7\text{ V}$
Digital Input Voltage to DGND	$-0.3\text{ V to }DV_{DD} + 0.3\text{ V}$
Digital Output Voltage to DGND	$-0.3\text{ V to }DV_{DD} + 0.3\text{ V}$
V_{REF} to AGND	$-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$
Analog Inputs to AGND	$-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$
Operating Temperature Range, Industrial	$-40^\circ\text{C to }+85^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature	150°C
θ_{JA} Thermal Impedance (ADuC84xBS)	90°C/W
θ_{JA} Thermal Impedance (ADuC84xBCP)	52°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

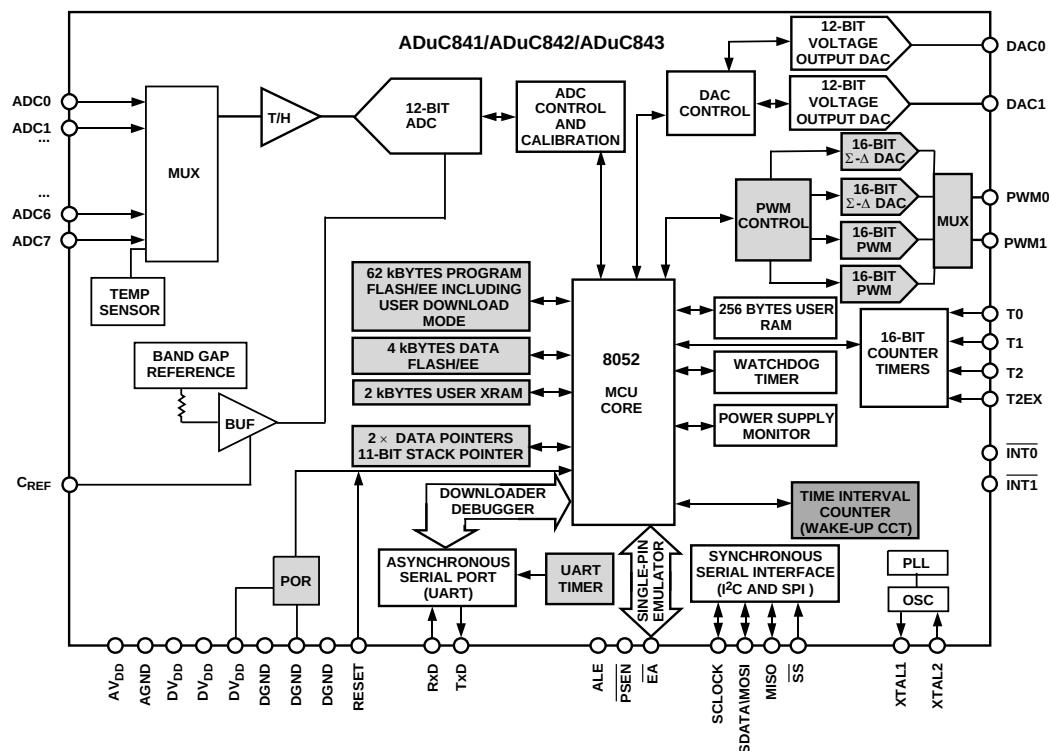


Figure 2. ADuC841/ADuC842/ADuC843 Block Diagram (Shaded Areas are Features Not Present on the ADuC812), No DACs on ADuC843, PLL on ADuC842/ADuC843 Only.

Pin No.	Mnemonic	Type ¹	Description
43	P0.0/A0	I/O	Input/Output Port 0 (P0.0). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A0). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
44	P0.1/A1	I/O	Input/Output Port 0 (P0.1). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A1). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
45	P0.2/A2	I/O	Input/Output Port 0 (P0.2). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A2). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
46	P0.3/A3	I/O	Input/Output Port 0 (P0.3). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A3). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
49	P0.4/A4	I/O	Input/Output Port 0 (P0.4). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A4). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
50	P0.5/A5	I/O	Input/Output Port 0 (P0.5). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A5). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
51	P0.6/A6	I/O	Input/Output Port 0 (P0.6). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A6). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
52	P0.7/A7	I/O	Input/Output Port 0 (P0.7). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A7). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.

¹ P = power, G = ground, I = input, O = output, NC = no connect.

Pin No.	Mnemonic	Type ¹	Description
46	P0.0/A0	I/O	Input/Output Port 0 (P0.0). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A0). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-ups when emitting 1s.
47	P0.1/A1	I/O	Input/Output Port 0 (P0.1). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A1). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
48	P0.2/A2	I/O	Input/Output Port 0 (P0.2). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A2). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
49	P0.3/A3	I/O	Input/Output Port 0 (P0.3). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A3). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
52	P0.4/A4	I/O	Input/Output Port 0 (P0.4). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A4). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
53	P0.5/A5	I/O	Input/Output Port 0 (P0.5). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A5). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
54	P0.6/A6	I/O	Input/Output Port 0 (P0.6). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A6). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
55	P0.7/A7	I/O	Input/Output Port 0 (P0.7). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A7). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
56	P1.0/ADC0/T2 EPAD	I	Input Port 1 (P1.0). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit. Single-Ended Analog Input (ADC0). Channel selection is via ADCCON2 SFR. Timer 2 Digital Input (T2). Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1-to-0 transition of the T2 input. Exposed Pad. The LFCSP has an exposed pad that must be soldered to the metal plate on the printed circuit board (PCB) for mechanical reasons and to DGND.

¹ P = power, G = ground, I = input, O = output, and NC = no connect.

Mnemonic	Description	Bytes	Cycles
Branching			
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
ACALL addr11	Absolute jump to subroutine	2	3
AJMP addr11	Absolute jump unconditional	2	3
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry equal to 1	2	3
JNC rel	Jump on carry equal to 0	2	3
JZ rel	Jump on accumulator = 0	2	3
JNZ rel	Jump on accumulator not equal to 0	2	3
DJNZ Rn,rel	Decrement register, JNZ relative	2	3
LJMP	Long jump unconditional	3	4
LCALL addr16	Long jump to subroutine	3	4
JB bit,rel	Jump on direct bit = 1	3	4
JNB bit,rel	Jump on direct bit = 0	3	4
JBC bit,rel	Jump on direct bit = 1 and clear	3	4
CJNE A,dir,rel	Compare A, direct JNE relative	3	4
CJNE A,#data,rel	Compare A, immediate JNE relative	3	4
CJNE Rn,#data,rel	Compare register, immediate JNE relative	3	4
CJNE @Ri,#data,rel	Compare indirect, immediate JNE relative	3	4
DJNZ dir,rel	Decrement direct byte, JNZ relative	3	4
Miscellaneous			
NOP	No operation	1	1

1. One cycle is one clock.

2. Cycles of MOVX instructions are four cycles when they have 0 wait state. Cycles of MOVX instructions are 4 + n cycles when they have n wait states.

3. Cycles of LCALL instruction are three cycles when the LCALL instruction comes from interrupt.

OTHER SINGLE-CYCLE CORE FEATURES

Timer Operation

Timers on a standard 8052 increment by 1 with each machine cycle. On the [ADuC841/ADuC842/ADuC843](#), one machine cycle is equal to one clock cycle; therefore the timers increment at the same rate as the core clock.

ALE

The output on the ALE pin on a standard 8052 part is a clock at 1/6th of the core operating frequency. On the [ADuC841/ADuC842/ADuC843](#) the ALE pin operates as follows. For a single machine cycle instruction, ALE is high for the first half of the machine cycle and low for the second half. The ALE output is at the core operating frequency. For a two or more machine cycle instruction, ALE is high for the first half of the first machine cycle and low for the rest of the machine cycles.

External Memory Access

There is no support for external program memory access on the parts. When accessing external RAM, the EWAIT register may need to be programmed to give extra machine cycles to MOVX commands. This is to account for differing external RAM access speeds.

EWAIT SFR

SFR Address	9FH
Power-On Default	00H
Bit Addressable	No

This special function register (SFR) is programmed with the number of wait states for a MOVX instruction. This value can range from 0H to 7H.

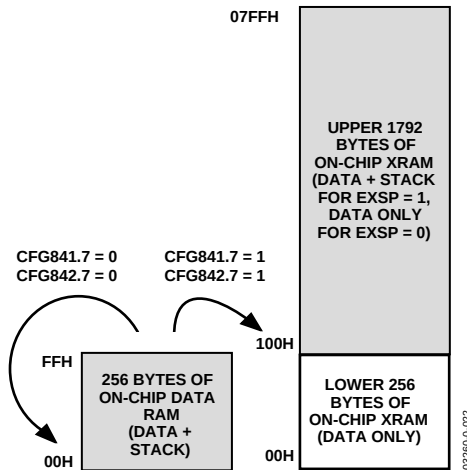


Figure 24. Extended Stack Pointer Operation

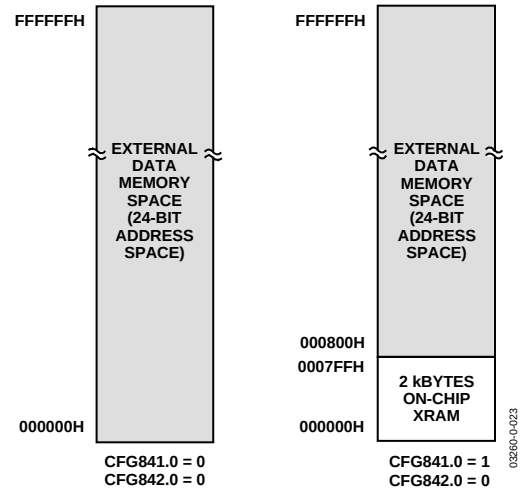


Figure 25. Internal and External XRAM

External Data Memory (External XRAM)

Just like a standard 8051 compatible core, the ADuC841/ADuC842/ADuC843 can access external data memory by using a MOVX instruction. The MOVX instruction automatically outputs the various control strobes required to access the data memory.

The parts, however, can access up to 16 MBytes of external data memory. This is an enhancement of the 64 kBytes of external data memory space available on a standard 8051 compatible core. The external data memory is discussed in more detail in the Hardware Design Considerations section.

Internal XRAM

The parts contain 2 kBytes of on-chip data memory. This memory, although on-chip, is also accessed via the MOVX instruction. The 2 kBytes of internal XRAM are mapped into the bottom 2 kBytes of the external address space if the CFG841/CFG842 bit is set. Otherwise, access to the external data memory occurs just like a standard 8051. When using the internal XRAM, Ports 0 and 2 are free to be used as general-purpose I/O.

SPECIAL FUNCTION REGISTERS (SFRS)

The SFR space is mapped into the upper 128 bytes of internal data memory space and is accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the parts via the SFR area is shown in Figure 26.

All registers, except the program counter (PC) and the four general-purpose register banks, reside in the SFR area. The SFR registers include control, configuration, and data registers, which provide an interface between the CPU and all on-chip peripherals.

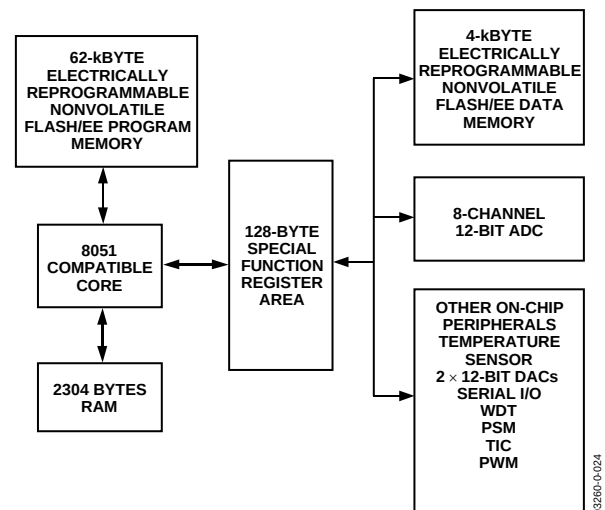


Figure 26. Programming Model

ADCCON1—(ADC Control SFR 1)

The ADCCON1 register controls conversion and acquisition times, hardware conversion modes, and power-down modes as detailed below.

SFR Address	EFH
SFR Power-On Default	40H
Bit Addressable	No

Table 8. ADCCON1 SFR Bit Designations

Bit No.	Name	Description															
7	MD1	The mode bit selects the active operating mode of the ADC. Set by the user to power up the ADC. Cleared by the user to power down the ADC.															
6	EXT_REF	Set by the user to select an external reference. Cleared by the user to use the internal reference.															
5	CK1	The ADC clock divide bits (CK1, CK0) select the divide ratio for the PLL master clock (ADuC842/ADuC843) or the external crystal (ADuC841) used to generate the ADC clock. To ensure correct ADC operation, the divider ratio must be chosen to reduce the ADC clock to 8.38 MHz or lower. A typical ADC conversion requires 16 ADC clocks plus the selected acquisition time. The divider ratio is selected as follows:															
4	CK0																
		<table> <tr> <th>CK1</th><th>CK0</th><th>MCLK Divider</th></tr> <tr> <td>0</td><td>0</td><td>32</td></tr> <tr> <td>0</td><td>1</td><td>4 (Do not use with a CD setting of 0)</td></tr> <tr> <td>1</td><td>0</td><td>8</td></tr> <tr> <td>1</td><td>1</td><td>2</td></tr> </table>	CK1	CK0	MCLK Divider	0	0	32	0	1	4 (Do not use with a CD setting of 0)	1	0	8	1	1	2
CK1	CK0	MCLK Divider															
0	0	32															
0	1	4 (Do not use with a CD setting of 0)															
1	0	8															
1	1	2															
3	AQ1	The ADC acquisition select bits (AQ1, AQ0) select the time provided for the input track-and-hold amplifier to acquire the input signal. An acquisition of three or more ADC clocks is recommended; clocks are as follows:															
2	AQ0																
		<table> <tr> <th>AQ1</th><th>AQ0</th><th>No. ADC Clks</th></tr> <tr> <td>0</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>2</td></tr> <tr> <td>1</td><td>0</td><td>3</td></tr> <tr> <td>1</td><td>1</td><td>4</td></tr> </table>	AQ1	AQ0	No. ADC Clks	0	0	1	0	1	2	1	0	3	1	1	4
AQ1	AQ0	No. ADC Clks															
0	0	1															
0	1	2															
1	0	3															
1	1	4															
1	T2C	The Timer 2 conversion bit (T2C) is set by the user to enable the Timer 2 overflow bit to be used as the ADC conversion start trigger input.															
0	EXC	The external trigger enable bit (EXC) is set by the user to allow the external Pin P3.5 ($\overline{\text{CONVST}}$) to be used as the active low convert start input. This input should be an active low pulse (minimum pulse width >100 ns) at the required sample rate.															

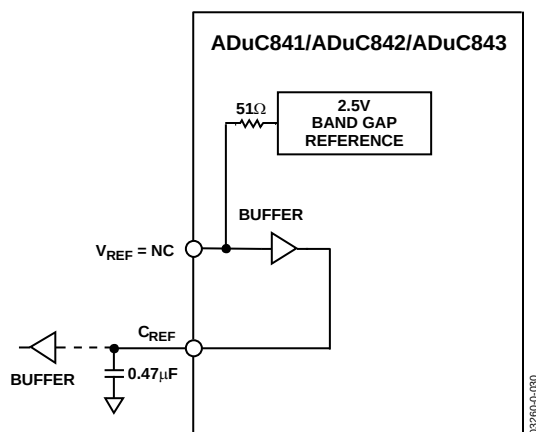
Table 12. Some Single-Supply Op Amps

Op Amp Model	Characteristics
OP281/OP481	Micropower
OP191/OP291/OP491	I/O Good up to V_{DD} , Low Cost
OP196/OP296/OP496	I/O to V_{DD} , Micropower, Low Cost
OP183/OP283	High Gain-Bandwidth Product
OP162/OP262/OP462	High GBP, Micro Package
AD820/AD822/AD824	FET Input, Low Cost
AD823	FET Input, High GBP

Keep in mind that the ADC transfer function is 0 V to V_{REF} , and that any signal range lost to amplifier saturation near ground impacts dynamic range. Though the op amps in Table 12 are capable of delivering output signals that very closely approach ground, no amplifier can deliver signals all the way to ground when powered by a single supply. Therefore, if a negative supply is available, you might consider using it to power the front end amplifiers. If you do, however, be sure to include the Schottky diodes shown in Figure 31 (or at least the lower of the two diodes) to protect the analog input from undervoltage conditions. To summarize this section, use the circuit in Figure 31 to drive the analog input pins of the parts.

Voltage Reference Connections

The on-chip 2.5 V band gap voltage reference can be used as the reference source for the ADC and DACs. To ensure the accuracy of the voltage reference, you must decouple the C_{REF} pin to ground with a 0.47 μ F capacitor, as shown in Figure 32. Note that this is different from the ADuC812/ADuC831/ADuC832.

Figure 32. Decoupling V_{REF} and C_{REF}

If the internal voltage reference is to be used as a reference for external circuitry, the C_{REF} output should be used. However, a buffer must be used in this case to ensure that no current is drawn from the C_{REF} pin itself. The voltage on the C_{REF} pin is that of an internal node within the buffer block, and its voltage is critical for ADC and DAC accuracy. The parts power up with their internal voltage reference in the off state.

If an external voltage reference is preferred, it should be connected to the C_{REF} pin as shown in Figure 33. Bit 6 of the ADCCON1 SFR must be set to 1 to switch in the external reference voltage.

To ensure accurate ADC operation, the voltage applied to C_{REF} must be between 1 V and AV_{DD} . In situations where analog input signals are proportional to the power supply (such as in some strain gage applications), it may be desirable to connect the C_{REF} pin directly to AV_{DD} . Operation of the ADC or DACs with a reference voltage below 1 V, however, may incur loss of accuracy, eventually resulting in missing codes or non-monotonicity. For that reason, do not use a reference voltage lower than 1 V.

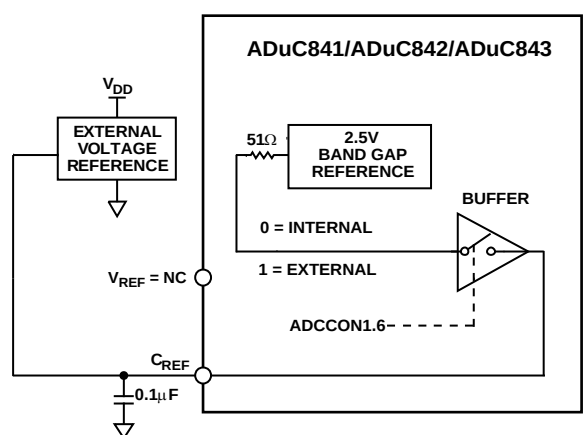


Figure 33. Using an External Voltage Reference

Configuring the ADC

The parts' successive approximation ADC is driven by a divided down version of the master clock. To ensure adequate ADC operation, this ADC clock must be between 400 kHz and 8.38 MHz. Frequencies within this range can be achieved easily with master clock frequencies from 400 kHz to well above 16 MHz, with the four ADC clock divide ratios to choose from. For example, set the ADC clock divide ratio to 8 (that is, $ADCCLK = 16.777216 \text{ MHz}/8 = 2 \text{ MHz}$) by setting the appropriate bits in ADCCON1 ($ADCCON1.5 = 1$, $ADCCON1.4 = 0$). The total ADC conversion time is 15 ADC clocks, plus 1 ADC clock for synchronization, plus the selected acquisition time (1, 2, 3, or 4 ADC clocks). For the preceding example, with a 3-clock acquisition time, total conversion time is 19 ADC clocks (or 9.05 μ s for a 2 MHz ADC clock).

In continuous conversion mode, a new conversion begins each time the previous one finishes. The sample rate is then simply the inverse of the total conversion time described previously. In the preceding example, the continuous conversion mode sample rate is 110.3 kHz.

Using the DAC

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier, the functional equivalent of which is illustrated in Figure 42. Features of this architecture include inherent guaranteed monotonicity and excellent differential linearity.

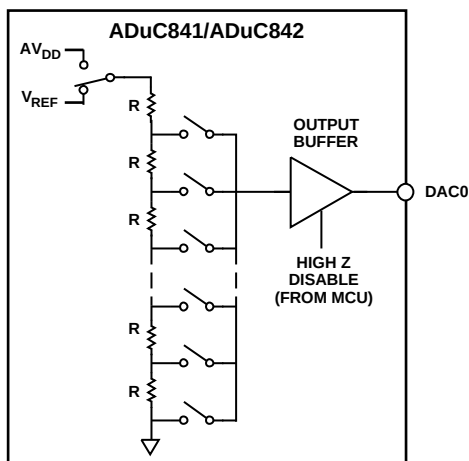


Figure 42. Resistor String DAC Functional Equivalent

As shown in Figure 42, the reference source for each DAC is user selectable in software. It can be either AV_{DD} or V_{REF} . In 0 V-to- AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0 V-to- V_{REF} mode, the DAC output transfer function spans from 0 V to the internal V_{REF} or, if an external reference is applied, the voltage at the C_{REF} pin. The DAC output buffer amplifier features a true rail-to-rail output stage implementation. This means that unloaded, each output is capable of swinging to within less than 100 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 10 k Ω resistive load to ground) is guaranteed through the full transfer function except Codes 0 to 100, and, in 0 V-to- AV_{DD} mode only, Codes 3995 to 4095. Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 43. The dotted line in Figure 43 indicates the ideal transfer function, and the solid line represents what the transfer function might look like with endpoint nonlinearities due to saturation of the output amplifier. Note that Figure 43 represents a transfer function in 0 V-to- V_{DD} mode only. In 0 V-to- V_{REF} mode (with $V_{REF} < V_{DD}$), the lower nonlinearity would be similar, but the upper portion of the transfer function would follow the ideal line right to the end (V_{REF} in this case, not V_{DD}), showing no signs of endpoint linearity errors.

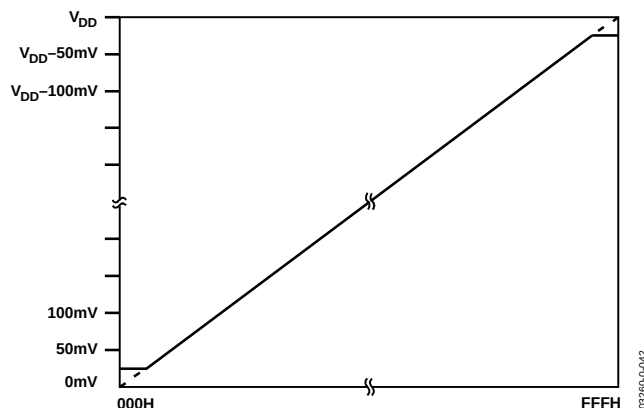


Figure 43. Endpoint Nonlinearities Due to Amplifier Saturation

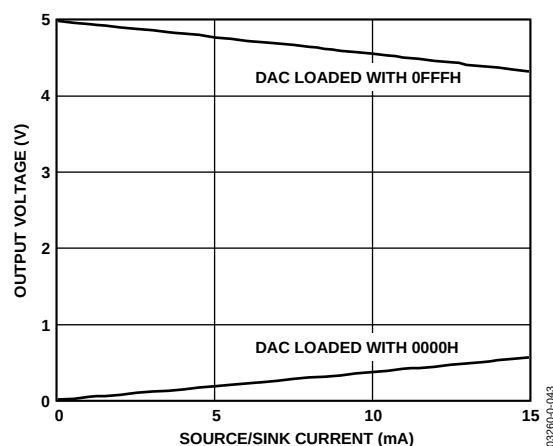


Figure 44. Source and Sink Current Capability with $V_{REF} = V_{DD} = 5$ V

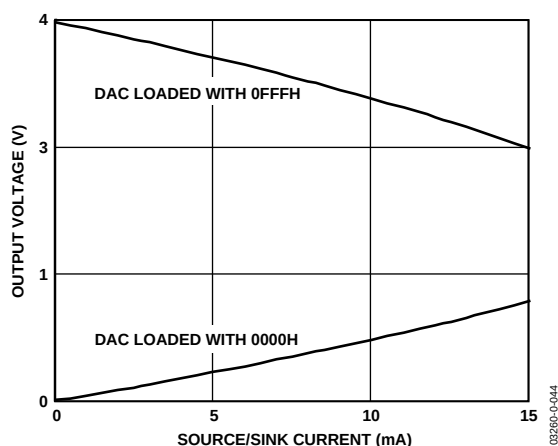


Figure 45. Source and Sink Current Capability with $V_{REF} = V_{DD} = 3$ V

ON-CHIP PLL

The ADuC842 and ADuC843 are intended for use with a 32.768 kHz watch crystal. A PLL locks onto a multiple (512) of this to provide a stable 16.78 MHz clock for the system. The ADuC841 operates directly from an external crystal. The core can operate at this frequency or at binary submultiples of it to allow power saving in cases where maximum core performance is not required. The default core clock is the PLL clock divided by 8 or 2.097152 MHz. The ADC clocks are also derived from the PLL clock, with the modulator rate being the same as the crystal oscillator frequency. The preceding choice of frequencies ensures that the modulators and the core are synchronous, regardless of the core clock rate. The PLL control register is PLLCON.

At 5 V the core clock can be set to a maximum of 16.78 MHz, while at 3 V the maximum core clock setting is 8.38 MHz. The CD bits should not be set to 0 on a 3 V part.

Note that on the ADuC841, changing the CD bits in PLLCON causes the core speed to change. The core speed is crystal freq/2^{CD}. The other bits in PLLCON are reserved in the case of the ADuC841 and should be written with 0.

PLLCON PLL	Control Register
SFR Address	D7H
Power-On Default	53H
Bit Addressable	No

Table 17. PLLCON SFR Bit Designations

Bit No.	Name	Description
7	OSC_PD	Oscillator Power-Down Bit. Set by the user to halt the 32 kHz oscillator in power-down mode. Cleared by the user to enable the 32 kHz oscillator in power-down mode. This feature allows the TIC to continue counting even in power-down mode.
6	LOCK	PLL Lock Bit. This is a read-only bit. Set automatically at power-on to indicate that the PLL loop is correctly tracking the crystal clock. If the external crystal subsequently becomes disconnected, the PLL rails. Cleared automatically at power-on to indicate that the PLL is not correctly tracking the crystal clock. This may be due to the absence of a crystal clock or an external crystal at power-on. In this mode, the PLL output can be 16.78 MHz $\pm 20\%$.
5	----	Reserved. Should be written with 0.
4	----	Reserved. Should be written with 0.
3	FINT	Fast Interrupt Response Bit. Set by the user enabling the response to any interrupt to be executed at the fastest core clock frequency, regardless of the configuration of the CD2–0 bits (see below). Once user code has returned from an interrupt, the core resumes code execution at the core clock selected by the CD2–0 bits. Cleared by the user to disable the fast interrupt response feature.
2	CD2	CPU (Core Clock) Divider Bits. This number determines the frequency at which the microcontroller core operates.
1	CD1	
0	CD0	
		CD2 CD1 CD0 Core Clock Frequency (MHz)
		0 0 0 16.777216
		0 0 1 8.388608
		0 1 0 4.194304
		0 1 1 2.097152 (Default Core Clock Frequency)
		1 0 0 1.048576
		1 0 1 0.524288
		1 1 0 0.262144
		1 1 1 0.131072

- An I²C slave can respond to repeated start conditions without a stop bit in between. This allows a master to change direction of transfer without giving up the bus. Note that the repeated start is detected only when a slave has previously been configured as a receiver.
- On-chip filtering rejects <50 ns spikes on the SDATA and the SCLOCK lines to preserve data integrity.

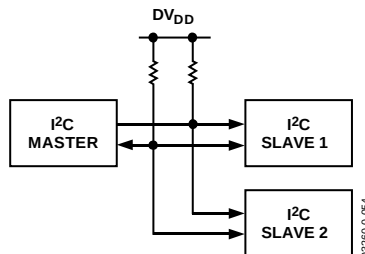


Figure 55. Typical I²C System

Software Master Mode

The ADuC841/ADuC842/ADuC843 can be used as I²C master devices by configuring the I²C peripheral in master mode and writing software to output the data bit by bit. This is referred to as a software master. Master mode is enabled by setting the I2CM bit in the I2CCON register.

To transmit data on the SDATA line, MDE must be set to enable the output driver on the SDATA pin. If MDE is set, the SDATA pin is pulled high or low depending on whether the MDO bit is set or cleared. MCO controls the SCLOCK pin and is always configured as an output in master mode. In master mode, the SCLOCK pin is pulled high or low depending on whether MCO is set or cleared.

To receive data, MDE must be cleared to disable the output driver on SDATA. Software must provide the clocks by toggling the MCO bit and reading the SDATA pin via the MDI bit. If MDE is cleared, MDI can be used to read the SDATA pin. The value of the SDATA pin is latched into MDI on a rising edge of SCLOCK. MDI is set if the SDATA pin was high on the last rising edge of SCLOCK. MDI is clear if the SDATA pin was low on the last rising edge of SCLOCK.

Software must control MDO, MCO, and MDE appropriately to generate the start condition, slave address, acknowledge bits, data bytes, and stop conditions. These functions are described in Application Note uC001.

Hardware Slave Mode

After reset, the ADuC841/ADuC842/ADuC843 default to hardware slave mode. The I²C interface is enabled by clearing the SPE bit in SPICON (this is not necessary if the MSPI bit is set). Slave mode is enabled by clearing the I2CM bit in I2CCON. The parts have a full hardware slave. In slave mode, the I²C address is stored in the I2CADD register. Data received or to be transmitted is stored in the I2CDAT register.

Once enabled in I²C slave mode, the slave controller waits for a start condition. If the part detects a valid start condition, followed by a valid address, followed by the R/W bit, the I2CI interrupt bit is automatically set by hardware. The I²C peripheral generates a core interrupt only if the user has pre-configured the I²C interrupt enable bit in the IEIP2 SFR as well as the global interrupt bit, EA, in the IE SFR. That is,

```
;Enabling I2C Interrupts for the ADuC842
MOV IEIP2,#01h           ; enable I2C interrupt
SETB EA
```

An autoclear of the I2CI bit is implemented on the parts so that this bit is cleared automatically on a read or write access to the I2CDAT SFR.

```
MOV I2CDAT, A             ; I2CI auto-cleared
MOV A, I2CDAT             ; I2CI auto-cleared
```

If for any reason the user tries to clear the interrupt more than once, that is, access the data SFR more than once per interrupt, then the I²C controller halts. The interface then must be reset using the I2CRS bit.

The user can choose to poll the I2CI bit or to enable the interrupt. In the case of the interrupt, the PC counter vectors to 003BH at the end of each complete byte. For the first byte, when the user gets to the I2CI ISR, the 7-bit address and the R/W bit appear in the I2CDAT SFR.

The I2CTX bit contains the R/W bit sent from the master. If I2CTX is set, the master is ready to receive a byte. Therefore the slave transmits data by writing to the I2CDAT register. If I2CTX is cleared, the master is ready to transmit a byte. Therefore the slave receives a serial byte. Software can interrogate the state of I2CTX to determine whether it must write to or read from I2CDAT.

Once the part has received a valid address, hardware holds SCLOCK low until the I2CI bit is cleared by software. This allows the master to wait for the slave to be ready before transmitting the clocks for the next byte.

The I2CI interrupt bit is set every time a complete data byte is received or transmitted, provided it is followed by a valid ACK. If the byte is followed by a NACK, an interrupt is not generated.

The part continues to issue interrupts for each complete data byte transferred until a stop condition is received or the interface is reset.

When a stop condition is received, the interface resets to a state in which it is waiting to be addressed (idle). Similarly, if the interface receives a NACK at the end of a sequence, it also returns to the default idle state. The I2CRS bit can be used to reset the I²C interface. This bit can be used to force the interface back to the default idle state.

TIME INTERVAL COUNTER (TIC)

A TIC is provided on-chip for counting longer intervals than the standard 8051 compatible timers are capable of. The TIC is capable of timeout intervals ranging from 1/128 second to 255 hours. Furthermore, this counter is clocked by the external 32.768 kHz crystal rather than by the core clock, and it has the ability to remain active in power-down mode and time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular widely spaced readings are required.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow clocks the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled. If the part is in power-down mode, again with TIC interrupt enabled, the TII bit wakes up the device and resumes code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described in Table 25. Note also that the time based SFRs can be written initially with the current time; the TIC can then be controlled and accessed by user software. In effect, this facilitates the implementation of a real-time clock. A block diagram of the TIC is shown in Figure 56.

The TIC is clocked directly from a 32 kHz external crystal on the [ADuC842/ADuC843](#) and by the internal 32 kHz $\pm 10\%$ R/C oscillator on the [ADuC841](#). Due to this, instructions that access the TIC registers are also clocked at this speed. The user should ensure that there is sufficient time between instructions to these registers to allow them to execute correctly.

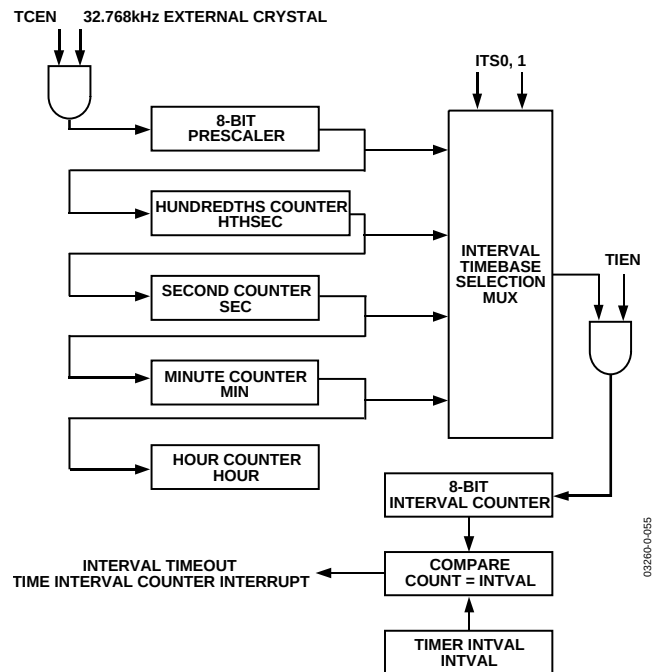


Figure 56. TIC, Simplified Block Diagram

INTVAL

Function

User Time Interval Select Register

User code writes the required time interval to this register. When the 8-bit interval counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled.

SFR Address

A6H

Power-On Default

00H

Bit Addressable

No

Valid Value

0 to 255 decimal

HTHSEC

Function

Hundredths Seconds Time Register

This register is incremented in 1/128 second intervals once TCEN in TIMECON is active. The HTHSEC SFR counts from 0 to 127 before rolling over to increment the SEC time register.

SFR Address

A2H

Power-On Default

00H

Bit Addressable

No

Valid Value

0 to 127 decimal

SEC

Function

Seconds Time Register

This register is incremented in 1-second intervals once TCEN in TIMECON is active. The SEC SFR counts from 0 to 59 before rolling over to increment the MIN time register.

SFR Address

A3H

Power-On Default

00H

Bit Addressable

No

Valid Value

0 to 59 decimal

MIN

Function

Minutes Time Register

This register is incremented in 1-minute intervals once TCEN in TIMECON is active. The MIN SFR counts from 0 to 59 before rolling over to increment the HOUR time register.

SFR Address

A4H

Power-On Default

00H

Bit Addressable

No

Valid Value

0 to 59 decimal

HOUR

Function

Hours Time Register

This register is incremented in 1-hour intervals once TCEN in TIMECON is active. The HOUR SFR counts from 0 to 23 before rolling over to 0.

SFR Address

A5H

Power-On Default

00H

Bit Addressable

No

Valid Value

0 to 23 decimal

In general-purpose I/O port mode, Port 2 pins that have 1s written to them are pulled high by the internal pull-ups (Figure 60) and, in that state, can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. Port 2 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 1.6 mA.

P2.6 and P2.7 can also be used as PWM outputs. When they are selected as the PWM outputs via the CFG841/CFG842 SFR, the PWM outputs overwrite anything written to P2.6 or P2.7.

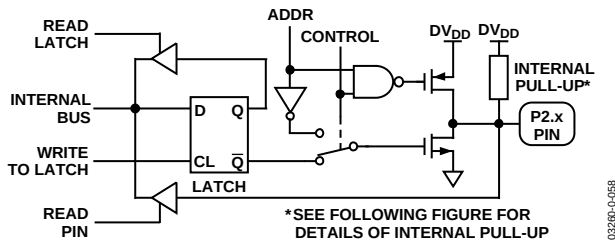


Figure 59. Port 2 Bit Latch and I/O Buffer

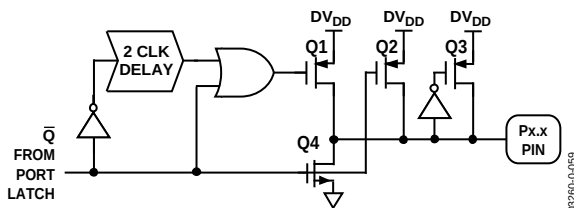


Figure 60. Internal Pull-Up Configuration

Port 3

Port 3 is a bidirectional port with internal pull-ups directly controlled via the P3 SFR. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and, in that state, can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-ups.

Port 3 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 4 mA. Port 3 pins also have various secondary functions as described in Table 27. The alternate functions of Port 3 pins can be activated only if the corresponding bit latch in the P3 SFR contains a 1. Otherwise, the port pin is stuck at 0.

Table 27. Port 3 Alternate Pin Functions

Pin No.	Alternate Function
P3.0	RxD (UART Input Pin) (or Serial Data I/O in Mode 0)
P3.1	TxD (UART Output Pin) (or Serial Clock Output in Mode 0)
P3.2	$\overline{\text{INT0}}$ (External Interrupt 0)
P3.3	$\overline{\text{INT1}}$ (External Interrupt 1)/PWM 1/MISO
P3.4	T0 (Timer/Counter 0 External Input) PWM External Clock/PWM 0
P3.5	T1 (Timer/Counter 1 External Input)
P3.6	$\overline{\text{WR}}$ (External Data Memory Write Strobe)
P3.7	$\overline{\text{RD}}$ (External Data Memory Read Strobe)

P3.3 and P3.4 can also be used as PWM outputs. When they are selected as the PWM outputs via the CFG841/CFG842 SFR, the PWM outputs overwrite anything written to P3.4 or P3.3.

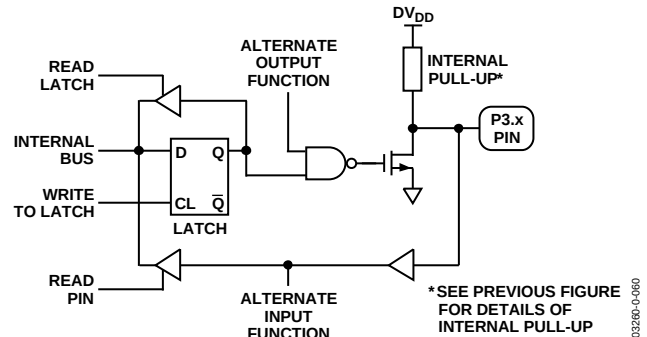


Figure 61. Port 3 Bit Latch and I/O Buffer

Additional Digital I/O

In addition to the port pins, the dedicated SPI/I²C pins (SCLOCK and SDATA/MOSI) also feature both input and output functions. Their equivalent I/O architectures are illustrated in Figure 62 and Figure 64, respectively, for SPI operation and in Figure 63 and Figure 65 for I²C operation. Notice that in I²C mode (SPE = 0), the strong pull-up FET (Q1) is disabled, leaving only a weak pull-up (Q2) present. By contrast, in SPI mode (SPE = 1) the strong pull-up FET (Q1) is controlled directly by SPI hardware, giving the pin push-pull capability.

In I²C mode (SPE = 0), two pull-down FETs (Q3 and Q4) operate in parallel to provide an extra 60% or 70% of current sinking capability. In SPI mode (SPE = 1), however, only one of the pull-down FETs (Q3) operates on each pin, resulting in sink capabilities identical to that of Port 0 and Port 2 pins. On the input path of SCLOCK, notice that a Schmitt trigger conditions the signal going to the SPI hardware to prevent false triggers (double triggers) on slow incoming edges. For incoming signals from the SCLOCK and SDATA pins going to I²C hardware, a filter conditions the signals to reject glitches of up to 50 ns in duration.

Notice also that direct access to the SCLOCK and SDATA/MOSI pins is afforded through the SFR interface in I²C master mode. Therefore, if you are not using the SPI or I²C functions, you can use these two pins to give additional high current digital outputs.

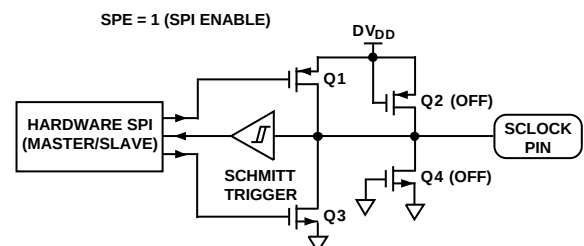


Figure 62. SCLOCK Pin I/O Functional Equivalent in SPI Mode

MOSI is shared with P3.3 and, as such, has the same configuration as the one shown in Figure 61.

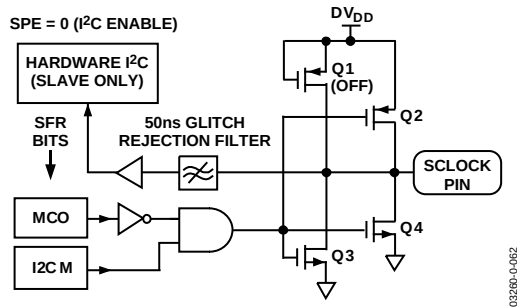


Figure 63. SCLOCK Pin I/O Functional Equivalent in I²C Mode

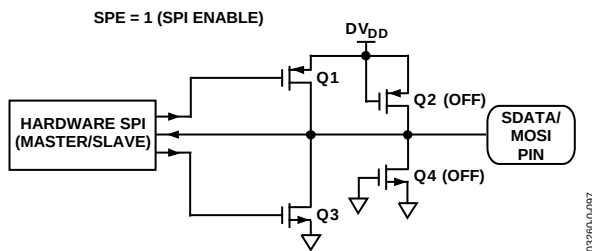


Figure 64. SDATA/MOSI Pin I/O Functional Equivalent in SPI Mode

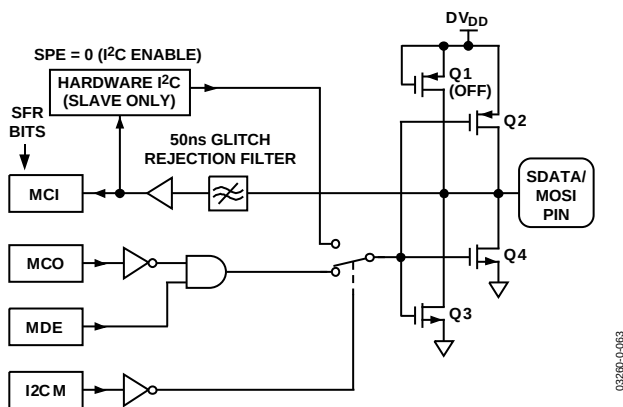


Figure 65. SDATA/MOSI Pin I/O Functional Equivalent in I²C Mode

Read-Modify-Write Instructions

Some 8051 instructions that read a port read the latch while others read the pin. The instructions that read the latch rather than the pins are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called read-modify-write instructions, which are listed below. When the destination operand is a port or a port bit, these instructions read the latch rather than the pin.

Table 28. Read-Write-Modify Instructions

Instruction	Description
ANL	Logical AND, for example, ANL P1, A
ORL	(Logical OR, for example, ORL P2, A
XRL	(Logical EX-OR, for example, XRL P3, A
JBC	Jump if Bit = 1 and clear bit, for example, JBC P1.1, LABEL
CPL	Complement bit, for example, CPL P3.0
INC	Increment, for example, INC P2
DEC	Decrement, for example, DEC P2
DJNZ	Decrement and Jump if Not Zero, for example, DJNZ P3, LABEL
MOV PX.Y, C ¹	Move Carry to Bit Y of Port X
CLR PX.Y ¹	Clear Bit Y of Port X
SETB PX.Y ¹	Set Bit Y of Port X

¹These instructions read the port byte (all 8 bits), modify the addressed bit, and then write the new byte back to the latch.

Read-modify-write instructions are directed to the latch rather than to the pin to avoid a possible misinterpretation of the voltage level of a pin. For example, a port pin might be used to drive the base of a transistor. When 1 is written to the bit, the transistor is turned on. If the CPU then reads the same port bit at the pin rather than the latch, it reads the base voltage of the transistor and interprets it as a Logic 0. Reading the latch rather than the pin returns the correct value of 1.

IEIP2	Secondary Interrupt Enable Register
SFR Address	A9H
Power-On Default	A0H
Bit Addressable	No

Table 38. IEIP2 SFR Bit Designations

Bit No.	Name	Description
7	----	Reserved.
6	PTI	Priority for time interval interrupt.
5	PPSM	Priority for power supply monitor interrupt.
4	PSI	Priority for SPI/I ² C interrupt.
3	----	This bit must contain zero.
2	ETI	Set by the user to enable, or cleared to disable time interval counter interrupts.
1	EPSMI	Set by the user to enable, or cleared to disable power supply monitor interrupts.
0	ESI	Set by the user to enable, or cleared to disable SPI or I ² C serial port interrupts.

Interrupt Priority

The interrupt enable registers are written by the user to enable individual interrupt sources, while the interrupt priority registers allow the user to select one of two priority levels for each interrupt. An interrupt of a high priority may interrupt the service routine of a low priority interrupt, and if two interrupts of different priority occur at the same time, the higher level interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed as shown in Table 39.

Table 39. Priority within an Interrupt Level

Source	Priority	Description
PSMI	1 (Highest)	Power Supply Monitor Interrupt.
WDS	2	Watchdog Timer Interrupt.
IE0	2	External Interrupt 0.
ADCI	3	ADC Interrupt.
TF0	4	Timer/Counter 0 Interrupt.
IE1	5	External Interrupt 1.
TF1	6	Timer/Counter 1 Interrupt.
ISPI/I ² CI	7	SPI Interrupt/I ² C Interrupt.
RI + TI	8	Serial Interrupt.
TF2 + EXF2	9	Timer/Counter 2 Interrupt.
TII	11(Lowest)	Time Interval Counter Interrupt.

Interrupt Vectors

When an interrupt occurs, the program counter is pushed onto the stack, and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown in Table 40.

Table 40. Interrupt Vector Addresses

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH
ADCI	0033H
ISPI/I ² CI	003BH
PSMI	0043H
TII	0053H
WDS	005BH

Parameter		16 MHz Core Clk		8 MHz Core Clock		Unit
		Min	Max	Min	Max	
t_{WLWH}	$\overline{WR}$ Pulse Width	65		130		ns
t_{AVLL}	Address Valid after ALE Low	60		120		ns
t_{LLAX}	Address Hold after ALE Low	65		135		ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low		130		260	ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	190		375		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	60		120		ns
t_{QVWH}	Data Setup before $\overline{WR}$	120		250		ns
t_{WHQX}	Data and Address Hold after $\overline{WR}$	380		755		ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	60		125		ns

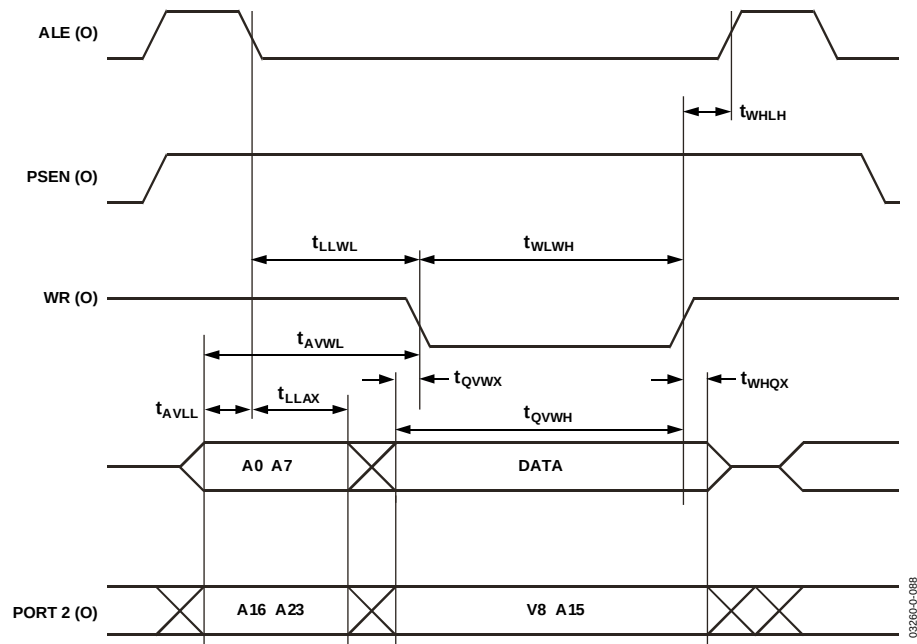


Figure 89. External Data Memory Write Cycle

Parameter		Min	Typ	Max	Unit
SPI MASTER MODE TIMING (CPHA = 1)					
t_{SL}	SCLOCK Low Pulse Width ¹		476		ns
t_{SH}	SCLOCK High Pulse Width ¹		476		ns
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

¹ Characterized under the following conditions:

- Core clock divider bits CD2, CD1, and CD0 bits in PLLCON SFR set to 0, 1, and 1, respectively, that is, core clock frequency = 2.09 MHz.
- SPI bit-rate selection bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

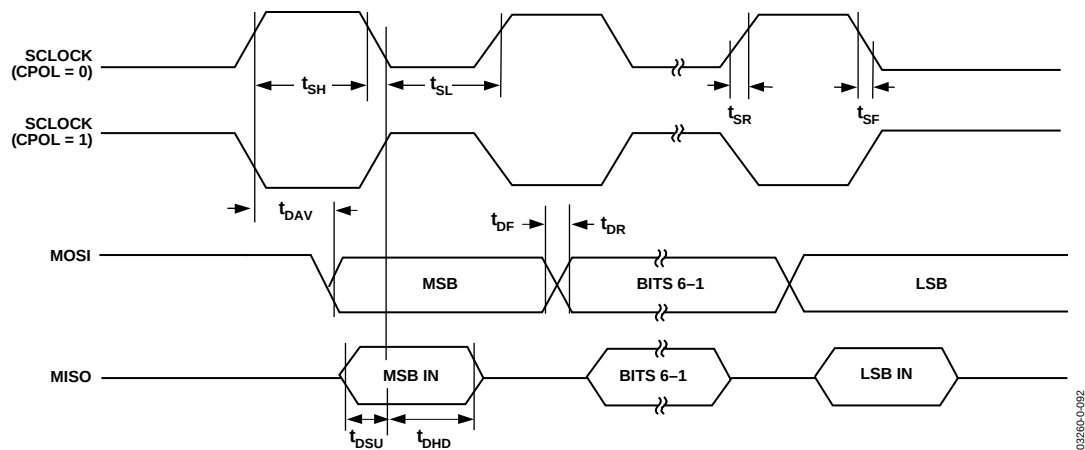


Figure 91. SPI Master Mode Timing (CPHA = 1)

Parameter		Min	Typ	Max	Unit
SPI MASTER MODE TIMING (CPHA = 0)					
t_{SL}	SCLOCK Low Pulse Width ¹		476		ns
t_{SH}	SCLOCK High Pulse Width ¹		476		ns
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t_{DOSU}	Data Output Setup before SCLOCK Edge			150	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

¹ Characterized under the following conditions:

- Core clock divider bits CD2, CD1, and CD0 bits in PLLCON SFR set to 0, 1, and 1, respectively, that is, core clock frequency = 2.09 MHz.
- SPI bit-rate selection bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

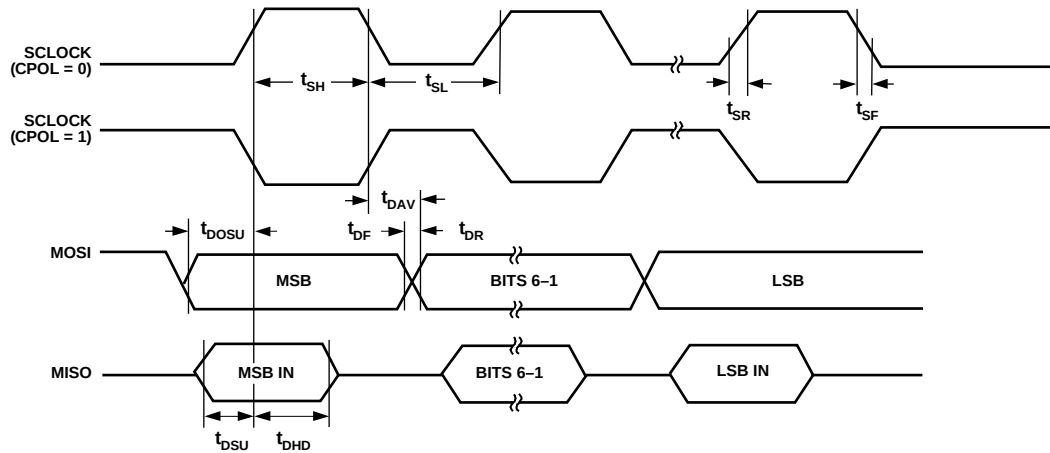


Figure 92. SPI Master Mode Timing (CPHA = 0)

03260-0-093

Parameter		Min	Typ	Max	Unit
SPI SLAVE MODE TIMING (CPHA = 1)					
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High after SCLOCK Edge	0			ns

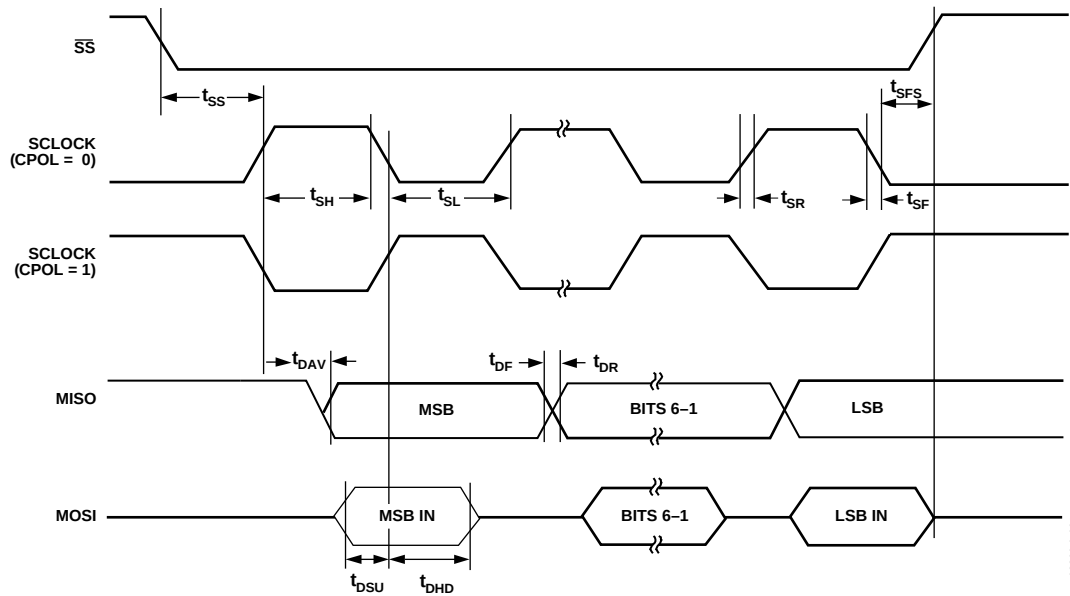


Figure 93. SPI Slave Mode Timing (CPHA = 1)