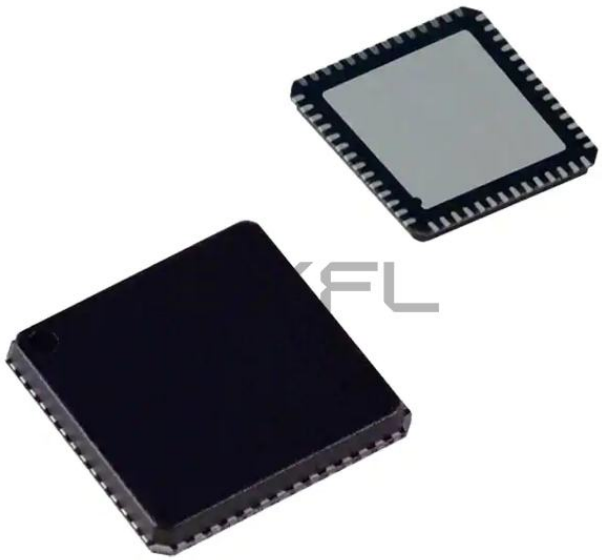

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	16.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, PSM, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc843bcpz8-5

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions/Comments
DAC AC CHARACTERISTICS				
Voltage Output Settling Time	15	15	µs typ	Full-scale settling time to within ½ LSB of final value
Digital-to-Analog Glitch Energy	10	10	nV-sec typ	1 LSB change at major carry
DAC CHANNEL SPECIFICATIONS[12, 13]				
Internal Buffer Disabled ADuC841/ADuC842 Only				
DC ACCURACY[10]				
Resolution	12	12	Bits	
Relative Accuracy	±3	±3	LSB typ	
Differential Nonlinearity[11]	–1	–1	LSB max	Guaranteed 12-bit monotonic
	±1/2	±1/2	LSB typ	
Offset Error	±5	±5	mV max	V_{REF} range
Gain Error	±0.5	±0.5	% typ	V_{REF} range
Gain Error Mismatch[4]	0.5	0.5	% typ	% of full-scale on DAC1
ANALOG OUTPUTS				
Voltage Range_0	0 to V_{REF}	0 to V_{REF}	V typ	DAC V_{REF} = 2.5 V
REFERENCE INPUT/OUTPUT REFERENCE OUTPUT[14]				
Output Voltage (V_{REF})	2.5	2.5	V	
Accuracy	±10	±10	mV Max	Of V_{REF} measured at the C_{REF} pin T_A = 25°C
Power Supply Rejection	65	67	dB typ	
Reference Temperature Coefficient	±15	±15	ppm/°C typ	
Internal V_{REF} Power-On Time	2	2	ms typ	
EXTERNAL REFERENCE INPUT[15]				
Voltage Range (V_{REF}) [4]	1	1	V min	
	V_{DD}	V_{DD}	V max	
Input Impedance	20	20	kΩ typ	
Input Leakage	1	1	µA max	Internal band gap deselected via ADCCON1.6
POWER SUPPLY MONITOR (PSM)				
DV_{DD} Trip Point Selection Range		2.93	V min	Two trip points selectable in this range programmed via TPD1–0 in PSMCON, 3 V part only
		3.08	V max	
DV_{DD} Power Supply Trip Point Accuracy		±2.5	% max	
WATCHDOG TIMER (WDT) [4]				
Timeout Period	0	0	ms min	Nine timeout periods selectable in this range
	2000	2000	ms max	
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS[16]				
Endurance[17]	100,000	100,000	Cycles min	
Data Retention[18]	100	100	Years min	
DIGITAL INPUTS				
Input Leakage Current (Port 0, $\overline{EA}$)	±10	±10	µA max	V_{IN} = 0 V or V_{DD}
	±1	±1	µA typ	V_{IN} = 0 V or V_{DD}
Logic 1 Input Current				
(All Digital Inputs), SDATA, SCLOCK	±10	±10	µA max	V_{IN} = V_{DD}
	±1	±1	µA typ	V_{IN} = V_{DD}
Logic 0 Input Current (Ports 1, 2, 3) SDATA, SCLOCK	–75	–25	µA max	
	–40	–15	µA typ	V_{IL} = 450 mV
Logic 1 to Logic 0 Transition Current (Ports 2 and 3)	–660	–250	µA max	V_{IL} = 2 V
	–400	–140	µA typ	V_{IL} = 2 V
RESET	±10	±10	µA max	V_{IN} = 0 V
	10	5	µA min	V_{IN} = 5 V, 3 V Internal Pull Down
	105	35	µA max	V_{IN} = 5 V, 3 V Internal Pull Down

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions/Comments
LOGIC INPUTS[4]				
INPUT VOLTAGES				
All Inputs Except SCLOCK, SDATA, RESET, and XTAL1				
VINL, Input Low Voltage	0.8	0.4	V max	
VINH, Input High Voltage	2.0	2.0	V min	
SDATA				
VINL, Input Low Voltage	0.8	0.8	V max	
VINH, Input High Voltage	2.0	2.0	V min	
SCLOCK and RESET ONLY[4]				
(Schmitt-Triggered Inputs)				
V_{T+}	1.3	0.95	V min	
	3.0	0.25	V max	
V_{T-}	0.8	0.4	V min	
	1.4	1.1	V max	
$V_{T+} - V_{T-}$	0.3	0.3	V min	
	0.85	0.85	V max	
CRYSTAL OSCILLATOR				
Logic Inputs, XTAL1 Only				
V_{INL}, Input Low Voltage	0.8	0.4	V typ	
V_{INH}, Input High Voltage	3.5	2.5	V typ	
XTAL1 Input Capacitance	18	18	pF typ	
XTAL2 Output Capacitance	18	18	pF typ	
MCU CLOCK RATE	16.78	8.38	MHz max	ADuC842/ADuC843 Only
	20	8.38	MHz max	ADuC841 Only
DIGITAL OUTPUTS				
Output High Voltage (V_{OH})	2.4		V min	V_{DD} = 4.5 V to 5.5 V
	4		V typ	I_{SOURCE} = 80 µA
		2.4	V min	V_{DD} = 2.7 V to 3.3 V
		2.6	V typ	I_{SOURCE} = 20 µA
Output Low Voltage (V_{OL})				
ALE, Ports 0 and 2	0.4	0.4	V max	I_{SINK} = 1.6 mA
	0.2	0.2	V typ	I_{SINK} = 1.6 mA
Port 3	0.4	0.4	V max	I_{SINK} = 4 mA
SCLOCK/SDATA	0.4	0.4	V max	I_{SINK} = 8 mA, I^2C Enabled
Floating State Leakage Current[4]	±10	±10	µA max	
	±1	±1	µA typ	
STARTUP TIME				At any core CLK
At Power-On	500	500	ms typ	
From Idle Mode	100	100	µs typ	
From Power-Down Mode				
Wake-up with $\overline{INT0}$ Interrupt	150	400	µs typ	
Wake-up with SPI/I^2C Interrupt	150	400	µs typ	
Wake-up with External RESET	150	400	µs typ	
After External RESET in Normal Mode	30	30	ms typ	
After WDT Reset in Normal Mode	3	3	ms typ	Controlled via WDCON SFR

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions/Comments
POWER REQUIREMENTS[19, 20]				
Power Supply Voltages				
AV_{DD}/DV_{DD} – AGND		2.7	V min	AV_{DD}/DV_{DD} = 3 V nom
		3.6	V max	
	4.75		V min	AV_{DD}/DV_{DD} = 5 V nom
	5.25		V max	
Power Supply Currents **Normal** Mode[21]				
DV_{DD} Current[4]	10	4.5	mA typ	Core CLK = 2.097 MHz
AV_{DD} Current	1.7	1.7	mA max	Core CLK = 2.097 MHz
DV_{DD} Current	38	12	mA max	Core CLK = 16.78MHz/8.38 MHz 5 V/3 V
	33	10	mA typ	Core CLK = 16.78MHz/8.38 MHz 5 V/3 V
AV_{DD} Current	1.7	1.7	mA max	Core CLK = 16.78MHz/8.38 MHz 5 V/3 V
DV_{DD} Current[4]	45	N/A	mA max	Core CLK = 20MHz **ADuC841 Only**
Power Supply Currents **Idle** Mode[21]				
DV_{DD} Current	4.5	2.2	mA typ	Core CLK = 2.097 MHz
AV_{DD} Current	3	2	µA typ	Core CLK = 2.097 MHz
DV_{DD} Current[4]	12	5	mA max	Core CLK = 16.78 MHz/8.38 MHz 5 V/3 V
	10	3.5	mA typ	Core CLK = 16.78 MHz/8.38 MHz 5 V/3 V
AV_{DD} Current	3	2	µA typ	Core CLK = 16.78 MHz/8.38 MHz 5 V/3 V
Power Supply Currents **Power-Down** Mode[21]				Core CLK = any frequency
DV_{DD} Current	28	18	µA max	Oscillator Off / TIMECON.1 = 0
	20	10	µA typ	
AV_{DD} Current	2	1	µA typ	Core CLK = any frequency, **ADuC841 Only**
DV_{DD} Current[4]	3	1	mA max	TIMECON.1 = 1
DV_{DD} Current[4]	50	22	µA max	Core CLK = any frequency
	40	15	µA typ	**ADuC842/ADuC843 Only,** oscillator on
Typical Additional Power Supply Currents				
PSM Peripheral	15	10	µA typ	AV_{DD} = DV_{DD}
ADC[4]	1.0	1.0	mA min	MCLK Divider = 32
	2.8	1.8	mA max	MCLK Divider = 2
DAC	150	130	µA typ	

See footnotes on the next page.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

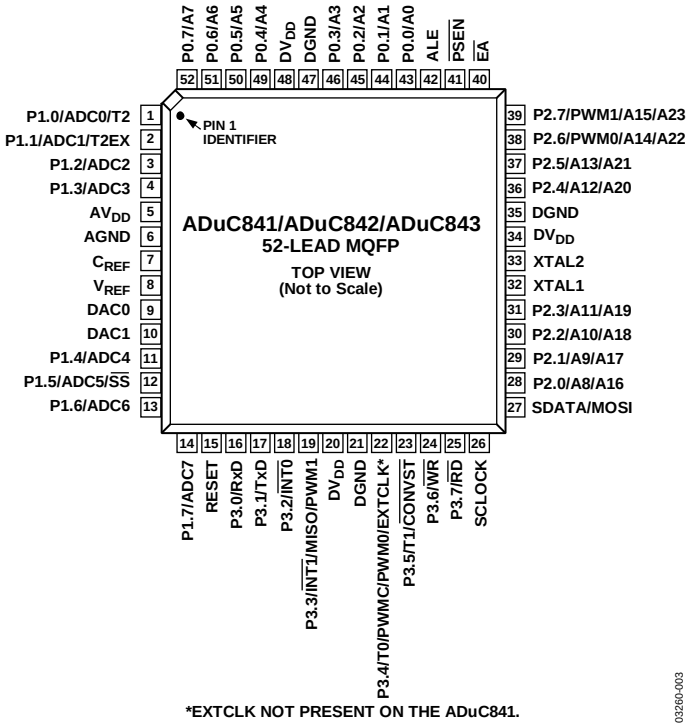

Figure 3. 52-Lead MQFP Pin Configuration

Table 3. 52-Lead MQFP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	P1.0/ADC0/T2	I	Input Port 1 (P1.0). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit. Single-Ended Analog Input (ADC0). Channel selection is via ADCCON2 SFR. Timer 2 Digital Input (T2). Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input.
2	P1.1/ADC1/T2EX	I	Input Port 1 (P1.1). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit. Single-Ended Analog Input 1 (ADC1). Channel selection is via ADCCON2 SFR. Capture/Reload Trigger for Counter 2 (T2EX). T2EX is a digital input. This pin also functions as an up/down control input for Counter 2.
3	P1.2/ADC2	I	Input Port 1 (P1.2). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit. Single-Ended Analog Input (ADC2). Channel selection is via ADCCON2 SFR.
4	P1.3/ADC3	I	Input Port 1 (P1.3). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit. Single-Ended Analog Input (ADC3). Channel selection is via ADCCON2 SFR.
5	AV_{DD}	P	Analog Positive Supply Voltage. 3 V or 5 V nominal.
6	AGND	G	Analog Ground. AGND is the ground reference point for the analog circuitry.
7	C_{REF}	I/O	Decoupling Input for On-Chip Reference. Connect a 0.47 µF capacitor between this pin and AGND.
8	V_{REF}	NC	Not Connected. This was a reference output on the ADuC812; use the C_{REF} pin instead.
9	DAC0	O	Voltage Output from DAC0. This pin is a no connect on the ADuC843.
10	DAC1	O	Voltage Output from DAC1. This pin is a no connect on the ADuC843.

Pin No.	Mnemonic	Type[1]	Description
11	P1.4/ADC4		Input Port 1 (P1.4). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit.
			Single-Ended Analog Input 4 (ADC4). Channel selection is via ADCCON2 SFR.
12	P1.5/ADC5/$\overline{SS}$	I	Input Port 1 (P1.5). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit.
			Single-Ended Analog Input 5 (ADC5). Channel selection is via ADCCON2 SFR.
			Slave Select Input for the SPI Interface ($\overline{SS}$).
13	P1.6/ADC6	I	Input Port 1 (P1.6). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit.
			Single-Ended Analog Input 6 (ADC6). Channel selection is via ADCCON2 SFR.
14	P1.7/ADC7	I	Input Port 1(P1.7). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit.
			Single-Ended Analog Input 7 (ADC7). Channel selection is via ADCCON2 SFR.
15	RESET	I	Reset. Digital Input. A high level on this pin for 24 master clock cycles while the oscillator is running resets the device.
16	P3.0/RxD	I/O	Input/Output Port 3 (P3.0). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.
			Receiver Data Input (Asynchronous) or Data Input/Output (Synchronous) of the Serial (UART) Port (RxD).
17	P3.1/TxD	I/O	Input/Output Port 3 (P3.1). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.
			Transmitter Data Output (Asynchronous) or Clock Output (Synchronous) of the Serial (UART) Port (TxD).
18	P3.2/$\overline{INT0}$	I/O	Input/Output Port 3 (P3.2). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.
			Interrupt 0 ($\overline{INT0}$). Programmable edge or level triggered interrupt input; can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 0.
19	P3.3/$\overline{INT1}$/MISO/PWM1	I/O	Input/Output Port 3 (P3.3). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.
			Interrupt 1 ($\overline{INT1}$). Programmable edge or level triggered interrupt input; can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 1.
			SPI Master Input/Slave Output Data I/O Pin for SPI Serial Interface (MISO).
			PWM 1 Voltage Output (PWM1). See the CFG841/CFG842 register for further information.
20, 34, 48	DV_{DD}	P	Digital Positive Supply Voltage. 3 V or 5 V nominal.
21, 35, 47	DGND	G	Digital Ground. DGND is the ground reference point for the digital circuitry.

Pin No.	Mnemonic	Type[1]	Description
43	P0.0/A0	I/O	Input/Output Port 0 (P0.0). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A0). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
44	P0.1/A1	I/O	Input/Output Port 0 (P0.1). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A1). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
45	P0.2/A2	I/O	Input/Output Port 0 (P0.2). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A2). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
46	P0.3/A3	I/O	Input/Output Port 0 (P0.3).Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A3). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
49	P0.4/A4	I/O	Input/Output Port 0 (P0.4). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A4). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
50	P0.5/A5	I/O	Input/Output Port 0 (P0.5). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A5). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
51	P0.6/A6	I/O	Input/Output Port 0 (P0.6). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A6). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.
52	P0.7/A7	I/O	Input/Output Port 0 (P0.7). Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high impedance inputs. External Memory Address (A7). Port 0 is also the multiplexed low order address and data bus during accesses to external data memory. In this application, it uses strong internal pull-up resistors when emitting 1s.

[1] P = power, G = ground, I= input, O = output., NC = no connect.

Pin No.	Mnemonic	Type[1]	Description
24	P3.4/T0/PWMC/PWM0/EXTCLK	I/O	Input/Output Port 3 (P3.4). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. Timer/Counter 0 Input (T0). PWM Clock Input (PWMC). PWM 0 Voltage Output (PWM0). PWM outputs can be configured to use Port 2.6 and Port 2.7 or Port 3.4 and Port 3.3. Input for External Clock Signal (EXTCLK). This pin function must be enabled via the CFG842 register.
25	P3.5/T1/$\overline{\text{CONVST}}$	I/O	Input/Output Port 3 (P3.5). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. Timer/Counter 1 Input (T1). Active Low Convert Start Logic Input for the ADC Block when the External Convert Start Function is Enabled ($\overline{\text{CONVST}}$). A low to high transition on this input puts the track-and-hold into hold mode and starts the conversion.
26	P3.6/$\overline{\text{WR}}$	I/O	Input/Output Port 3 (P3.6). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. Write Control Signal, Logic Output ($\overline{\text{WR}}$). Latches the data byte from Port 0 into the external data memory.
27	P3.7/$\overline{\text{RD}}$	I/O	Input/Output Port 3 (P3.7). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. Read Control Signal, Logic Output ($\overline{\text{RD}}$). Enables the external data memory to Port 0.
28	SCLOCK	I/O	Serial Clock Pin for I^2C-Compatible Clock or for SPI Serial Interface Clock.
29	SDATA/MOSI	I/O	User Selectable, I^2C Compatible, or SPI Data Input/Output Pin (SDATA). SPI Master Output/Slave Input Data I/O Pin for SPI Interface (MOSI).
30	P2.0/A8/A16	I/O	Input/Output Port 2 (P2.0). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A8). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A16). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
31	P2.1/A9/A17	I/O	Input/Output Port 2 (P2.1). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A9). Port 2 emits the middle order address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A17). Port 2 emits the high order address byte during accesses to the external 24-bit external data memory space.
32	P2.2/A10/A18	I/O	Input/Output Port 2 (P2.2). Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. External Memory Addresses (A10). Port 2 emits the middle address byte during accesses to the external 24-bit external data memory space. External Memory Addresses (A18). Port 2 emits the high-order address byte during accesses to the external 24-bit external data memory space.

TYPICAL PERFORMANCE CHARACTERISTICS

The typical performance plots presented in this section illustrate typical performance of the ADuC841/ADuC842/ADuC843 under various operating conditions.

Figure 5 and Figure 6 show typical ADC integral nonlinearity (INL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and is operating at a sampling rate of 152 kHz; the typical worst-case errors in both plots are just less than 0.3 LSB. Figure 7 and Figure 8 also show ADC INL at a higher sampling rate of 400 kHz. Figure 9 and Figure 10 show the variation in worst-case positive (WCP) INL and worst-case negative (WCN) INL versus external reference input voltage.

Figure 11 and Figure 12 show typical ADC differential nonlinearity (DNL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and is operating at a sampling rate of 152 kHz; the typical worst-case errors in both plots are just less than 0.2 LSB. Figure 13 and Figure 14 show the variation in worst-case positive (WCP) DNL and worst-case negative (WCN) DNL versus external reference input voltage.

Figure 15 shows a histogram plot of 10,000 ADC conversion results on a dc input with V_{DD} = 5 V. The plot illustrates an excellent code distribution pointing to the low noise performance of the on-chip precision ADC.

Figure 16 shows a histogram plot of 10,000 ADC conversion results on a dc input for V_{DD} = 3 V. The plot again illustrates a very tight code distribution of 1 LSB with the majority of codes appearing in one output pin.

Figure 17 and Figure 18 show typical FFT plots for the parts. These plots were generated using an external clock input. The ADC is using its internal reference (2.5 V), sampling a full-scale, 10 kHz sine wave test tone input at a sampling rate of 149.79 kHz. The resulting FFTs shown at 5 V and 3 V supplies illustrate an excellent 100 dB noise floor, 71 dB signal-to-noise ratio (SNR), and THD greater than –80 dB.

Figure 19 and Figure 20 show typical dynamic performance versus external reference voltages. Again, excellent ac performance can be observed in both plots with some roll-off being observed as V_{REF} falls below 1 V.

Figure 21 shows typical dynamic performance versus sampling frequency. SNR levels of 71 dB are obtained across the sampling range of the parts.

Figure 22 shows the voltage output of the on-chip temperature sensor versus temperature. Although the initial voltage output at 25°C can vary from part to part, the resulting slope of −1. 4 mV/°C is constant across all parts.

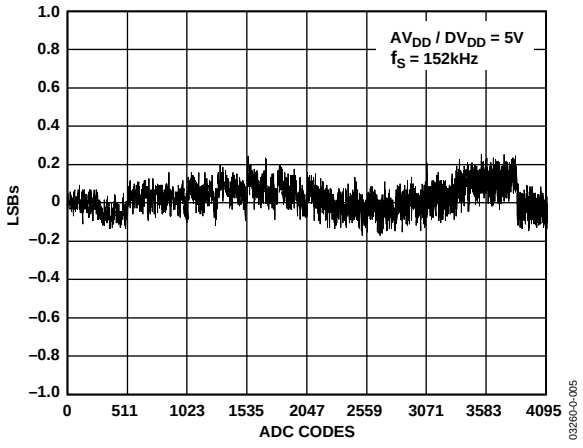

Figure 5. Typical INL Error, V_{DD} = 5 V, f_s = 152 kHz

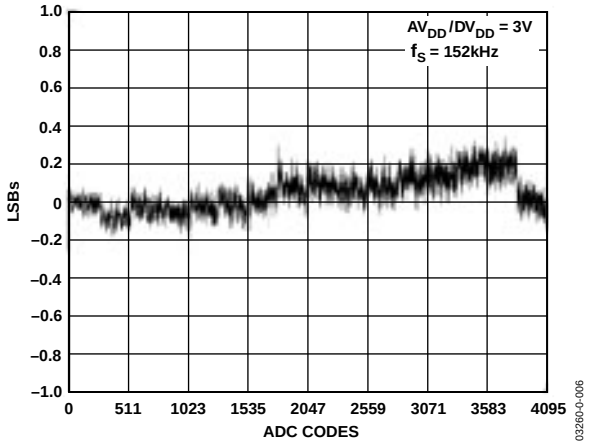

Figure 6. Typical INL Error, V_{DD} = 3 V, f_s = 152 kHz

ACCUMULATOR SFR (ACC)

ACC is the accumulator register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions refer to the accumulator as A.

B SFR (B)

The B register is used with the ACC for multiplication and division operations. For other instructions, it can be treated as a general-purpose scratchpad register.

Stack Pointer (SP and SPH)

The SP SFR is the stack pointer and is used to hold an internal RAM address that is called the top of the stack. The SP register is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the SP register is initialized to 07H after a reset, which causes the stack to begin at location 08H.

As mentioned earlier, the parts offer an extended 11-bit stack pointer. The 3 extra bits used to make up the 11-bit stack pointer are the 3 LSBs of the SPH byte located at B7H.

Data Pointer (DPTR)

The data pointer is made up of three 8-bit registers named DPP (page byte), DPH (high byte), and DPL (low byte). These are used to provide memory addresses for internal and external code access and for external data access. They may be manipulated as a 16-bit register (DPTR = DPH, DPL), although INC DPTR instructions automatically carry over to DPP, or as three independent 8-bit registers (DPP, DPH, DPL). The parts support dual data pointers. Refer to the Dual Data Pointer section.

Program Status Word (PSW)

The PSW SFR contains several bits reflecting the current status of the CPU, as detailed in Table 6.

SFR Address	D0H
Power-On Default	00H
Bit Addressable	Yes

Table 6. PSW SFR Bit Designations

Bit	Name	Description		
7	CY	Carry Flag.		
6	AC	Auxiliary Carry Flag.		
5	F0	General-Purpose Flag.		
4	RS1	Register Bank Select Bits.		
3	RS0	RS1	RS0	Selected Bank
		0	0	0
		0	1	1
		1	0	2
		1	1	3
2	OV	Overflow Flag.		
1	F1	General-Purpose Flag.		
0	P	Parity Bit.		

Power Control SFR (PCON)

The PCON SFR contains bits for power-saving options and general-purpose status flags, as shown in Table 7.

SFR Address	87H
Power-On Default	00H
Bit Addressable	No

Table 7. PCON SFR Bit Designations

Bit No.	Name	Description
7	SMOD	Double UART Baud Rate.
6	SERIPD	I^2C/SPI Power-Down Interrupt Enable.
5	INT0PD	$\overline{INT0}$ Power-Down Interrupt Enable.
4	ALEOFF	Disable ALE Output.
3	GF1	General-Purpose Flag Bit.
2	GF0	General-Purpose Flag Bit.
1	PD	Power-Down Mode Enable.
0	IDL	Idle Mode Enable.

The ADC incorporates a successive approximation architecture (SAR) involving a charge-sampled input stage. Figure 30 shows the equivalent circuit of the analog input section. Each ADC conversion is divided into two distinct phases, as defined by the position of the switches in Figure 30. During the sampling phase (with SW1 and SW2 in the track position), a charge proportional to the voltage on the analog input is developed across the input sampling capacitor. During the conversion phase (with both switches in the hold position), the capacitor DAC is adjusted via internal SAR logic until the voltage on Node A is 0, indicating that the sampled charge on the input capacitor is balanced out by the charge being output by the capacitor DAC. The final digital value contained in the SAR is then latched out as the result of the ADC conversion. Control of the SAR and timing of acquisition and sampling modes is handled automatically by built-in ADC control logic. Acquisition and conversion times are also fully configurable under user control.

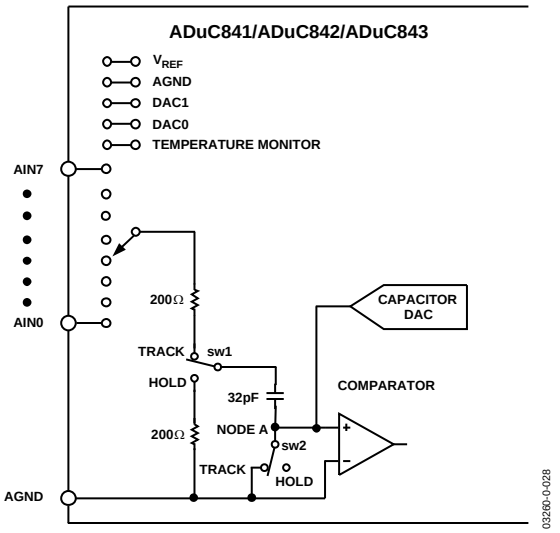

Figure 30. Internal ADC Structure

Note that whenever a new input channel is selected, a residual charge from the 32 pF sampling capacitor places a transient on the newly selected input. The signal source must be capable of recovering from this transient before the sampling switches go into hold mode. Delays can be inserted in software (between channel selection and conversion request) to account for input stage settling, but a hardware solution alleviates this burden from the software design task and ultimately results in a cleaner system implementation. One hardware solution is to choose a very fast settling op amp to drive each analog input. Such an op amp would need to fully settle from a small signal transient in less than 300 ns in order to guarantee adequate settling under all software configurations. A better solution, recommended for use with any amplifier, is shown in Figure 31. Though at first glance the circuit in Figure 31 may look like a simple antialiasing filter, it actually serves no such purpose since its corner frequency is well above the Nyquist frequency, even at a 200 kHz sample rate. Though the R/C does help to reject some incoming high frequency noise, its primary function is to ensure that the transient demands of the ADC input stage are met.

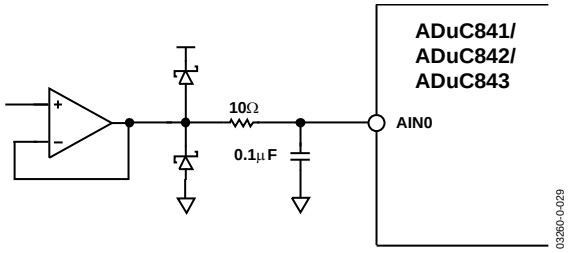

Figure 31. Buffering Analog Inputs

It does so by providing a capacitive bank from which the 32 pF sampling capacitor can draw its charge. Its voltage does not change by more than one count (1/4096) of the 12-bit transfer function when the 32 pF charge from a previous channel is dumped onto it. A larger capacitor can be used if desired, but not a larger resistor (for reasons described below). The Schottky diodes in Figure 31 may be necessary to limit the voltage applied to the analog input pin per the Absolute Maximum Ratings. They are not necessary if the op amp is powered from the same supply as the part since in that case the op amp is unable to generate voltages above V_{DD} or below ground. An op amp of some kind is necessary unless the signal source is very low impedance to begin with. DC leakage currents at the parts' analog inputs can cause measurable dc errors with external source impedances as low as 100 Ω or so. To ensure accurate ADC operation, keep the total source impedance at each analog input less than 61 Ω. The Table 11 illustrates examples of how source impedance can affect dc accuracy.

Table 11. Source Impedance and DC Accuracy

Source Impedance Ω	Error from 1 μA Leakage Current	Error from 10 μA Leakage Current
61	61 μV = 0.1 LSB	610 μV = 1 LSB
610	610 μV = 1 LSB	6.1 mV = 10 LSB

Although Figure 31 shows the op amp operating at a gain of 1, one can, of course, configure it for any gain needed. Also, one can just as easily use an instrumentation amplifier in its place to condition differential signals. Use an amplifier that is capable of delivering the signal (0 V to V_{REF}) with minimal saturation. Some single-supply rail-to-rail op amps that are useful for this purpose are described in Table 12. Check Analog Devices website www.analog.com for details on these and other op amps and instrumentation amps.

User Download Mode (ULOAD)

Figure 39 shows that it is possible to use the 62 kBytes of Flash/EE program memory available to the user as a single block of memory. In this mode, all of the Flash/EE memory is read-only to user code.

However, the Flash/EE program memory can also be written to during runtime simply by entering ULOAD mode. In ULOAD mode, the lower 56 kBytes of program memory can be erased and reprogrammed by user software as shown in Figure 39. ULOAD mode can be used to upgrade your code in the field via any user defined download protocol. By configuring the SPI port on the part as a slave, it is possible to completely reprogram the 56 kBytes of Flash/EE program memory in only 5 seconds (refer to Application Note uC007).

Alternatively, ULOAD mode can be used to save data to the 56 kBytes of Flash/EE memory. This can be extremely useful in data logging applications where the part can provide up to 60 kBytes of NV data memory on chip (4 kBytes of dedicated Flash/EE data memory also exist).

The upper 6 kBytes of the 62 kBytes of Flash/EE program memory are programmable only via serial download or parallel programming. This means that this space appears as read-only to user code. Therefore, it cannot be accidentally erased or reprogrammed by erroneous code execution, which makes it very suitable to use the 6 kBytes as a bootloader.

A bootload enable option exists in the serial downloader to "always run from E000H after reset." If using a bootloader, this option is recommended to ensure that the bootloader always executes correct code after reset. Programming the Flash/EE program memory via ULOAD mode is described in more detail in the description of ECON and in Application Note uC007.

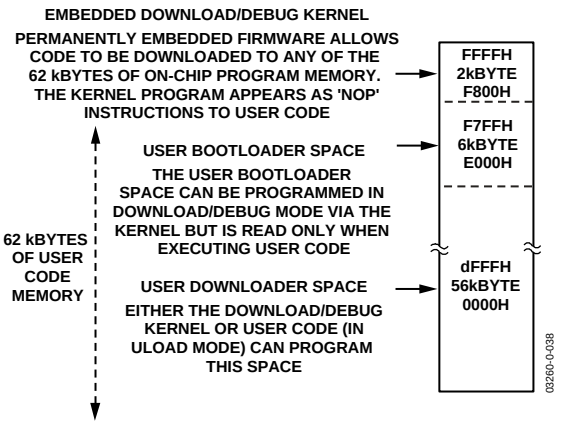

Figure 39. Flash/EE Program Memory Map in ULOAD Mode (62 kByte Part)

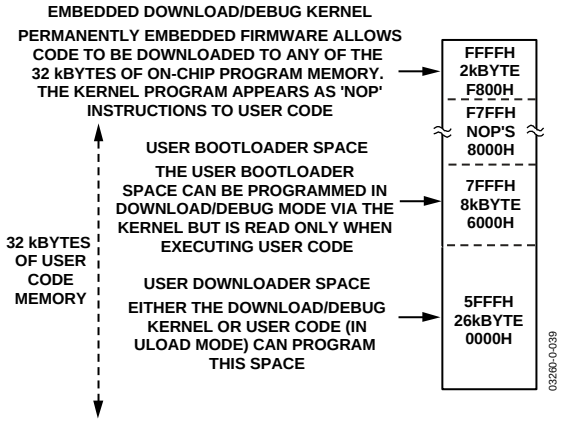

Figure 40. Flash/EE Program Memory Map in ULOAD Mode (32 kByte Part)

Flash/EE Program Memory Security

The ADuC841/ADuC842/ADuC843 facilitate three modes of Flash/EE program memory security. These modes can be independently activated, restricting access to the internal code space. These security modes can be enabled as part of serial download protocol as described in Application Note uC004 or via parallel programming. The security modes available on the parts are as follows:

Lock Mode

This mode locks the code memory, disabling parallel programming of the program memory. However, reading the memory in parallel mode and reading the memory via a MOVC command from external memory is still allowed. This mode is deactivated by initiating a code-erase command in serial download or parallel programming modes.

Secure Mode

This mode locks code in memory, disabling parallel programming (program and verify/read commands) as well as disabling the execution of a MOVC instruction from external memory, which is attempting to read the op codes from internal memory. Read/write of internal data Flash/EE from external memory is also disabled. This mode is deactivated by initiating a code-erase command in serial download or parallel programming modes.

Serial Safe Mode

This mode disables serial download capability on the device. If serial safe mode is activated and an attempt is made to reset the part into serial download mode, that is, $\overline{\text{RESET}}$ asserted and de-asserted with $\overline{\text{PSEN}}$ low, the part interprets the serial download reset as a normal reset only. It therefore cannot enter serial download mode but can only execute as a normal reset sequence. Serial safe mode can be disabled only by initiating a code-erase command in parallel programming mode.

Using the DAC

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier, the functional equivalent of which is illustrated in Figure 42. Features of this architecture include inherent guaranteed monotonicity and excellent differential linearity.

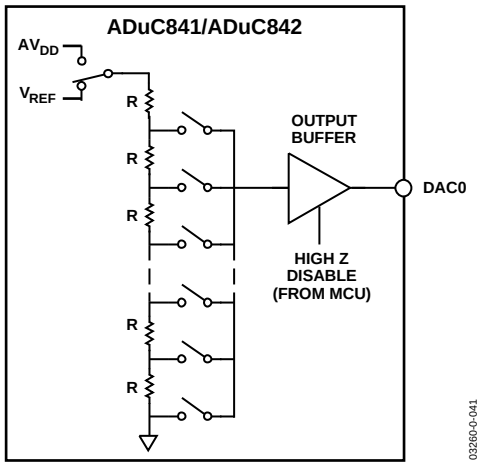

Figure 42. Resistor String DAC Functional Equivalent

As shown in Figure 42, the reference source for each DAC is user selectable in software. It can be either AV_{DD} or V_{REF}. In 0 V-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0 V-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal V_{REF} or, if an external reference is applied, the voltage at the C_{REF} pin. The DAC output buffer amplifier features a true rail-to-rail output stage implementation. This means that unloaded, each output is capable of swinging to within less than 100 mV of both AVDD and ground. Moreover, the DAC's linearity specification (when driving a 10 kΩ resistive load to ground) is guaranteed through the full transfer function except Codes 0 to 100, and, in 0 V-to-AVDD mode only, Codes 3995 to 4095. Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 43. The dotted line in Figure 43 indicates the ideal transfer function, and the solid line represents what the transfer function might look like with endpoint nonlinearities due to saturation of the output amplifier. Note that Figure 43 represents a transfer function in 0 V-to-V_{DD} mode only. In 0 V-to-V_{REF} mode (with $V_{REF} < V_{DD}$), the lower nonlinearity would be similar, but the upper portion of the transfer function would follow the ideal line right to the end (V_{REF} in this case, not V_{DD}), showing no signs of endpoint linearity errors.

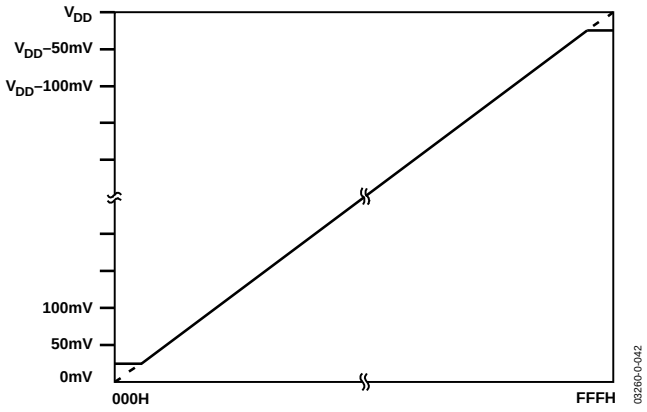

Figure 43. Endpoint Nonlinearities Due to Amplifier Saturation

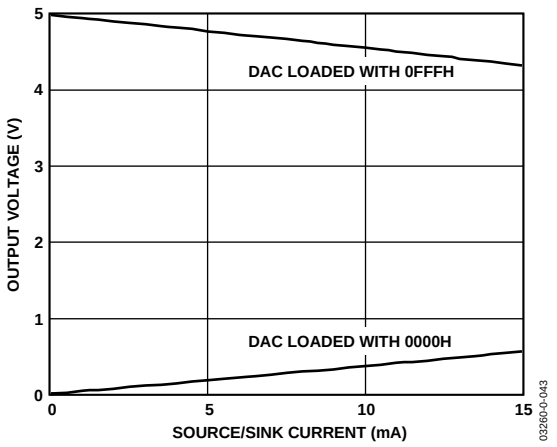

Figure 44. Source and Sink Current Capability with $V_{REF} = V_{DD} = 5$ V

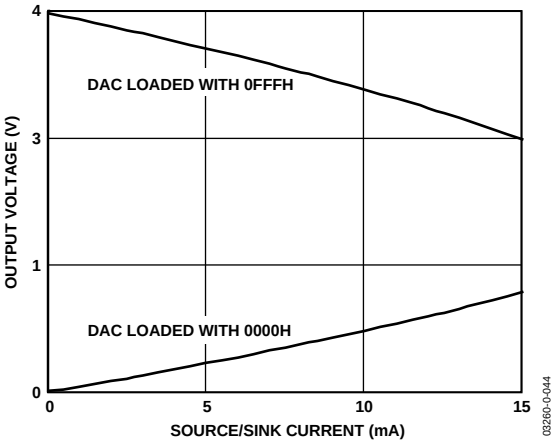

Figure 45. Source and Sink Current Capability with $V_{REF} = V_{DD} = 3$ V

Mode 4: Dual NRZ 16-Bit Σ-Δ DAC

Mode 4 provides a high speed PWM output similar to that of a Σ-Δ DAC. Typically, this mode is used with the PWM clock equal to 16.777216 MHz. In this mode, P2.6 and P2.7 are updated every PWM clock (60 ns in the case of 16 MHz). Over any 65536 cycles (16-bit PWM) PWM0 (P2.6) is high for PWM0H/L cycles and low for (65536 – PWM0H/L) cycles. Similarly, PWM1 (P2.7) is high for PWM1H/L cycles and low for (65536 – PWM1H/L) cycles.

For example, if PWM1H is set to 4010H (slightly above one quarter of FS), then P2.7 is typically low for three clocks and high for one clock (each clock is approximately 60 ns). Over every 65536 clocks, the PWM compensates for the fact that the output should be slightly above one quarter of full scale by having a high cycle followed by only two low cycles.

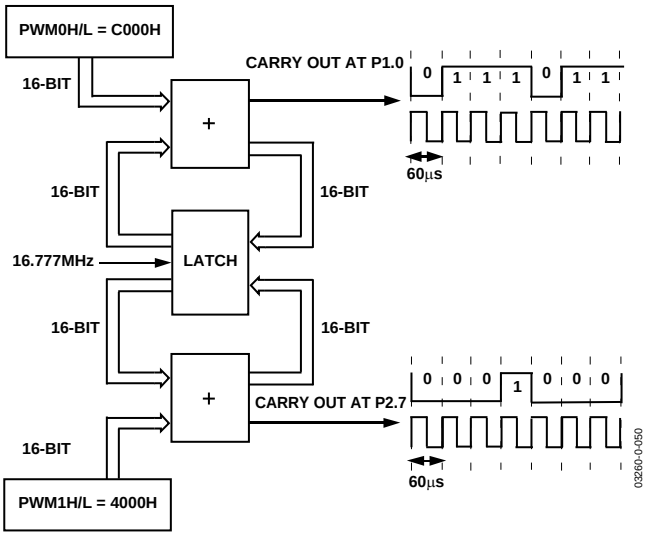

Figure 51. PWM Mode 4

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required. If, for example, only 12-bit performance is required, write 0s to the four LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 4.096 kHz. Similarly writing 0s to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 65 kHz.

Mode 5: Dual 8-Bit PWM

In Mode 5, the duty cycle of the PWM outputs and the resolution of the PWM outputs are individually programmable. The maximum resolution of the PWM output is 8 bits. The output resolution is set by the PWM1L and PWM1H SFRs for the P2.6 and P2.7 outputs, respectively. PWM0L and PWM0H sets the duty cycles of the PWM outputs at P2.6 and P2.7, respectively. Both PWMs have the same clock source and clock divider.

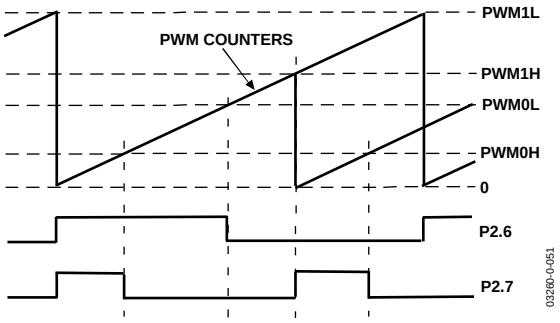

Figure 52. PWM Mode 5

Mode 6: Dual RZ 16-Bit Σ-Δ DAC

Mode 6 provides a high speed PWM output similar to that of a Σ-Δ DAC. Mode 6 operates very similarly to Mode 4. However, the key difference is that Mode 6 provides return-to-zero (RZ) Σ-Δ DAC output. Mode 4 provides non-return-to-zero Σ-Δ DAC outputs. The RZ mode ensures that any difference in the rise and fall times do not affect the Σ-Δ DAC INL. However, the RZ mode halves the dynamic range of the Σ-Δ DAC outputs from 0 V–AV_{DD} down to 0 V–AV_{DD}/2. For best results, this mode should be used with a PWM clock divider of 4.

If PWM1H is set to 4010H (slightly above one quarter of FS), P2.7 is typically low for three full clocks (3 × 60 ns), high for half a clock (30 ns), and then low again for half a clock (30 ns) before repeating itself. Over every 65536 clocks, the PWM compensates for the fact that the output should be slightly above one quarter of full scale by leaving the output high for two half clocks in four. The rate at which this happens depends on the value and degree of compensation required.

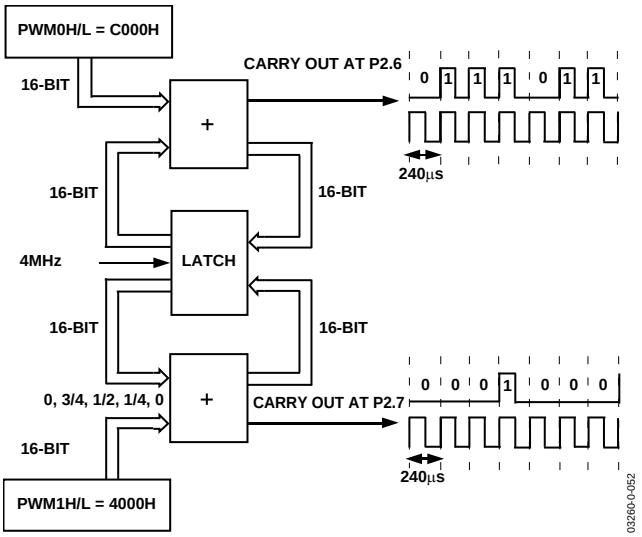

Figure 53. PWM Mode 6

SPICON SPI Control Register

SFR Address	F8H
Power-On Default	04H
Bit Addressable	Yes

Table 19. SPICON SFR Bit Designations

Bit No.	Name	Description
7	ISPI	SPI Interrupt Bit. Set by the MicroConverter at the end of each SPI transfer. Cleared directly by user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by the MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by user code.
5	SPE	SPI Interface Enable Bit. Set by the user to enable the SPI interface. Cleared by the user to enable the I^2C pins, this is not requiredto enable the I^2C interface if the MSPI bit is set in CFG841/CFG842. In this case, the I^2C interface is automatically enabled.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by the user to enable master mode operation (SCLOCK is an output). Cleared by the user to enable slave mode operation (SCLOCK is an input).
3	CPOL[1]	Clock Polarity Select Bit. Set by the user if SCLOCK idles high. Cleared by the user if SCLOCK idles low.
2	CPHA[1]	Clock Phase Select Bit. Set by the user if leading SCLOCK edge is to transmit data. Cleared by the user if trailing SCLOCK edge is to transmit data.
1	SPR1	SPI Bit Rate Select Bits.
0	SPR0	These bits select the SCLOCK rate (bit rate) in master mode as follows: SPR1 SPR0 Selected Bit Rate 0 0 $f_{osc}/2$ 0 1 $f_{osc}/4$ 1 0 $f_{osc}/8$ 1 1 $f_{osc}/16$ In SPI slave mode, that is, SPIM = 0, the logic level on the external $\overline{SS}$ pin can be read via the SPR0 bit.

[1]The CPOL and CPHA bits should both contain the same values for master and slave devices.

SPIDAT	**SPI Data Register**
Function	SPIDAT SFR is written by the user to transmit data over the SPI interface or read by user code to read data just received by the SPI interface.
SFR Address	F7H
Power-On Default	00H
Bit Addressable	No

DUAL DATA POINTER

The ADuC841/ADuC842/ADuC843 incorporate two data pointers. The second data pointer is a shadow data pointer and is selected via the data pointer control SFR (DPCON). DPCON also includes some useful features such as automatic hardware post-increment and post-decrement as well as automatic data pointer toggle. DPCON is described in Table 22.

DPCON	Data Pointer Control SFR
SFR Address	A7H
Power-On Default	00H
Bit Addressable	No

Table 22. DPCON SFR Bit Designations

Bit No.	Name	Description
7	----	Reserved.
6	DPT	Data Pointer Automatic Toggle Enable. Cleared by the user to disable autoswapping of the DPTR. Set in user software to enable automatic toggling of the DPTR after each each MOVX or MOVC instruction.
5	DP1m1	Shadow Data Pointer Mode.
4	DP1m0	These two bits enable extra modes of the shadow data pointer's operation, allowing for more compact and more efficient code size and execution. m1 m0 Behavior of the shadow data pointer. 0 0 8052 behavior. 0 1 DPTR is post-incremented after a MOVX or a MOVC instruction. 1 0 DPTR is post-decremented after a MOVX or MOVC instruction. 1 1 DPTR LSB is toggled after a MOVX or MOVC instruction. (This instruction can be useful for moving 8-bit blocks to/from 16-bit devices.)
3	DP0m1	Main Data Pointer Mode.
2	DP0m0	These two bits enable extra modes of the main data pointer operation, allowing for more compact and more efficient code size and execution. m1 m0 Behavior of the main data pointer. 0 0 8052 behavior. 0 1 DPTR is post-incremented after a MOVX or a MOVC instruction. 1 0 DPTR is post-decremented after a MOVX or MOVC instruction. 1 1 DPTR LSB is toggled after a MOVX or MOVC instruction. (This instruction can be useful for moving 8-bit blocks to/from 16-bit devices.)
1	----	This bit is not implemented to allow the INC DPCON instruction toggle the data pointer without incrementing the rest of the SFR.
0	DPSEL	Data Pointer Select. Cleared by the user to select the main data pointer. This means that the contents of this 24-bit register are placed into the three SFRs: DPL, DPH, and DPP. Set by the user to select the shadow data pointer. This means that the contents of a separate 24-bit register appears in the three SFRs: DPL, DPH, and DPP.

Note 1: This is the only place where the main and shadow data pointers are distinguished. Everywhere else in this data sheet wherever the DPTR is mentioned, operation on the active DPTR is implied.

Note 2: Only MOVC/MOVX @DPTR instructions are relevant above. MOVC/MOVX PC/@Ri instructions do not cause the DPTR to automatically post increment/decrement, and so on.

To illustrate the operation of DPCON, the following code copies 256 bytes of code memory at address D000H into XRAM starting from Address 0000H.

```
    MOV DPTR,#0          ; Main DPTR = 0
    MOV DPCON,#55H       ; Select shadow DPTR
                         ; DPTR1 increment mode,
                         ; DPTR0 increment mode
                         ; DPTR auto toggling ON
    MOV DPTR,#0D000H     ; Shadow DPTR = D000H
MOVELOOP:
    CLR A
    MOVC A,@A+DPTR       ; Get data
                         ; Post Inc DPTR
                         ; Swap to Main DPTR (Data)
    MOVX @DPTR,A         ; Put ACC in XRAM
                         ; Increment main DPTR
                         ; Swap Shadow DPTR (Code)
    MOV A, DPL
    JNZ MOVELOOP
```

MOSI is shared with P3.3 and, as such, has the same configuration as the one shown in Figure 61.

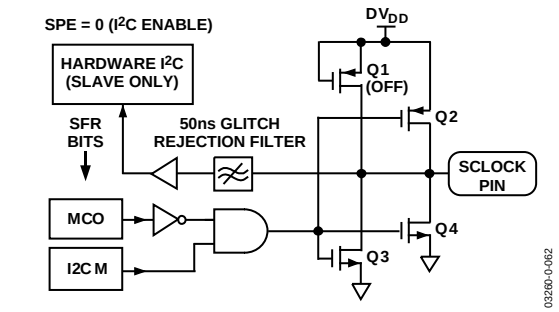

Figure 63. SCLOCK Pin I/O Functional Equivalent in I²C Mode

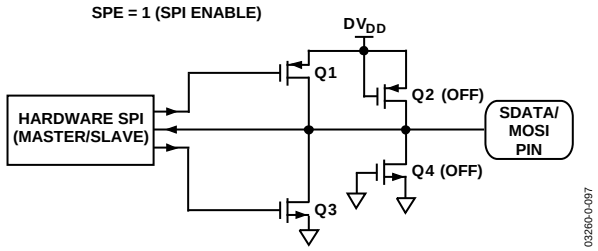

Figure 64. SDATA/MOSI Pin I/O Functional Equivalent in SPI Mode

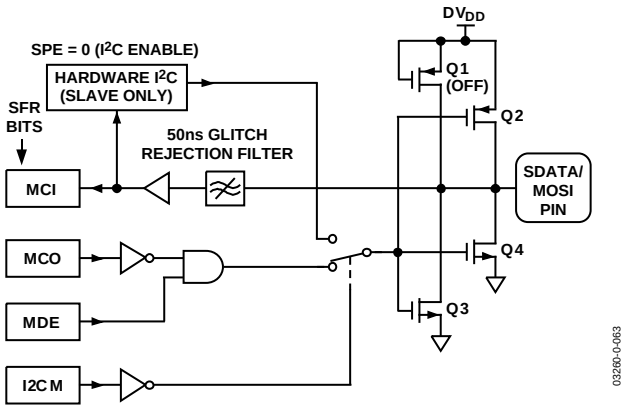

Figure 65. SDATA/MOSI Pin I/O Functional Equivalent in I²C Mode

Read-Modify-Write Instructions

Some 8051 instructions that read a port read the latch while others read the pin. The instructions that read the latch rather than the pins are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called read-modify-write instructions, which are listed below. When the destination operand is a port or a port bit, these instructions read the latch rather than the pin.

Table 28. Read-Write-Modify Instructions

Instruction	Description
ANL	Logical AND, for example, ANL P1, A
ORL	(Logical OR, for example, ORL P2, A
XRL	(Logical EX-OR, for example, XRL P3, A
JBC	Jump if Bit = 1 and clear bit, for example, JBC P1.1, LABEL
CPL	Complement bit, for example, CPL P3.0
INC	Increment, for example, INC P2
DEC	Decrement, for example, DEC P2
DJNZ	Decrement and Jump if Not Zero, for example, DJNZ P3, LABEL
MOV PX.Y, C[1]	Move Carry to Bit Y of Port X
CLR PX.Y[1]	Clear Bit Y of Port X
SETB PX.Y[1]	Set Bit Y of Port X

[1] These instructions read the port byte (all 8 bits), modify the addressed bit, and then write the new byte back to the latch.

Read-modify-write instructions are directed to the latch rather than to the pin to avoid a possible misinterpretation of the voltage level of a pin. For example, a port pin might be used to drive the base of a transistor. When 1 is written to the bit, the transistor is turned on. If the CPU then reads the same port bit at the pin rather than the latch, it reads the base voltage of the transistor and interprets it as a Logic 0. Reading the latch rather than the pin returns the correct value of 1.

TIMER/COUNTER 0 AND 1 OPERATING MODES

The following sections describe the operating modes for Timer/Counters 0 and 1. Unless otherwise noted, assume that these modes of operation are the same for both Timer 0 and Timer 1.

Mode 0 (13-Bit Timer/Counter)

Mode 0 configures an 8-bit timer/counter. Figure 66 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single-cycle core.

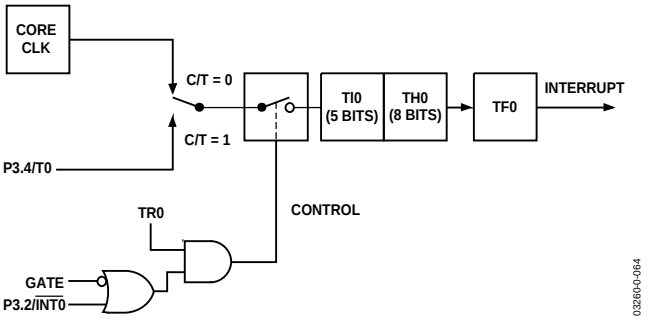

Figure 66. Timer/Counter 0, Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulse-width measurements. TR0 is a control bit in the special function register TCON; Gate is in TMOD. The 13-bit register consists of all 8 bits of TH0 and the lower five bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the Mode 1 timer register is running with all 16 bits. Mode 1 is shown in Figure 67.

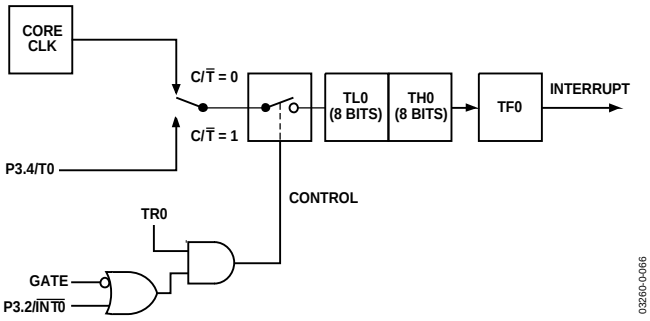

Figure 67. Timer/Counter 0, Mode 1

Mode 2 (8-Bit Timer/Counter with Autoreload)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload, as shown in Figure 68. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

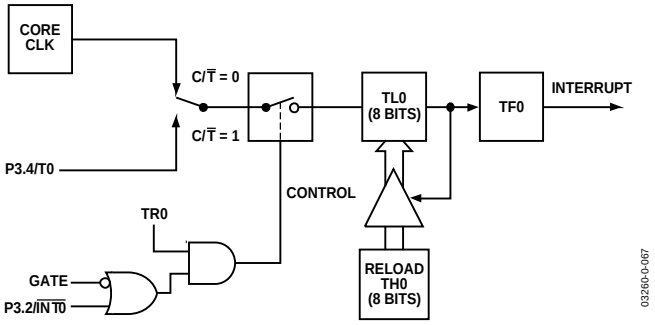

Figure 68. Timer/Counter 0, Mode 2

Mode 3 (Two 8-Bit Timer/Counters)

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 69. TL0 uses the Timer 0 control bits: C/$\overline{T}$, Gate, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can still be used by the serial interface as a baud rate generator. In fact, it can be used in any application not requiring an interrupt from Timer 1 itself.

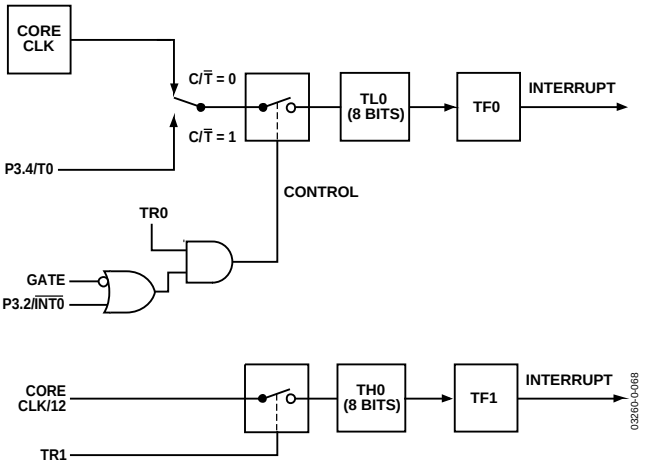

Figure 69. Timer/Counter 0, Mode 3

T2CON	Timer/Counter 2 Control Register
SFR Address	C8H
Power-On Default	00H
Bit Addressable	Yes

Table 31. T2CON SFR Bit Designations

Bit No.	Name	Description
7	TF2	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 cannot be set when either RCLK = 1 or TCLK = 1. Cleared by user software.
6	EXF2	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. Cleared by user software.
5	RCLK	Receive Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the receive clock.
4	TCLK	Transmit Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the transmit clock.
3	EXEN2	Timer 2 External Enable Flag. Set by the user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by the user for Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 Start/Stop Control Bit. Set by the user to start Timer 2. Cleared by the user to stop Timer 2.
1	CNT2	Timer 2 Timer or Counter Function Select Bit. Set by the user to select counter function (input from external T2 pin). Cleared by the user to select timer function (input from on-chip core clock).
0	CAP2	Timer 2 Capture/Reload Select Bit. Set by the user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by the user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Timer/Counter 2 Data Registers

Timer/Counter 2 also has two pairs of 8-bit data registers associated with it. These are used as both timer data registers and as timer capture/reload registers.

TH2 and TL2

Timer 2, data high byte and low byte.
SFR Address = CDH, CCH, respectively.

RCAP2H and RCAP2L

Timer 2, capture/reload byte and low byte.
SFR Address = CBH, CAH, respectively.

INTERRUPT SYSTEM

The ADuC841/ADuC842/ADuC843 provide a total of nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

IE	Interrupt Enable Register
IP	Interrupt Priority Register
IEIP2	Secondary Interrupt Enable Register

IE	**Interrupt Enable Register**
SFR Address	A8H
Power-On Default	00H
Bit Addressable	Yes

Table 36. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Set by the user to enable, or cleared to disable all interrupt sources.
6	EADC	Set by the user to enable, or cleared to disable ADC interrupts.
5	ET2	Set by the user to enable, or cleared to disable Timer 2 interrupts.
4	ES	Set by the user to enable, or cleared to disable UART serial port interrupts.
3	ET1	Set by the user to enable, or cleared to disable 0 Timer 1 interrupts.
2	EX1	Set by the user to enable, or cleared to disable External Interrupt 1.
1	ET0	Set by the user to enable, or cleared to disable Timer 0 interrupts.
0	EX0	Set by the user to enable, or cleared to disable External Interrupt 0 .

IP	**Interrupt Priority Register**
SFR Address	B8H
Power-On Default	00H
Bit Addressable	Yes

Table 37. IP SFR Bit Designations

Bit No.	Name	Description
7	----	Reserved.
6	PADC	Written by the user to select the ADC interrupt priority (1 = High; 0 = Low).
5	PT2	Written by the user to select the Timer 2 interrupt priority (1 = High; 0 = Low).
4	PS	Written by the user to select the UART serial port interrupt priority (1 = High; 0 = Low).
3	PT1	Written by the user to select the Timer 1 interrupt priority (1 = High; 0 = Low).
2	PX1	Written by the user to select External Interrupt 1 priority (1 = High; 0 = Low).
1	PT0	Written by the user to select the Timer 0 interrupt priority (1 = High; 0 = Low).
0	PX0	Written by the user to select External Interrupt 0 priority (1 = High; 0 = Low).

Parameter		Min	Typ	Max	Unit
SPI SLAVE MODE TIMING (CPHA = 1)					
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High after SCLOCK Edge	0			ns

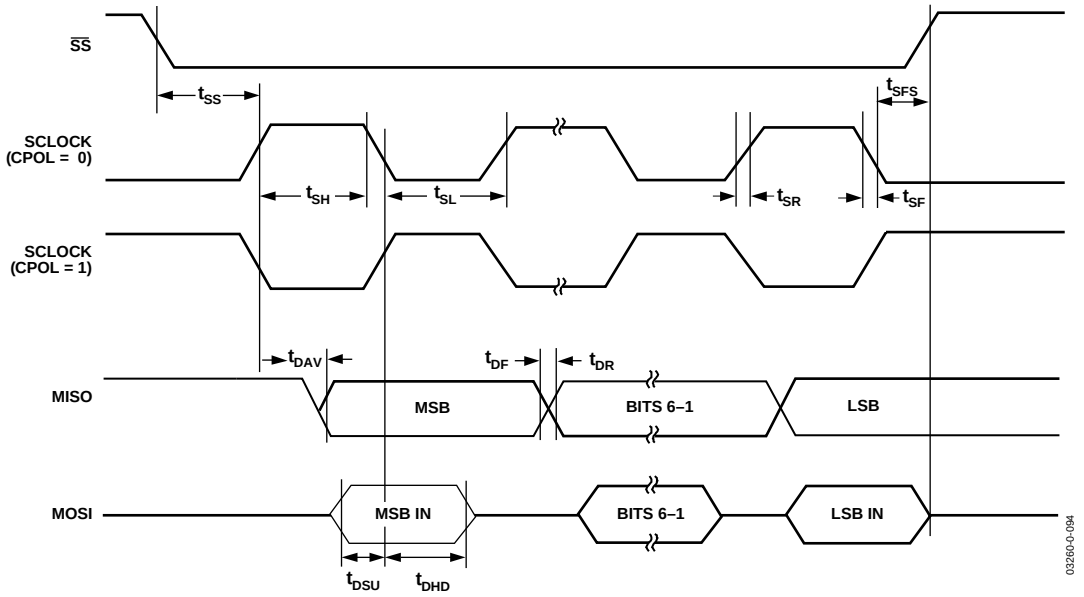

Figure 93. SPI Slave Mode Timing (CPHA = 1)