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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	16.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, PSM, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	80-PQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc843bsz62-5

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions/Comments
DAC AC CHARACTERISTICS				
Voltage Output Settling Time	15	15	µs typ	Full-scale settling time to within ½ LSB of final value
Digital-to-Analog Glitch Energy	10	10	nV-sec typ	1 LSB change at major carry
DAC CHANNEL SPECIFICATIONS[12, 13]				
Internal Buffer Disabled ADuC841/ADuC842 Only				
DC ACCURACY[10]				
Resolution	12	12	Bits	
Relative Accuracy	±3	±3	LSB typ	
Differential Nonlinearity[11]	–1	–1	LSB max	Guaranteed 12-bit monotonic
	±1/2	±1/2	LSB typ	
Offset Error	±5	±5	mV max	V_{REF} range
Gain Error	±0.5	±0.5	% typ	V_{REF} range
Gain Error Mismatch[4]	0.5	0.5	% typ	% of full-scale on DAC1
ANALOG OUTPUTS				
Voltage Range_0	0 to V_{REF}	0 to V_{REF}	V typ	DAC V_{REF} = 2.5 V
REFERENCE INPUT/OUTPUT REFERENCE OUTPUT[14]				
Output Voltage (V_{REF})	2.5	2.5	V	
Accuracy	±10	±10	mV Max	Of V_{REF} measured at the C_{REF} pin T_A = 25°C
Power Supply Rejection	65	67	dB typ	
Reference Temperature Coefficient	±15	±15	ppm/°C typ	
Internal V_{REF} Power-On Time	2	2	ms typ	
EXTERNAL REFERENCE INPUT[15]				
Voltage Range (V_{REF}) [4]	1	1	V min	
	V_{DD}	V_{DD}	V max	
Input Impedance	20	20	kΩ typ	
Input Leakage	1	1	µA max	Internal band gap deselected via ADCCON1.6
POWER SUPPLY MONITOR (PSM)				
DV_{DD} Trip Point Selection Range		2.93	V min	Two trip points selectable in this range programmed via TPD1–0 in PSMCON, 3 V part only
		3.08	V max	
DV_{DD} Power Supply Trip Point Accuracy		±2.5	% max	
WATCHDOG TIMER (WDT) [4]				
Timeout Period	0	0	ms min	Nine timeout periods selectable in this range
	2000	2000	ms max	
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS[16]				
Endurance[17]	100,000	100,000	Cycles min	
Data Retention[18]	100	100	Years min	
DIGITAL INPUTS				
Input Leakage Current (Port 0, $\overline{EA}$)	±10	±10	µA max	V_{IN} = 0 V or V_{DD}
	±1	±1	µA typ	V_{IN} = 0 V or V_{DD}
Logic 1 Input Current				
(All Digital Inputs), SDATA, SCLOCK	±10	±10	µA max	V_{IN} = V_{DD}
	±1	±1	µA typ	V_{IN} = V_{DD}
Logic 0 Input Current (Ports 1, 2, 3) SDATA, SCLOCK	–75	–25	µA max	
	–40	–15	µA typ	V_{IL} = 450 mV
Logic 1 to Logic 0 Transition Current (Ports 2 and 3)	–660	–250	µA max	V_{IL} = 2 V
	–400	–140	µA typ	V_{IL} = 2 V
RESET	±10	±10	µA max	V_{IN} = 0 V
	10	5	µA min	V_{IN} = 5 V, 3 V Internal Pull Down
	105	35	µA max	V_{IN} = 5 V, 3 V Internal Pull Down

[1] Temperature Range –40°C to +85°C.
[2] ADC linearity is guaranteed during normal MicroConverter core operation.
[3] ADC LSB size = $V_{REF}/2^{12}$, that is, for internal V_{REF} = 2.5 V, 1 LSB = 610 µV, and for external V_{REF} = 1 V, 1 LSB = 244 µV.
[4] These numbers are not production tested but are supported by design and/or characterization data on production release.
[5] Offset and gain error and offset and gain error match are measured after factory calibration.
[6] Based on external ADC system components, the user may need to execute a system calibration to remove additional external channel errors to achieve these specifications.
[7] SNR calculation includes distortion and noise components.
[8] Channel-to-channel crosstalk is measured on adjacent channels.
[9] The temperature monitor gives a measure of the die temperature directly; air temperature can be inferred from this result.
[10] DAC linearity is calculated using:
Reduced code range of 100 to 4095, 0 V to V_{REF} range.
Reduced code range of 100 to 3945, 0 V to V_{DD} range.
DAC output load = 10 kΩ and 100 pF.
[11] DAC differential nonlinearity specified on 0 V to V_{REF} and 0 V to V_{DD} ranges.
[12] DAC specification for output impedance in the unbuffered case depends on DAC code.
[13] DAC specifications for I_{SINK}, voltage output settling time, and digital-to-analog glitch energy depend on external buffer implementation in unbuffered mode. DAC in unbuffered mode tested with OP270 external buffer, which has a low input leakage current.
[14] Measured with C_{REF} pin decoupled with 0.47 µF capacitor to ground. Power-up time for the internal reference is determined by the value of the decoupling capacitor chosen for the C_{REF} pin.
[15] When using an external reference device, the internal band gap reference input can be bypassed by setting the ADCCON1.6 bit.
[16] Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and the Flash/EE data memory.
[17] Endurance is qualified to 100,000 cycles as per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, and +85°C. Typical endurance at 25°C is 700,000 cycles.
[18] Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22 method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature as shown in Figure 38 in the Flash/EE Memory Reliability section.
[19] Power supply current consumption is measured in normal, idle, and power-down modes under the following conditions:

Normal Mode:	Reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON (ADuC842/ADuC843), core executing internal software loop.
Idle Mode:	Reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON (ADuC842/ADuC843), PCON.0 = 1, core execution suspended in idle mode.
Power-Down Mode:	Reset = 0.4 V, all Port 0 pins = 0.4 V, All other digital I/O and Port 1 pins are open circuit, Core Clk changed via CD bits in PLLCON (ADuC842/ADuC843), PCON.0 = 1, core execution suspended in power-down mode, OSC turned on or off via OSC_PD bit (PLLCON.7) in PLLCON SFR (ADuC842/ADuC843).

[20] DV_{DD} power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.
[21] Power supply currents are production tested at 5.25 V and 3.3 V for a 5 V and 3 V part, respectively.

Pin No.	Mnemonic	Type[1]	Description
11	P1.4/ADC4		Input Port 1 (P1.4). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit.
			Single-Ended Analog Input 4 (ADC4). Channel selection is via ADCCON2 SFR.
12	P1.5/ADC5/$\overline{SS}$	I	Input Port 1 (P1.5). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit.
			Single-Ended Analog Input 5 (ADC5). Channel selection is via ADCCON2 SFR.
			Slave Select Input for the SPI Interface ($\overline{SS}$).
13	P1.6/ADC6	I	Input Port 1 (P1.6). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit.
			Single-Ended Analog Input 6 (ADC6). Channel selection is via ADCCON2 SFR.
14	P1.7/ADC7	I	Input Port 1(P1.7). Port 1 is an 8-bit input port only. Unlike the other ports, Port 1 defaults to analog input mode. To configure this port pin as a digital input, write a 0 to the port bit.
			Single-Ended Analog Input 7 (ADC7). Channel selection is via ADCCON2 SFR.
15	RESET	I	Reset. Digital Input. A high level on this pin for 24 master clock cycles while the oscillator is running resets the device.
16	P3.0/RxD	I/O	Input/Output Port 3 (P3.0). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.
			Receiver Data Input (Asynchronous) or Data Input/Output (Synchronous) of the Serial (UART) Port (RxD).
17	P3.1/TxD	I/O	Input/Output Port 3 (P3.1). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.
			Transmitter Data Output (Asynchronous) or Clock Output (Synchronous) of the Serial (UART) Port (TxD).
18	P3.2/$\overline{INT0}$	I/O	Input/Output Port 3 (P3.2). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.
			Interrupt 0 ($\overline{INT0}$). Programmable edge or level triggered interrupt input; can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 0.
19	P3.3/$\overline{INT1}$/MISO/PWM1	I/O	Input/Output Port 3 (P3.3). Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors.
			Interrupt 1 ($\overline{INT1}$). Programmable edge or level triggered interrupt input; can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 1.
			SPI Master Input/Slave Output Data I/O Pin for SPI Serial Interface (MISO).
			PWM 1 Voltage Output (PWM1). See the CFG841/CFG842 register for further information.
20, 34, 48	DV_{DD}	P	Digital Positive Supply Voltage. 3 V or 5 V nominal.
21, 35, 47	DGND	G	Digital Ground. DGND is the ground reference point for the digital circuitry.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity

The maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity

The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

The deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, that is, +½ LSB.

Gain Error

The deviation of the last code transition from the ideal AIN voltage (Full Scale – ½ LSB) after the offset error has been adjusted out.

Signal-to-(Noise + Distortion) Ratio

The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio depends on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)

The ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time

The amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse

The amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV-sec.

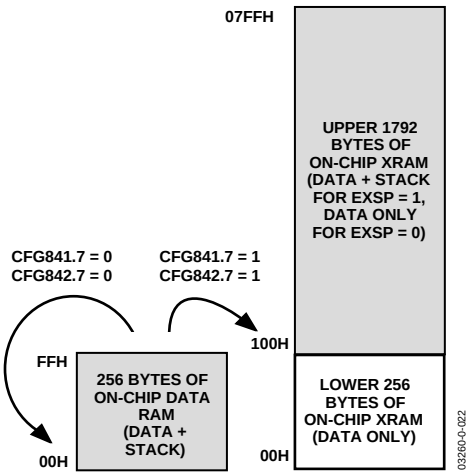

Figure 24. Extended Stack Pointer Operation

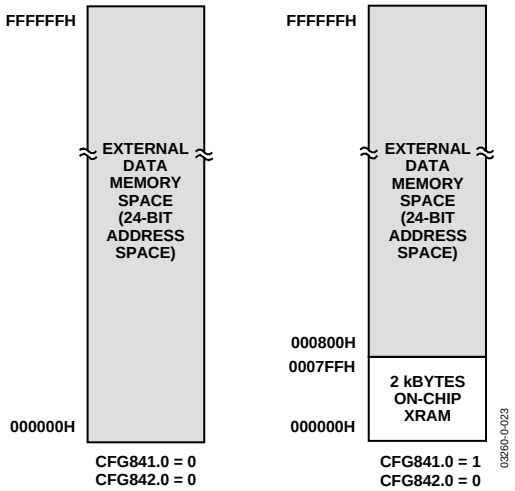

Figure 25. Internal and External XRAM

External Data Memory (External XRAM)

Just like a standard 8051 compatible core, the ADuC841/ADuC842/ADuC843 can access external data memory by using a MOVX instruction. The MOVX instruction automatically outputs the various control strobes required to access the data memory.

The parts, however, can access up to 16 MBytes of external data memory. This is an enhancement of the 64 kBytes of external data memory space available on a standard 8051 compatible core. The external data memory is discussed in more detail in the Hardware Design Considerations section.

Internal XRAM

The parts contain 2 kBytes of on-chip data memory. This memory, although on-chip, is also accessed via the MOVX instruction. The 2 kBytes of internal XRAM are mapped into the bottom 2 kBytes of the external address space if the CFG841/CFG842 bit is set. Otherwise, access to the external data memory occurs just like a standard 8051. When using the internal XRAM, Ports 0 and 2 are free to be used as general-purpose I/O.

SPECIAL FUNCTION REGISTERS (SFRS)

The SFR space is mapped into the upper 128 bytes of internal data memory space and is accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the parts via the SFR area is shown in Figure 26.

All registers, except the program counter (PC) and the four general-purpose register banks, reside in the SFR area. The SFR registers include control, configuration, and data registers, which provide an interface between the CPU and all on-chip peripherals.

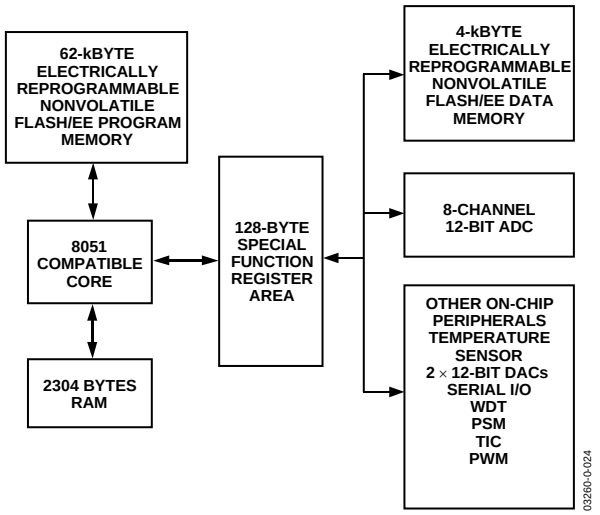

Figure 26. Programming Model

ADCCON1—(ADC Control SFR 1)

The ADCCON1 register controls conversion and acquisition times, hardware conversion modes, and power-down modes as detailed below.

SFR Address	EFH
SFR Power-On Default	40H
Bit Addressable	No

Table 8. ADCCON1 SFR Bit Designations

Bit No.	Name	Description
7	MD1	The mode bit selects the active operating mode of the ADC. Set by the user to power up the ADC. Cleared by the user to power down the ADC.
6	EXT_REF	Set by the user to select an external reference. Cleared by the user to use the internal reference.
5 4	CK1 CK0	The ADC clock divide bits (CK1, CK0) select the divide ratio for the PLL master clock (ADuC842/ADuC843) or the external crystal (ADuC841) used to generate the ADC clock. To ensure correct ADC operation, the divider ratio must be chosen to reduce the ADC clock to 8.38 MHz or lower. A typical ADC conversion requires 16 ADC clocks plus the selected acquisition time. The divider ratio is selected as follows: CK1 CK0 MCLK Divider 0 0 32 0 1 4 (Do not use with a CD setting of 0) 1 0 8 1 1 2
3 2	AQ1 AQ0	The ADC acquisition select bits (AQ1, AQ0) select the time provided for the input track-and-hold amplifier to acquire the input signal. An acquisition of three or more ADC clocks is recommended; clocks are as follows: AQ1 AQ0 No. ADC Clks 0 0 1 0 1 2 1 0 3 1 1 4
1	T2C	The Timer 2 conversion bit (T2C) is set by the user to enable the Timer 2 overflow bit to be used as the ADC conversion start trigger input.
0	EXC	The external trigger enable bit (EXC) is set by the user to allow the external Pin P3.5 ($\overline{\text{CONVST}}$) to be used as the active low convert start input. This input should be an active low pulse (minimum pulse width >100 ns) at the required sample rate.

The DMA logic operates from the ADC clock and uses pipelining to perform the ADC conversions and to access the external memory at the same time. The time it takes to perform one ADC conversion is called a DMA cycle. The actions performed by the logic during a typical DMA cycle are shown in Figure 36.

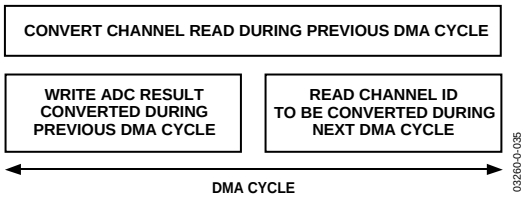

Figure 36. DMA Cycle

Figure 36 shows that during one DMA cycle, the following actions are performed by the DMA logic:

1. An ADC conversion is performed on the channel whose ID was read during the previous cycle.
2. The 12-bit result and the channel ID of the conversion performed in the previous cycle is written to the external memory.
3. The ID of the next channel to be converted is read from external memory.

For the previous example, the complete flow of events is shown in Figure 36. Because the DMA logic uses pipelining, it takes three cycles before the first correct result is written out.

Micro Operation during ADC DMA Mode

During ADC DMA mode, the MicroConverter core is free to continue code execution, including general housekeeping and communication tasks. However, note that MCU core accesses to Ports 0 and 2 (which of course are being used by the DMA controller) are gated off during the ADC DMA mode of operation. This means that even though the instruction that accesses the external Ports 0 or 2 appears to execute, no data is seen at these external ports as a result. Note that during DMA to the internally contained XRAM, Ports 0 and 2 are available for use.

The only case in which the MCU can access XRAM during DMA is when the internal XRAM is enabled and the section of RAM to which the DMA ADC results are being written to lies in an external XRAM. Then the MCU can access the internal XRAM only. This is also the case for use of the extended stack pointer.

The MicroConverter core can be configured with an interrupt to be triggered by the DMA controller when it has finished filling the requested block of RAM with ADC results, allowing the service routine for this interrupt to postprocess data without any real-time timing constraints.

ADC Offset and Gain Calibration Coefficients

The ADuC841/ADuC842/ADuC843 have two ADC calibration coefficients, one for offset calibration and one for gain calibration. Both the offset and gain calibration coefficients are 14-bit words, and are each stored in two registers located in the special function register (SFR) area. The offset calibration coefficient is divided into ADCOFSH (six bits) and ADCOFSL (8 bits), and the gain calibration coefficient is divided into ADCGAINH (6 bits) and ADCGAINL (8 bits).

The offset calibration coefficient compensates for dc offset errors in both the ADC and the input signal. Increasing the offset coefficient compensates for positive offset, and effectively pushes the ADC transfer function down. Decreasing the offset coefficient compensates for negative offset, and effectively pushes the ADC transfer function up. The maximum offset that can be compensated is typically ±5% of V_{REF}, which equates to typically ±125 mV with a 2.5 V reference.

Similarly, the gain calibration coefficient compensates for dc gain errors in both the ADC and the input signal. Increasing the gain coefficient compensates for a smaller analog input signal range and scales the ADC transfer function up, effectively increasing the slope of the transfer function. Decreasing the gain coefficient compensates for a larger analog input signal range and scales the ADC transfer function down, effectively decreasing the slope of the transfer function. The maximum analog input signal range for which the gain coefficient can compensate is $1.025 \times V_{REF}$, and the minimum input range is $0.975 \times V_{REF}$, which equates to typically ±2.5% of the reference voltage.

CALIBRATING THE ADC

Two hardware calibration modes are provided, which can be easily initiated by user software. The ADCCON3 SFR is used to calibrate the ADC. Bit 1 (typical) and CS3 to CS0 (ADCCON2) set up the calibration modes.

Device calibration can be initiated to compensate for significant changes in operating condition frequency, analog input range, reference voltage, and supply voltages. In this calibration mode, offset calibration uses internal AGND selected via ADCCON2 register Bits CS3 to CS0 (1011), and gain calibration uses internal V_{REF} selected by Bits CS3 to CS0 (1100). Offset calibration should be executed first, followed by gain calibration. System calibration can be initiated to compensate for both internal and external system errors. To perform system calibration by using an external reference, tie the system ground and reference to any two of the six selectable inputs. Enable external reference mode (ADCCON1.6). Select the channel connected to AGND via Bits CS3 to CS0 and perform system offset calibration. Select the channel connected to V_{REF} via Bits CS3 to CS0 and perform system gain calibration.

User Download Mode (ULOAD)

Figure 39 shows that it is possible to use the 62 kBytes of Flash/EE program memory available to the user as a single block of memory. In this mode, all of the Flash/EE memory is read-only to user code.

However, the Flash/EE program memory can also be written to during runtime simply by entering ULOAD mode. In ULOAD mode, the lower 56 kBytes of program memory can be erased and reprogrammed by user software as shown in Figure 39. ULOAD mode can be used to upgrade your code in the field via any user defined download protocol. By configuring the SPI port on the part as a slave, it is possible to completely reprogram the 56 kBytes of Flash/EE program memory in only 5 seconds (refer to Application Note uC007).

Alternatively, ULOAD mode can be used to save data to the 56 kBytes of Flash/EE memory. This can be extremely useful in data logging applications where the part can provide up to 60 kBytes of NV data memory on chip (4 kBytes of dedicated Flash/EE data memory also exist).

The upper 6 kBytes of the 62 kBytes of Flash/EE program memory are programmable only via serial download or parallel programming. This means that this space appears as read-only to user code. Therefore, it cannot be accidentally erased or reprogrammed by erroneous code execution, which makes it very suitable to use the 6 kBytes as a bootloader.

A bootload enable option exists in the serial downloader to "always run from E000H after reset." If using a bootloader, this option is recommended to ensure that the bootloader always executes correct code after reset. Programming the Flash/EE program memory via ULOAD mode is described in more detail in the description of ECON and in Application Note uC007.

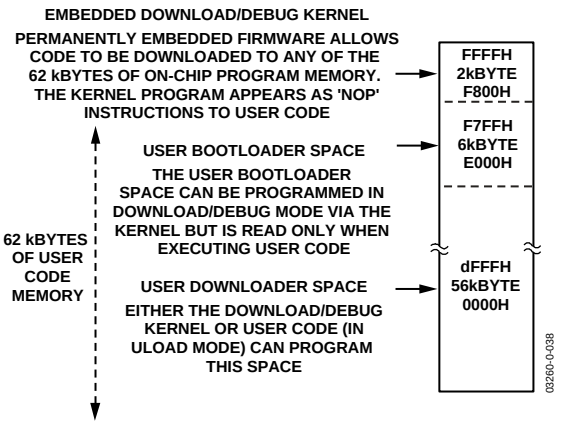

Figure 39. Flash/EE Program Memory Map in ULOAD Mode (62 kByte Part)

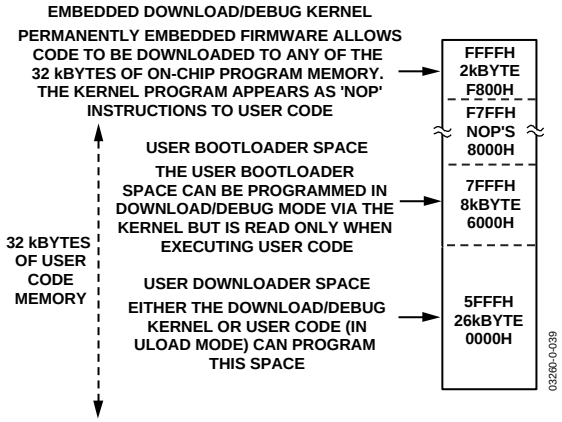

Figure 40. Flash/EE Program Memory Map in ULOAD Mode (32 kByte Part)

Flash/EE Program Memory Security

The ADuC841/ADuC842/ADuC843 facilitate three modes of Flash/EE program memory security. These modes can be independently activated, restricting access to the internal code space. These security modes can be enabled as part of serial download protocol as described in Application Note uC004 or via parallel programming. The security modes available on the parts are as follows:

Lock Mode

This mode locks the code memory, disabling parallel programming of the program memory. However, reading the memory in parallel mode and reading the memory via a MOVC command from external memory is still allowed. This mode is deactivated by initiating a code-erase command in serial download or parallel programming modes.

Secure Mode

This mode locks code in memory, disabling parallel programming (program and verify/read commands) as well as disabling the execution of a MOVC instruction from external memory, which is attempting to read the op codes from internal memory. Read/write of internal data Flash/EE from external memory is also disabled. This mode is deactivated by initiating a code-erase command in serial download or parallel programming modes.

Serial Safe Mode

This mode disables serial download capability on the device. If serial safe mode is activated and an attempt is made to reset the part into serial download mode, that is, $\overline{\text{RESET}}$ asserted and de-asserted with $\overline{\text{PSEN}}$ low, the part interprets the serial download reset as a normal reset only. It therefore cannot enter serial download mode but can only execute as a normal reset sequence. Serial safe mode can be disabled only by initiating a code-erase command in parallel programming mode.

CFG841	**ADuC841 Config SFR**
SFR Address	AFH
Power-On Default	10H[1]
Bit Addressable	No

Table 15. CFG841 SFR Bit Designations

Bit No.	Name	Description
7	EXSP	Extended SP Enable. When set to 1 by the user, the stack rolls over from SPH/SP = 00FFH to 0100H. When set to 0 by the user, the stack rolls over from SP = FFH to SP = 00H.
6	PWPO	PWM Pin Out Selection. Set to 1 by the user to select P3.4 and P3.3 as the PWM output pins. Set to 0 by the user to select P2.6 and P2.7 as the PWM output pins.
5	DBUF	DAC Output Buffer. Set to 1 by the user to bypass the DAC output buffer. Set to 0 by the user to enable the DAC output buffer.
4	EPM2	Flash/EE Controller and PWM Clock Frequency Configuration Bits. Frequency should be configured such that F_{OSC}/Divide Factor = 32 kHz + 50%.
3	EPM1	EPM2 EPM1 EPM0 Divide Factor
2	EPM0	0 0 0 32 0 0 1 64 0 1 0 128 0 1 1 256 1 0 0 512 1 0 1 1024
1	MSPI	Set to 1 by the user to move the SPI functionality of MISO, MOSI, and SCLOCK to P3.3, P3.4, and P3.5, respectively. Set to 0 by the user to leave the SPI functionality as usual on MISO, MOSI, and SCLOCK pins.
0	XRAMEN	XRAM Enable Bit. When set to 1 by the user, the internal XRAM is mapped into the lower two kBytes of the external address space. When set to 0 by the user, the internal XRAM is not accessible, and the external data memory is mapped into the lower two kBytes of external data memory.

[1] Note that the Flash/EE controller bits EPM2, EPM1, EPM0 are set to their correct values depending on the crystal frequency at power-up. The user should not modify these bits so all instructions to the CFG841 register should use the ORL, XRL, or ANL instructions. Value of 10H is for 11.0592 MHz crystal.

USER INTERFACE TO ON-CHIP PERIPHERALS

This section gives a brief overview of the various peripherals also available on-chip. A summary of the SFRs used to control and configure these peripherals is also given.

DAC

The ADuC841/ADuC842 incorporate two 12-bit voltage output DACs on-chip. Each has a rail-to-rail voltage output buffer capable of driving 10 kΩ/100 pF. Each has two selectable ranges, 0 V to V_{REF} (the internal band gap 2.5 V reference) and 0 V to AV_{DD}. Each can operate in 12-bit or 8-bit mode.

Both DACs share a control register, DACCON, and four data registers, DAC1H/L, DAC0/L. Note that in 12-bit asynchronous mode, the DAC voltage output is updated as soon as the DACL data SFR has been written; therefore, the DAC data registers should be updated as DACH first, followed by DACL. Note that for correct DAC operation on the 0 V to V_{REF} range, the ADC must be switched on. This results in the DAC using the correct reference value.

DACCON	**DAC Control Register**
SFR Address	FDH
Power-On Default	04H
Bit Addressable	No

Table 16. DACCON SFR Bit Designations

Bit No.	Name	Description
7	MODE	The DAC MODE bit sets the overriding operating mode for both DACs. Set to 1 by the user to select 8-bit mode (write 8 bits to DACxL SFR). Set to 0 by the user to select 12-bit mode.
6	RNG1	DAC1 Range Select Bit. Set to 1 by the user to select the range for DAC1 as 0 V to V_{DD}. Set to 0 by the user to select the range for DAC1 as 0 V to V_{REF}.
5	RNG0	DAC0 Range Select Bit. Set to 1 by the user to select the range for DAC0 as 0 V to V_{DD}. Set to 0 by the user to select the range for DAC0 as 0 V to V_{REF}.
4	CLR1	DAC1 Clear Bit. Set to 1 by the user to leave the output of DAC1 at its normal level. Set to 0 by the user to force the output of DAC1 to 0 V.
3	CLR0	DAC0 Clear Bit. Set to 1 by the user to leave the output of DAC0 at its normal level. Set to 0 by the user to force the output of DAC0 to 0 V.
2	SYNC	DAC0/1 Update Synchronization Bit. When set to 1, the DAC outputs update as soon as DACxL SFRs are written. The user can simultaneously update both DACs by first updating the DACxL/H SFRs while SYNC is 0. Both DACs then update simultaneously when the SYNC bit is set to 1.
1	PD1	DAC1 Power-Down Bit. Set to 1 by the user to power on DAC1. Set to 0 by the user to power off DAC1.
0	PD0	DAC0 Power-Down Bit. Set to 1 by the user to power on DAC0. Set to 0 by the user to power off DAC0.

DACxH/L	**DAC Data Registers**	
Function	DAC data registers, written by the user to update the DAC output.	
SFR Address	DAC0L (DAC0 Data Low Byte) -> F9H; DAC1L (DAC1 Data Low Byte) -> FBH	
	DACH (DAC0 Data High Byte) -> FAH; DAC1H (DAC1 Data High Byte) -> FCH	
Power-On Default	00H	All Four Registers.
Bit Addressable	No	All Four Registers.

The 12-bit DAC data should be written into DACxH/L right-justified such that DACxL contains the lower 8 bits, and the lower nibble of DACxH contains the upper 4 bits.

PULSE-WIDTH MODULATOR (PWM)

The PWM on the ADuC841/ADuC842/ADuC843 is a highly flexible PWM offering programmable resolution and an input clock, and can be configured for any one of six different modes of operation. Two of these modes allow the PWM to be configured as a Σ-Δ DAC with up to 16 bits of resolution. A block diagram of the PWM is shown in Figure 47. Note the PWM clock's sources are different for the ADuC841, and are given in Table 18.

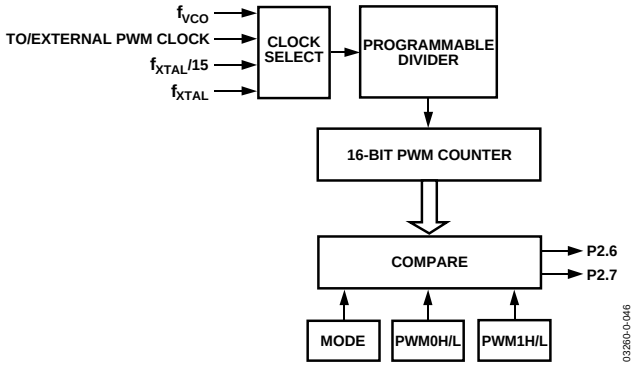

Figure 47. PWM Block Diagram

The PWM uses five SFRs: the control SFR (PWMCON) and four data SFRs (PWM0H, PWM0L, PWM1H, and PWM1L).

PWMCON, as described in the following sections, controls the different modes of operation of the PWM as well as the PWM clock frequency.

PWM0H/L and PWM1H/L are the data registers that determine the duty cycles of the PWM outputs. The output pins that the PWM uses are determined by the CFG841/CFG842 register, and can be either P2.6 and P2.7 or P3.4 and P3.3. In this section of the data sheet, it is assumed that P2.6 and P2.7 are selected as the PWM outputs.

To use the PWM user software, first write to PWMCON to select the PWM mode of operation and the PWM input clock. Writing to PWMCON also resets the PWM counter. In any of the 16-bit modes of operation (Modes 1, 3, 4, 6), user software should write to the PWM0L or PWM1L SFRs first. This value is written to a hidden SFR. Writing to the PWM0H or PWM1H SFRs updates both the PWMxH and the PWMxL SFRs but does not change the outputs until the end of the PWM cycle in progress. The values written to these 16-bit registers are then used in the next PWM cycle.

PWMCON PWM	**Control SFR**
SFR Address	AEH
Power-On Default	00H
Bit Addressable	No

Table 18. PWMCON SFR Bit Designations

Bit No.	Name	Description			
7	SNGL	Turns off PMW output at P2.6 or P3.4, leaving the port pin free for digital I/O.			
6	MD2	PWM Mode Bits.			
5	MD1	The MD2/1/0 bits choose the PWM mode as follows:			
4	MD0	MD2	MD1	MD0	Mode
		0	0	0	Mode 0: PWM Disabled
		0	0	1	Mode 1: Single variable resolution PWM on P2.7 or P3.3
		0	1	0	Mode 2: Twin 8-bit PWM
		0	1	1	Mode 3: Twin 16-bit PWM
		1	0	0	Mode 4: Dual NRZ 16-bit ∑-Δ DAC
		1	0	1	Mode 5: Dual 8-bit PWM
		1	1	0	Mode 6: Dual RZ 16-bit ∑-Δ DAC
		1	1	1	Reserved
3	CDIV1	PWM Clock Divider.			
2	CDIV0	Scale the clock source for the PWM counter as follows:			
		CDIV1	CDIV0	Description	
		0	0	PWM Counter = Selected Clock/1	
		0	1	PWM Counter = Selected Clock/4	
		1	0	PWM Counter = Selected Clock/16	
		1	1	PWM Counter = Selected Clock/64	
1	CSEL1	PWM Clock Divider.			
0	CSEL0	Select the clock source for the PWM as follows:			
		CSEL1	CSEL0	Description	
		0	0	PWM Clock = f_{XTAL}/15, ADuC841 = f_{OCS}/DIVIDE FACTOR /15 (see the CFG841 register)	
		0	1	PWM Clock = f_{XTAL}, ADuC841 = f_{OCS}/DIVIDE FACTOR (see the CFG841 register)	
		1	0	PWM Clock = External input at P3.4/T0	
		1	1	PWM Clock = f_{VCO} = 16.777216 MHz, ADuC841 = f_{OSC}	

SERIAL PERIPHERAL INTERFACE (SPI)

The ADuC841/ADuC842/ADuC843 integrate a complete hardware serial peripheral interface on-chip. SPI is an industry-standard synchronous serial interface that allows 8 bits of data to be synchronously transmitted and received simultaneously, that is, full duplex. Note that the SPI pins are shared with the I^2C pins. Therefore, the user can enable only one interface or the other on these pins at any given time (see SPE in Table 19). SPI can be operated at the same time as the I^2C interface if the MSPI bit in CFG841/CFG8842 is set. This moves the SPI outputs (MISO, MOSI, and SCLOCK) to P3.3, P3.4, and P3.5, respectively). The SPI port can be configured for master or slave operation and typically consists of four pins, described in the following sections.

MISO (Master In, Slave Out Data I/O Pin)

The MISO pin is configured as an input line in master mode and as an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte-wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin)

The MOSI pin is configured as an output line in master mode and as an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte-wide (8-bit) serial data, MSB first.

SCLOCK (Serial Clock I/O Pin)

The master serial clock (SCLOCK) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines. A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode. In master mode, the bit rate, polarity, and phase of the clock are controlled by the CPOL, CPHA, SPR0, and SPR1 bits in the SPICON SFR (see Table 19). In slave mode, the SPICON register must be configured with the phase and polarity (CPHA and CPOL) of the expected input clock. In both master and slave modes, the data is transmitted on one edge of the SCLOCK signal and sampled on the other. It is important, therefore, that CPHA and CPOL are configured the same for the master and slave devices.

$\overline{SS}$ (Slave Select Input Pin)

The $\overline{SS}$ pin is shared with the ADC5 input. To configure this pin as a digital input, the bit must be cleared, for example, CLR P1.5. This line is active low. Data is received or transmitted in slave mode only when the $\overline{SS}$ pin is low, allowing the parts to be used in single-master, multislave SPI configurations. If CPHA = 1, the $\overline{SS}$ input may be permanently pulled low. If CPHA = 0, the $\overline{SS}$ input must be driven low before the first bit in a byte-wide transmission or reception and return high again after the last bit in that byte-wide transmission or reception. In SPI slave mode, the logic level on the external $\overline{SS}$ pin can be read via the SPR0 bit in the SPICON SFR. The SFR registers, described in the following tables, are used to control the SPI interface.

I²C COMPATIBLE INTERFACE

The ADuC841/ADuC842/ADuC843 support a fully licensed I²C serial interface. The I²C interface is implemented as a full hardware slave and software master. SDATA is the data I/O pin, and SCLOCK is the serial clock. These two pins are shared with the MOSI and SCLOCK pins of the on-chip SPI interface. To enable the I²C interface, the SPI interface must be turned off (see SPE in Table 19) or the SPI interface must be moved to P3.3, P3.4, and P3.5 via the CFG841.1/CFG842.1 bit. Application Note uC001 describes the operation of this interface as implemented and is available from the MicroConverter website at www.analog.com/microconverter.

Three SFRs are used to control the I²C interface and are described in the following tables.

I2CCON	I²C Control Register
SFR Address	E8H
Power-On Default	00H
Bit Addressable	Yes

Table 20. I2CCON SFR Bit Designations, Master Mode

Bit No.	Name	Description
7	MDO	I²C Software Master Data Output Bit (Master Mode Only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit is output on the SDATA pin if the data output enable (MDE) bit is set.
6	MDE	I²C Software Master Data Output Enable Bit (Master Mode Only). Set by the user to enable the SDATA pin as an output (Tx). Cleared by the user to enable the SDATA pin as an input (Rx).
5	MCO	I²C Software Master Clock Output Bit (Master Mode Only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit is output on the SCLOCK pin.
4	MDI	I²C Software Master Data Input Bit (Master Mode Only). This data bit is used to implement a master I²C receiver interface in software. Data on the SDATA pin is latched into this bit on SCLOCK if the data output enable (MDE) bit is 0.
3	I2CM	I²C Master/Slave Mode Bit. Set by the user to enable I²C software master mode. Cleared by the user to enable I²C hardware slave mode.
2	----	Reserved.
1	----	Reserved.
0	----	Reserved.

Table 21. I2CCON SFR Bit Designations, Slave Mode

Bit No.	Name	Description
7	I2CSI	I²C Stop Interrupt Enable Bit. Set by the user to enable I²C stop interrupts. If set, a stop bit that follows a valid start condition generates an interrupt. Cleared by the user to disable I²C stop interrupts.
6	I2CGC	I²C General Call Status Bit. Set by hardware after receiving a general call address. Cleared by the user.
5	I2CID1	I²C Interrupt Decode Bits.
4	I2CID0	Set by hardware to indicate the source of an I²C interrupt. 00 Start and Matching Address. 01 Repeated Start and Matching Address. 10 User Data. 11 Stop after a Start and Matching Address.
3	I2CM	I²C Master/Slave Mode Bit. Set by the user to enable I²C software master mode. Cleared by the user to enable I²C hardware slave mode.

- An I²C slave can respond to repeated start conditions without a stop bit in between. This allows a master to change direction of transfer without giving up the bus. Note that the repeated start is detected only when a slave has previously been configured as a receiver.
- On-chip filtering rejects <50 ns spikes on the SDATA and the SCLOCK lines to preserve data integrity.

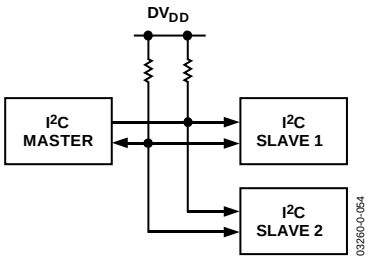

Figure 55. Typical I²C System

Software Master Mode

The ADuC841/ADuC842/ADuC843 can be used as I²C master devices by configuring the I²C peripheral in master mode and writing software to output the data bit by bit. This is referred to as a software master. Master mode is enabled by setting the I2CM bit in the I2CCON register.

To transmit data on the SDATA line, MDE must be set to enable the output driver on the SDATA pin. If MDE is set, the SDATA pin is pulled high or low depending on whether the MDO bit is set or cleared. MCO controls the SCLOCK pin and is always configured as an output in master mode. In master mode, the SCLOCK pin is pulled high or low depending on the whether MCO is set or cleared.

To receive data, MDE must be cleared to disable the output driver on SDATA. Software must provide the clocks by toggling the MCO bit and reading the SDATA pin via the MDI bit. If MDE is cleared, MDI can be used to read the SDATA pin. The value of the SDATA pin is latched into MDI on a rising edge of SCLOCK. MDI is set if the SDATA pin was high on the last rising edge of SCLOCK. MDI is clear if the SDATA pin was low on the last rising edge of SCLOCK.

Software must control MDO, MCO, and MDE appropriately to generate the start condition, slave address, acknowledge bits, data bytes, and stop conditions. These functions are described in Application Note uC001.

Hardware Slave Mode

After reset, the ADuC841/ADuC842/ADuC843 default to hardware slave mode. The I²C interface is enabled by clearing the SPE bit in SPICON (this is not necessary if the MSPI bit is set). Slave mode is enabled by clearing the I2CM bit in I2CCON. The parts have a full hardware slave. In slave mode, the I²C address is stored in the I2CADD register. Data received or to be transmitted is stored in the I2CDAT register.

Once enabled in I²C slave mode, the slave controller waits for a start condition. If the part detects a valid start condition, followed by a valid address, followed by the R/$\overline{W}$ bit, the I2CI interrupt bit is automatically set by hardware. The I²C peripheral generates a core interrupt only if the user has pre-configured the I²C interrupt enable bit in the IEIP2 SFR as well as the global interrupt bit, $\overline{EA}$, in the IE SFR. That is,

```
;Enabling I2C Interrupts for the ADuC842
MOV IEIP2,#01h            ; enable I2C interrupt
SETB EA
```

An autoclear of the I2CI bit is implemented on the parts so that this bit is cleared automatically on a read or write access to the I2CDAT SFR.

```
MOV I2CDAT, A             ; I2CI auto-cleared
MOV A, I2CDAT             ; I2CI auto-cleared
```

If for any reason the user tries to clear the interrupt more than once, that is, access the data SFR more than once per interrupt, then the I²C controller halts. The interface then must be reset using the I2CRS bit.

The user can choose to poll the I2CI bit or to enable the interrupt. In the case of the interrupt, the PC counter vectors to 003BH at the end of each complete byte. For the first byte, when the user gets to the I2CI ISR, the 7-bit address and the R/$\overline{W}$ bit appear in the I2CDAT SFR.

The I2CTX bit contains the R/$\overline{W}$ bit sent from the master. If I2CTX is set, the master is ready to receive a byte. Therefore the slave transmits data by writing to the I2CDAT register. If I2CTX is cleared, the master is ready to transmit a byte. Therefore the slave receives a serial byte. Software can interrogate the state of I2CTX to determine whether it must write to or read from I2CDAT.

Once the part has received a valid address, hardware holds SCLOCK low until the I2CI bit is cleared by software. This allows the master to wait for the slave to be ready before transmitting the clocks for the next byte.

The I2CI interrupt bit is set every time a complete data byte is received or transmitted, provided it is followed by a valid ACK. If the byte is followed by a NACK, an interrupt is not generated.

The part continues to issue interrupts for each complete data byte transferred until a stop condition is received or the interface is reset.

When a stop condition is received, the interface resets to a state in which it is waiting to be addressed (idle). Similarly, if the interface receives a NACK at the end of a sequence, it also returns to the default idle state. The I2CRS bit can be used to reset the I²C interface. This bit can be used to force the interface back to the default idle state.

TIMECON	**TIC Control Register**
SFR Address	A1H
Power-On Default	00H
Bit Addressable	No

Table 25. TIMECON SFR Bit Designations

Bit No.	Name	Description
7	----	Reserved.
6	TFH	Twenty-Four Hour Select Bit. Set by the user to enable the hour counter to count from 0 to 23. Cleared by the user to enable the hour counter to count from 0 to 255.
5	ITS1	Interval Timebase Selection Bits.
4	ITS0	Written by user to determine the interval counter update rate. ITS1 ITS0 Interval Timebase 0 0 1/128 Second 0 1 Seconds 1 0 Minutes 1 1 Hours
3	STI	Single Time Interval Bit. Set by the user to generate a single interval timeout. If set, a timeout clears the TIEN bit. Cleared by the user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.
2	TII	TIC Interrupt Bit. Set when the 8-bit interval counter matches the value in the INTVAL SFR. Cleared by user software.
1	TIEN	Time Interval Enable Bit. Set by the user to enable the 8-bit time interval counter. Cleared by the user to disable the interval counter.
0	TCEN	Time Clock Enable Bit. Set by the user to enable the time clock to the time interval counters. Cleared by the user to disable the clock to the time interval counters and reset the time interval SFRs to the last value written to them by the user. The time registers (HTHSEC, SEC, MIN, and HOUR) can be written while TCEN is low.

INTVAL	**User Time Interval Select Register**
Function	User code writes the required time interval to this register. When the 8-bit interval counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled.
SFR Address	A6H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 255 decimal

HTHSEC	**Hundredths Seconds Time Register**
Function	This register is incremented in 1/128 second intervals once TCEN in TIMECON is active. The HTHSEC SFR counts from 0 to 127 before rolling over to increment the SEC time register.
SFR Address	A2H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 127 decimal

SEC	**Seconds Time Register**
Function	This register is incremented in 1-second intervals once TCEN in TIMECON is active. The SEC SFR counts from 0 to 59 before rolling over to increment the MIN time register.
SFR Address	A3H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 59 decimal

MIN	**Minutes Time Register**
Function	This register is incremented in 1-minute intervals once TCEN in TIMECON is active. The MIN SFR counts from 0 to 59 before rolling over to increment the HOUR time register.
SFR Address	A4H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 59 decimal

HOUR	**Hours Time Register**
Function	This register is incremented in 1-hour intervals once TCEN in TIMECON is active. The HOUR SFR counts from 0 to 23 before rolling over to 0.
SFR Address	A5H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 23 decimal

If access to more than 64 kBytes of RAM is desired, a feature unique to the ADuC841/ADuC842/ADuC843 allows addressing up to 16 MBytes of external RAM simply by adding an additional latch as illustrated in Figure 79.

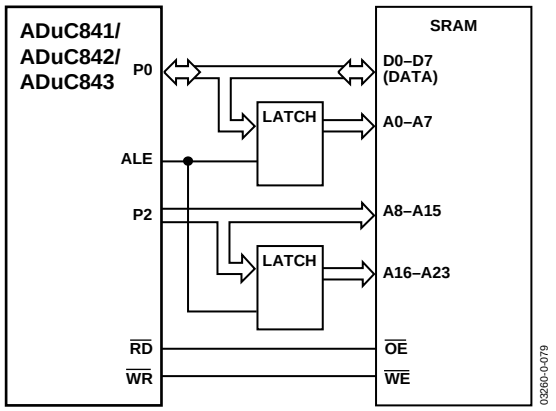

Figure 79. External Data Memory Interface (16 MBytes Address Space)

In either implementation, Port 0 (P0) serves as a multiplexed address/data bus. It emits the low byte of the data pointer (DPL) as an address, which is latched by a pulse of ALE prior to data being placed on the bus by the ADuC841/ADuC842/ADuC843 (write operation) or by the SRAM (read operation). Port 2 (P2) provides the data pointer page byte (DPP) to be latched by ALE, followed by the data pointer high byte (DPH). If no latch is connected to P2, DPP is ignored by the SRAM, and the 8051 standard of 64 kBytes external data memory access is maintained.

Power Supplies

The operational power supply voltage of the parts depends on whether the part is the 3 V version or the 5 V version. The specifications are given for power supplies within 2.7 V to 3.6 V or ±5% of the nominal 5 V level.

Note that Figure 80 and Figure 81 refer to the PQFP package. For the CSP package, connect the extra DV_{DD}, DGND, AV_{DD}, and AGND in the same manner. Also, the paddle on the bottom of the package should be soldered to a metal plate to provide mechanical stability. This metal plate should not be connected to ground.

Separate analog and digital power supply pins (AV_{DD} and DV_{DD}, respectively) allow AV_{DD} to be kept relatively free of the noisy digital signals that are often present on the system DV_{DD} line. However, though you can power AV_{DD} and DV_{DD} from two separate supplies if desired, you must ensure that they remain within ±0.3 V of one another at all times to avoid damaging the chip (as per the Absolute Maximum Ratings section). Therefore, it is recommended that unless AV_{DD} and DV_{DD} are connected directly together, back-to-back Schottky diodes should be connected between them, as shown in Figure 80.

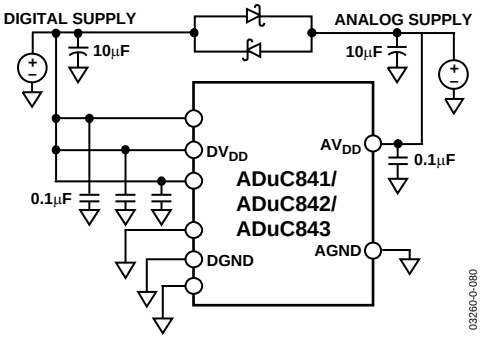

Figure 80. External Dual-Supply Connections

As an alternative to providing two separate power supplies, the user can help keep AV_{DD} quiet by placing a small series resistor and/or ferrite bead between it and DV_{DD}, and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 81. With this configuration, other analog circuitry (such as op amps and voltage reference) can be powered from the AV_{DD} supply line as well. The user still needs to include back-to-back Schottky diodes between AV_{DD} and DV_{DD} to protect them from power-up and power-down transient conditions that could momentarily separate the two supply voltages.

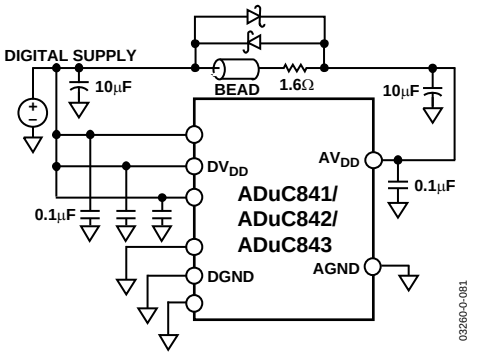

Figure 81. External Single-Supply Connections

Notice that in both Figure 80 and Figure 81, a large value (10 µF) reservoir capacitor sits on DV_{DD} and a separate 10 µF capacitor sits on AV_{DD}. Also, local small-value (0.1 µF) capacitors are located at each V_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors, and ensure the smaller capacitors are close to each AV_{DD} pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, note that at all times, the analog and digital ground pins on the part must be referenced to the same system ground reference point.

5 V Part

For DV_{DD} below 4.5 V, the internal POR holds the part in reset. As DV_{DD} rises above 4.5 V, an internal timer times out for approximately 128 ms before the part is released from reset. The user must ensure that the power supply has reached a stable 4.75 V minimum level by this time. Likewise on power-down, the internal POR holds the part in reset until the power supply has dropped below 1 V. Figure 83 illustrates the operation of the internal POR in detail.

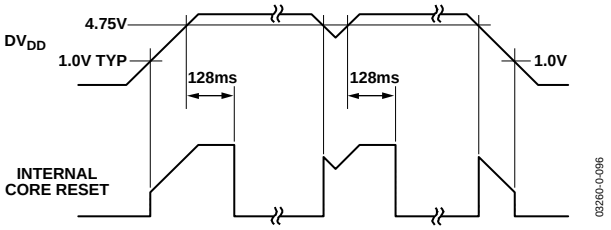

Figure 83. Internal POR Operation

Grounding and Board Layout Recommendations

As with all high resolution data converters, special attention must be paid to grounding and PC board layout of ADuC841/ADuC842/ADuC843 based designs to achieve optimum performance from the ADC and the DACs. Although the parts have separate pins for analog and digital ground (AGND and DGND), the user must not tie these to two separate ground planes unless the two ground planes are connected together very close to the part, as illustrated in the simplified example of Figure 84a. In systems where digital and analog ground planes are connected together somewhere else (for example, at the system's power supply), they cannot be connected again near the part since a ground loop would result. In these cases, tie all the part's AGND and DGND pins to the analog ground plane, as illustrated in Figure 84b. In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board such that digital return currents do not flow near analog circuitry and vice versa. The part can then be placed between the digital and analog sections, as illustrated in Figure 84c.

In all of these scenarios, and in more complicated real-life applications, keep in mind the flow of current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths that the currents took to reach their destinations. For example, do not power components on the analog side of Figure 84b with DV_{DD} since that would force return currents from DV_{DD} to flow through AGND. Also, try to avoid digital currents flowing under analog circuitry, which could happen if the user places a noisy digital chip on the left half of the board in Figure 84c. Whenever possible, avoid large discontinuities in the ground plane(s) (like those formed by a long trace on the same layer), since they force return signals to travel a longer path. And of course, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the part's digital inputs, a series resistor should be added to each relevant line to keep rise and fall times longer than 5 ns at the part's input pins. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the part and from affecting the accuracy of ADC conversions.

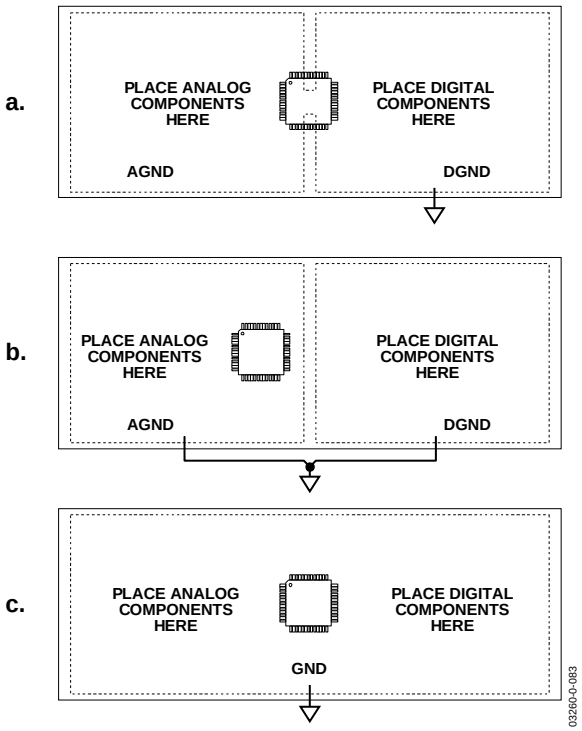

Figure 84. System Grounding Schemes

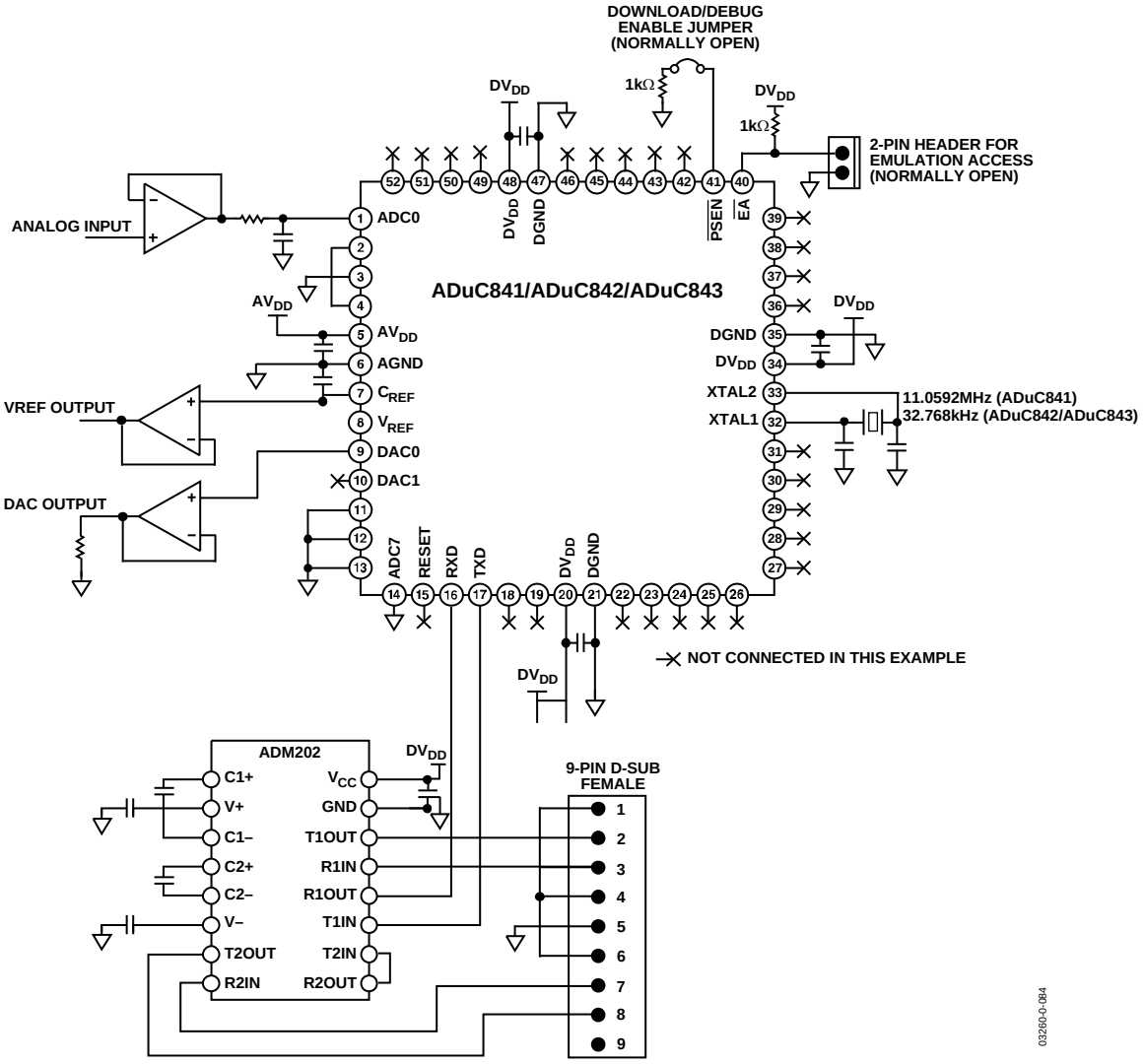

Figure 85. Example System (PQFP Package), DACs Not Present on ADuC843

OTHER HARDWARE CONSIDERATIONS

To facilitate in-circuit programming, plus in-circuit debug and emulation options, users need to implement some simple connection points in their hardware to allow easy access to download, debug, and emulation modes.

In-Circuit Serial Download Access

Nearly all ADuC841/ADuC842/ADuC843 designs want to take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the ADuC841/ADuC842/ADuC843's UART, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is illustrated in Figure 85 with a simple ADM202 based circuit. If users would rather not design an RS-232 chip onto a board, refer to Application Note uC006, *A 4-Wire UART-to-PC Interface*, (at www.analog.com/microconverter) for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the part.

In addition to the basic UART connections, users also need a way to trigger the chip into download mode. This is accomplished via a 1 kΩ pull-down resistor that can be jumpered onto the $\overline{\text{PSEN}}$ pin, as shown in Figure 85. To get the part into download mode, simply connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available), and it is then ready to serially receive a new program. With the jumper removed, the device comes up in normal mode (and runs the program) whenever power is cycled or RESET is toggled.

ORDERING GUIDE

Model[1]	Supply Voltage V_{DD}	User Program Code Space	Temperature Range	Package Description	Package Option
ADuC841BSZ62-5	5	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC841BSZ62-3	3	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC841BCPZ62-5	5	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC841BCPZ62-3	3	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC841BCPZ8-5	5	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC841BCPZ8-3	3	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BSZ62-5	5	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC842BSZ62-3	3	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC842BCPZ62-5	5	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BCPZ62-3	3	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BCPZ32-5	5	32	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BCPZ32-3	3	32	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BCPZ8-5	5	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC842BCPZ8-3	3	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADUC843BSZ62-5	5	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC843BSZ62-3	3	62	–40°C to +85°C	52-Lead Plastic Quad Flat Package [MQFP]	S-52-2
ADuC843BCP62Z-5	5	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC843BCPZ62-3	3	62	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC843BCP32Z-5	5	32	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC843BCPZ32-3	3	32	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC843BCPZ8-5	5	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
ADuC843BCPZ8-3	3	8	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-11
EVAL-ADuC841QSZ	5			QuickStart Development System for the ADuC841	
EVAL-ADuC841QSPZ	5			QuickStart Plus Development System	
EVAL-ADuC842QSZ	5			QuickStart Development System for the ADuC842 and ADuC843	
EVAL-ADuC842QSPZ	5			QuickStart Plus Development System	
USB-EA-CONVZ				USB to EA Emulator	

[1] The only difference between the ADuC842 and ADuC843devices is the voltage output DACs on the ADuC842; thus, the evaluation system for the ADuC842 is also suitable for the ADuC843.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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