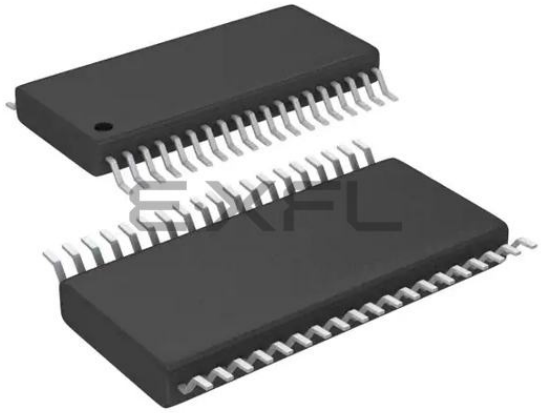

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	86MHz
Connectivity	SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	19
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc866-2fri-bc

XC866

8-Bit Single-Chip Microcontroller

Microcontrollers

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3.2 Memory Organization

The XC866 CPU operates in the following five address spaces:

- 8 Kbytes of Boot ROM program memory
- 256 bytes of internal RAM data memory
- 512 bytes of XRAM memory
  (XRAM can be read/written as program memory or external data memory)
- a 128-byte Special Function Register area
- 4/8/16 Kbytes of Flash program memory (Flash devices); or
  8/16 Kbytes of ROM program memory, with additional 4 Kbytes of Flash
  (ROM devices)

Figure 6 illustrates the memory address spaces of the XC866-4FR device.

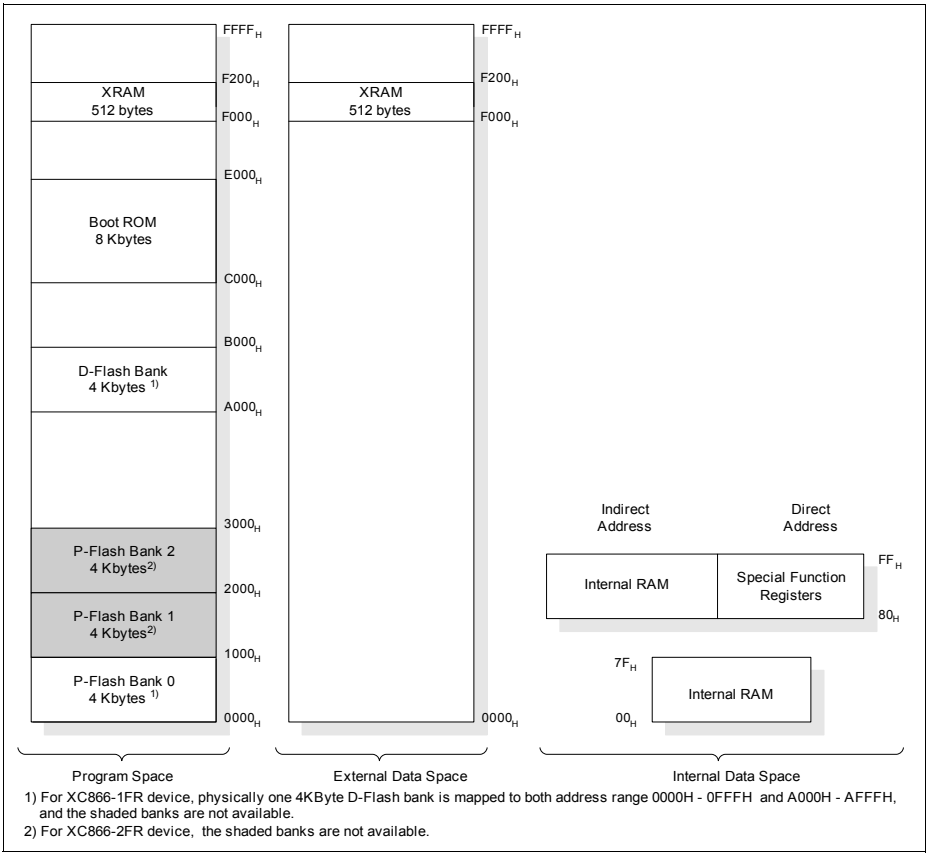


Figure 6 Memory Map of XC866 Flash Devices

Table 5 Flash Protection Type for XC866-2FR and XC866-4FR devices

PASSWORD	Type of Protection	Flash Banks to Erase when Unprotected
$1XXXXXXX_B$	Flash Protection Mode 1	All Banks
$0XXXXXXX_B$	Flash Protection Mode 0	P-Flash Bank

For XC866-1FR device and ROM devices:

The selection of protection type is summarized in **Table 6**.

Table 6 Flash Protection Type for XC866-1FR device and ROM devices

PASSWORD	Type of Protection (Applicable to the whole Flash)	Sectors to Erase when Unprotected	Comments
$1XXXXXXX_B$	Read/Program/Erase	All Sectors	Compatible to Protection mode 1
$00001XXX_B$	Erase	Sector 0	
$00010XXX_B$	Erase	Sector 0 and 1	
$00011XXX_B$	Erase	Sector 0 to 2	
$00100XXX_B$	Erase	Sector 0 to 3	
$00101XXX_B$	Erase	Sector 0 to 4	
$00110XXX_B$	Erase	Sector 0 to 5	
$00111XXX_B$	Erase	Sector 0 to 6	
$01000XXX_B$	Erase	Sector 0 to 7	
$01001XXX_B$	Erase	Sector 0 to 8	
$01010XXX_B$	Erase	All Sectors	
Others	Erase	None	

Although no protection scheme can be considered infallible, the XC866 memory protection strategy provides a very high level of protection for a general purpose microcontroller.

Note: The RMAP bit must be cleared/set by ANL or ORL instructions. The rest bits of SYSCON0 should not be modified.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

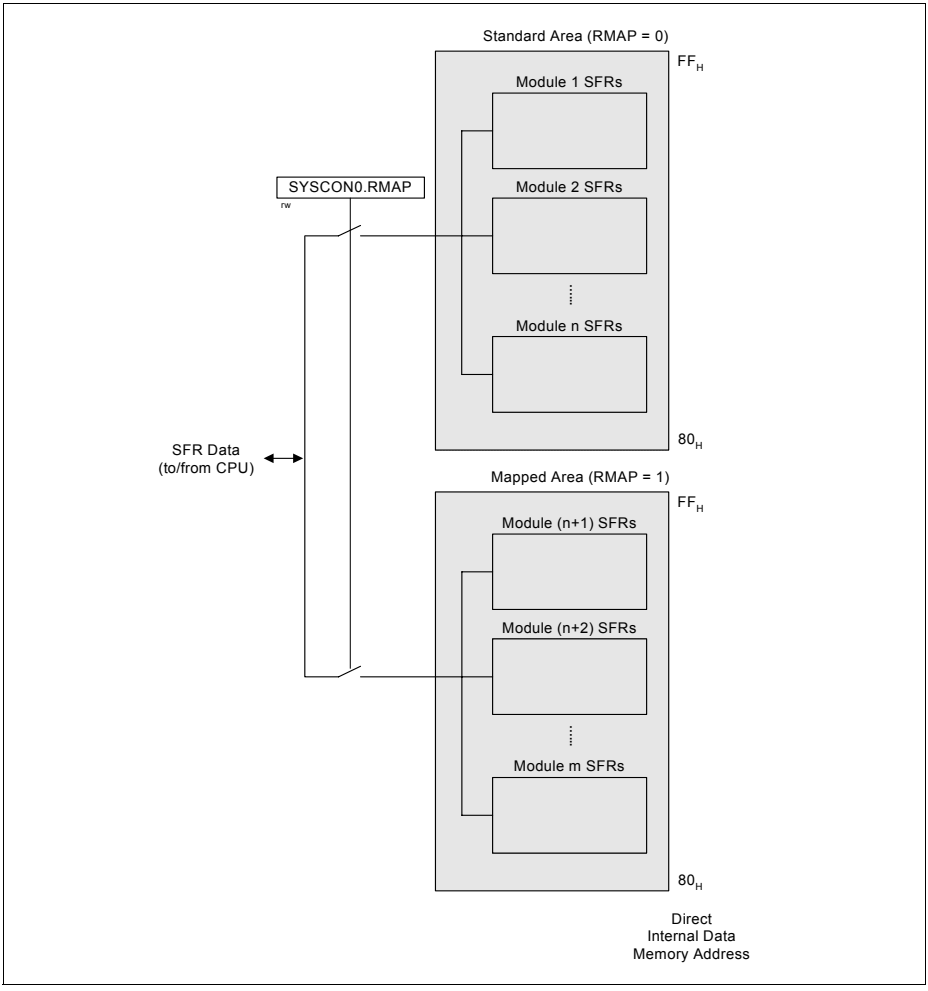


Figure 8 Address Extension by Mapping

3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the XC866 has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in **Figure 9**.

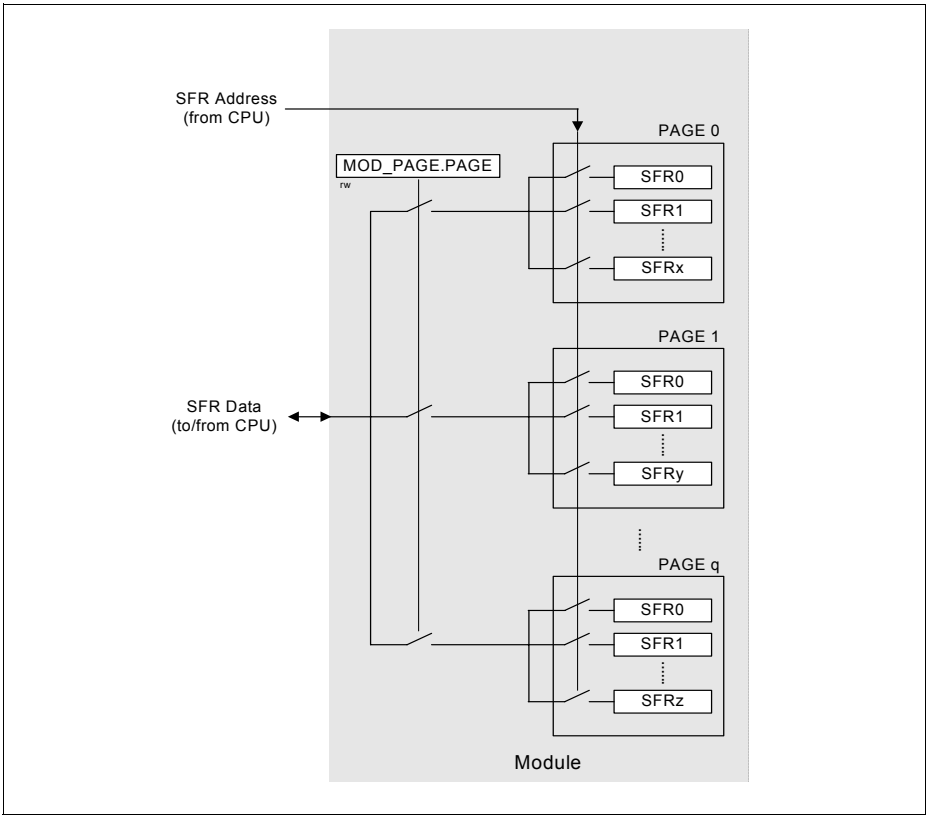
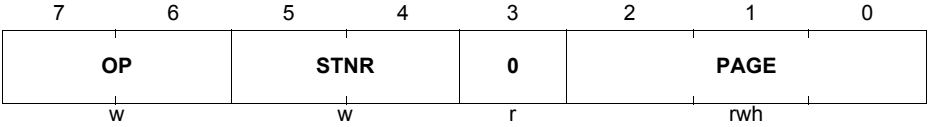


Figure 9 Address Extension by Paging

The page register has the following definition:

MOD_PAGE
Page Register for module MOD **Reset Value: 00_H**



Field	Bits	Type	Description
PAGE	[2:0]	rwh	**Page Bits** When written, the value indicates the new page. When read, the value indicates the currently active page.
STNR	[5:4]	w	**Storage Number** This number indicates which storage bit field is the target of the operation defined by bit field OP. If OP = 10_B, the contents of PAGE are saved in STx before being overwritten with the new value. If OP = 11_B, the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored. 00 ST0 is selected. 01 ST1 is selected. 10 ST2 is selected. 11 ST3 is selected.

Field	Bits	Type	Description
OP	[7:6]	w	**Operation** 0X Manual page mode. The value of STNR is ignored and PAGE is directly written. 10 New page programming with automatic page saving. The value written to the bit positions of PAGE is stored. In parallel, the previous contents of PAGE are saved in the storage bit field STx indicated by STNR. 11 Automatic restore page action. The value written to the bit positions PAGE is ignored and instead, PAGE is overwritten by the contents of the storage bit field STx indicated by STNR.
0	3	r	**Reserved** Returns 0 if read; should be written with 0.

Table 8 System Control Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$B3_H$	**ID** **Reset: 01_H** Identity Register	Bit Field	PRODID					VERID		
		Type	r					r		
$B4_H$	**PMCON0** **Reset: 00_H** Power Mode Control Register 0	Bit Field	0	WDT RST	WKRS	WK SEL	SD	PD	WS	
		Type	r	rwh	rwh	rw	rw	rwh	rw	
$B5_H$	**PMCON1** **Reset: 00_H** Power Mode Control Register 1	Bit Field	0				T2_DIS	CCU _DIS	SSC _DIS	ADC _DIS
		Type	r				rw	rw	rw	rw
$B6_H$	**OSC_CON** **Reset: 08_H** OSC Control Register	Bit Field	0			OSC PD	XPD	OSC SS	ORD RES	OSCR
		Type	r			rw	rw	rw	rwh	rh
$B7_H$	**PLL_CON** **Reset: 20_H** PLL Control Register	Bit Field	NDIV				VCO BYP	OSC DISC	RESLD	LOCK
		Type	rw				rw	rw	rwh	rh
BA_H	**CMCON** **Reset: 00_H** Clock Control Register	Bit Field	VCO SEL	0			CLKREL			
		Type	rw	r			rw			
BB_H	**PASSWD** **Reset: 07_H** Password Register	Bit Field	PASS					PROTE CT_S	MODE	
		Type	w					rh	rw	
BC_H	**FEAL** **Reset: 00_H** Flash Error Address Register Low	Bit Field	ECCERRADDR[7:0]							
		Type	rh							
BD_H	**FEAH** **Reset: 00_H** Flash Error Address Register High	Bit Field	ECCERRADDR[15:8]							
		Type	rh							
BE_H	**COCON** **Reset: 00_H** Clock Output Control Register	Bit Field	0		TLEN	COUT S	COREL			
		Type	r		rw	rw	rw			
$E9_H$	**MISC_CON** **Reset: 00_H** Miscellaneous Control Register	Bit Field	0							DFLAS HEN
		Type	r							rwh
RMAP = 0, Page 3										
$B3_H$	**XADDRH** **Reset: $F0_H$** On-Chip XRAM Address Higher Order	Bit Field	ADDRH							
		Type	rw							

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 9 WDT Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
BB_H	**WDTCON** **Reset: 00_H** Watchdog Timer Control Register	Bit Field	0		WINB EN	WDT PR	0	WDT EN	WDT RS	WDT IN
		Type	r		rw	rh	r	rw	rwh	rw
BC_H	**WDTREL** **Reset: 00_H** Watchdog Timer Reload Register	Bit Field	WDTREL							
		Type	rw							
BD_H	**WDTWINB** **Reset: 00_H** Watchdog Window-Boundary Count Register	Bit Field	WDTWINB							
		Type	rw							
BE_H	**WDTL** **Reset: 00_H** Watchdog Timer Register Low	Bit Field	WDT[7:0]							
		Type	rh							
BF_H	**WDTH** **Reset: 00_H** Watchdog Timer Register High	Bit Field	WDT[15:8]							
		Type	rh							

Table 12 Timer 2 Register Overview (cont'd)

$C1_H$	**T2_T2MOD** **Reset: 00_H** Timer 2 Mode Register	Bit Field	T2 REGS	T2 RHEN	EDGE SEL	PREN	T2PRE		DCEN
		Type	rw	rw	rw	rw	rw		rw
$C2_H$	**T2_RC2L** **Reset: 00_H** Timer 2 Reload/Capture Register Low	Bit Field	RC2[7:0]						
		Type	rwh						
$C3_H$	**T2_RC2H** **Reset: 00_H** Timer 2 Reload/Capture Register High	Bit Field	RC2[15:8]						
		Type	rwh						
$C4_H$	**T2_T2L** **Reset: 00_H** Timer 2 Register Low	Bit Field	THL2[7:0]						
		Type	rwh						
$C5_H$	**T2_T2H** **Reset: 00_H** Timer 2 Register High	Bit Field	THL2[15:8]						
		Type	rwh						

The CCU6 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 13 CCU6 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$A3_H$	**CCU6_PAGE** **Reset: 00_H** Page Register for CCU6	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, Page 0										
$9A_H$	**CCU6_CC63SRL** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC63 Low	Bit Field	CC63SL							
		Type	rw							
$9B_H$	**CCU6_CC63SRH** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC63 High	Bit Field	CC63SH							
		Type	rw							
$9C_H$	**CCU6_TCTR4L** **Reset: 00_H** Timer Control Register 4 Low	Bit Field	T12 STD	T12 STR	0		DTRES	T12 RES	T12RS	T12RR
		Type	w	w	r		w	w	w	w
$9D_H$	**CCU6_TCTR4H** **Reset: 00_H** Timer Control Register 4 High	Bit Field	T13 STD	T13 STR	0			T13 RES	T13RS	T13RR
		Type	w	w	r			w	w	w
$9E_H$	**CCU6_MCMOUTSL** **Reset: 00_H** Multi-Channel Mode Output Shadow Register Low	Bit Field	STRM CM	0	MCMPS					
		Type	w	r	rw					
$9F_H$	**CCU6_MCMOUTSH** **Reset: 00_H** Multi-Channel Mode Output Shadow Register High	Bit Field	STRHP	0	CURHS			EXPHS		
		Type	w	r	rw			rw		
$A4_H$	**CCU6_ISRL** **Reset: 00_H** Capture/Compare Interrupt Status Reset Register Low	Bit Field	RT12P M	RT12O M	RCC62 F	RCC62 R	RCC61 F	RCC61 R	RCC60 F	RCC60 R
		Type	w	w	w	w	w	w	w	w
$A5_H$	**CCU6_ISRH** **Reset: 00_H** Capture/Compare Interrupt Status Reset Register High	Bit Field	RSTR	RIDLE	RWHE	RCHE	0	RTRPF	RT13 PM	RT13 CM
		Type	w	w	w	w	r	w	w	w
$A6_H$	**CCU6_CMPMODIFL** **Reset: 00_H** Compare State Modification Register Low	Bit Field	0	MCC63 S	0			MCC62 S	MCC61 S	MCC60 S
		Type	r	w	r			w	w	w
$A7_H$	**CCU6_CMPMODIFH** **Reset: 00_H** Compare State Modification Register High	Bit Field	0	MCC63 R	0			MCC62 R	MCC61 R	MCC60 R
		Type	r	w	r			w	w	w
FA_H	**CCU6_CC60SRL** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC60 Low	Bit Field	CC60SL							
		Type	rwh							

Table 17 Interrupt Vector Addresses (cont'd)

XINTR6	0033_H	ADC	EADC	IEN1
XINTR7	$003B_H$	SSC	ESSC	
XINTR8	0043_H	External Interrupt 2	EX2	
XINTR9	$004B_H$	External Interrupt 3	EXM	
		External Interrupt 4		
		External Interrupt 5		
		External Interrupt 6		
XINTR10	0053_H	CCU6 INP0	ECCIP0	
XINTR11	$005B_H$	CCU6 INP1	ECCIP1	
XINTR12	0063_H	CCU6 INP2	ECCIP2	
XINTR13	$006B_H$	CCU6 INP3	ECCIP3	

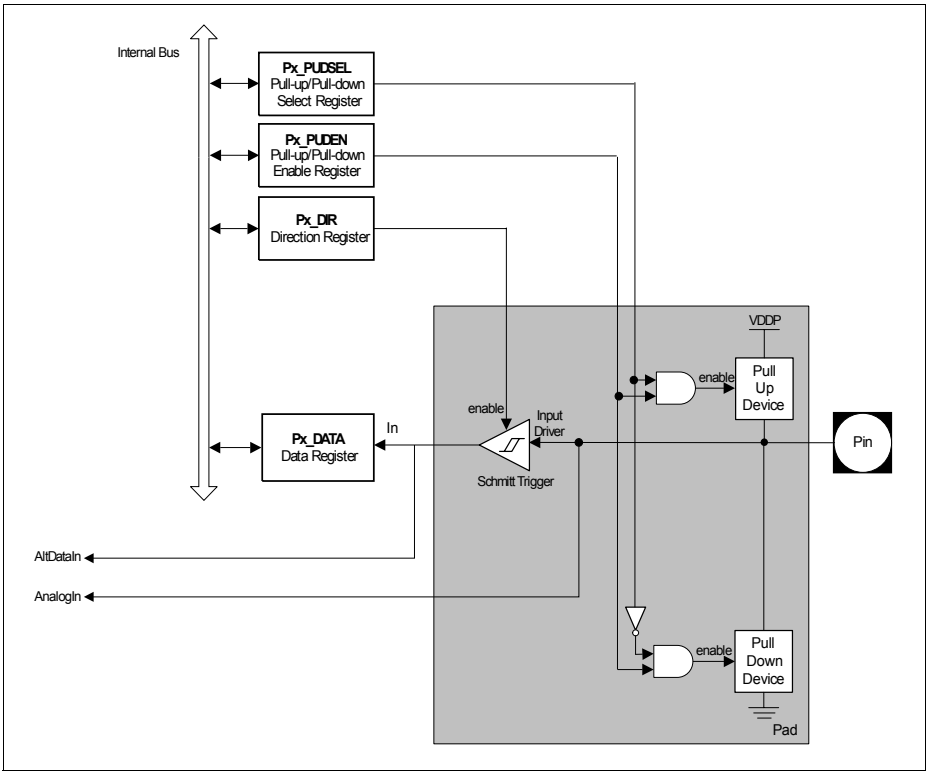


Figure 19 General Structure of Input Port

Table 21 System frequency (f_{sys} = 80 MHz)

Oscillator	fosc	N	P	K	fsys
On-chip	10 MHz	16	1	2	80 MHz
External	10 MHz	16	1	2	80 MHz
	8 MHz	20	1	2	80 MHz
	5 MHz	32	1	2	80 MHz

Table 22 shows the VCO range for the XC866.

Table 22 VCO Range

f_{VCOmin}	f_{VCOmax}	$f_{VCOFREEmin}$	$f_{VCOFREEmax}$	Unit
150	200	20	80	MHz
100	150	10	80	MHz

3.8.1 Recommended External Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 4 MHz to 12 MHz. Additionally, it is necessary to have two load capacitances C_{X1} and C_{X2}, and depending on the crystal type, a series resistor R_{X2}, to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. The C_{X1} and C_{X2} values shown in Figure 24 can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the crystal vendor using the negative resistance method. Oscillation measurement with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal system.

When using an external clock signal, the signal must be connected to XTAL1. XTAL2 is left open (unconnected).

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must also be verified by the resonator vendor.

Figure 24 shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode.

3.9 Power Saving Modes

The power saving modes of the XC866 provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see **Figure 26**) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode

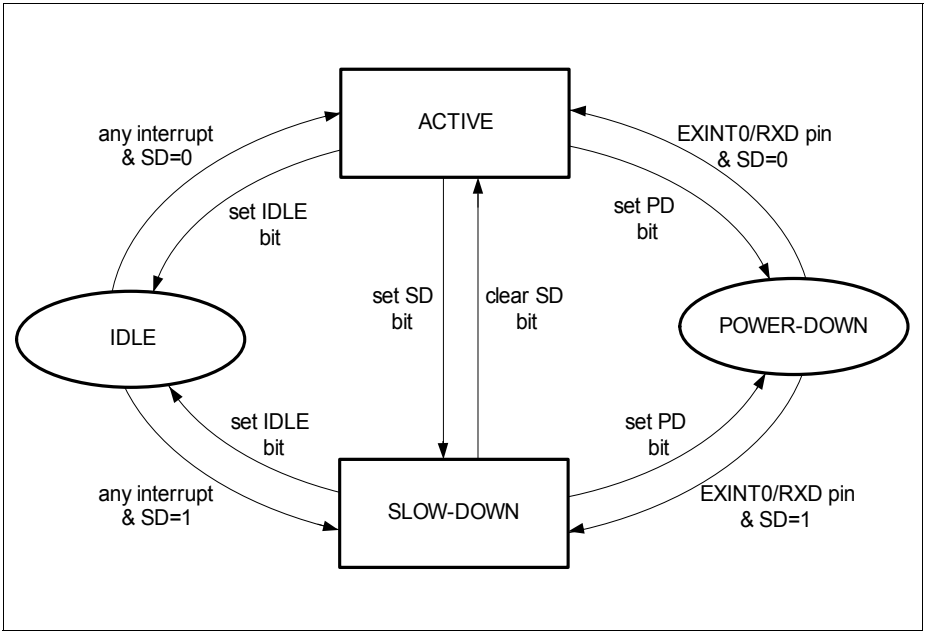


Figure 26 Transition between Power Saving Modes

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

Figure 31 shows the block diagram of the SSC.

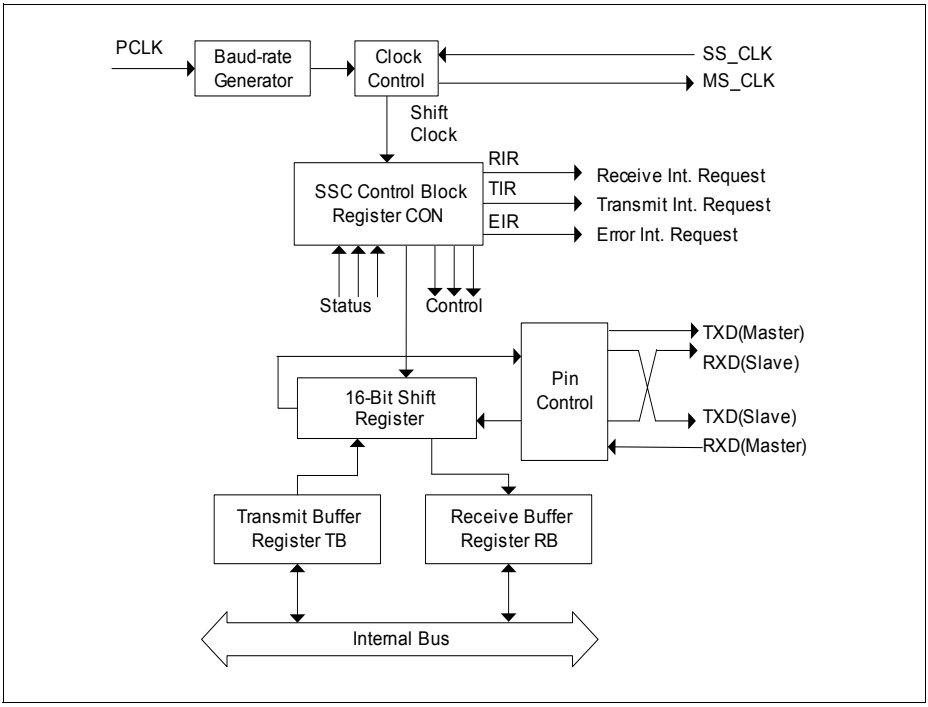


Figure 31 SSC Block Diagram

3.16 Timer 2

Timer 2 is a 16-bit general purpose timer (THL2) that has two modes of operation, a 16-bit auto-reload mode and a 16-bit one channel capture mode. If the prescalar is disabled, Timer 2 counts with an input clock of PCLK/12. Timer 2 continues counting as long as it is enabled.

Table 29 Timer 2 Modes

Mode	Description
Auto-reload	**Up/Down Count Disabled** • Count up only • Start counting from 16-bit reload value, overflow at $FFFF_H$ • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmble reload value in register RC2 • Interrupt is generated with reload event
	Up/Down Count Enabled • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up – Start counting from 16-bit reload value, overflow at $FFFF_H$ – Reload event triggered by overflow condition – Programmble reload value in register RC2 • Count down – Start counting from $FFFF_H$, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at $FFFF_H$
Channel capture	• Count up only • Start counting from 0000_H, overflow at $FFFF_H$ • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generated with reload or capture event

The block diagram of the CCU6 module is shown in **Figure 32**.

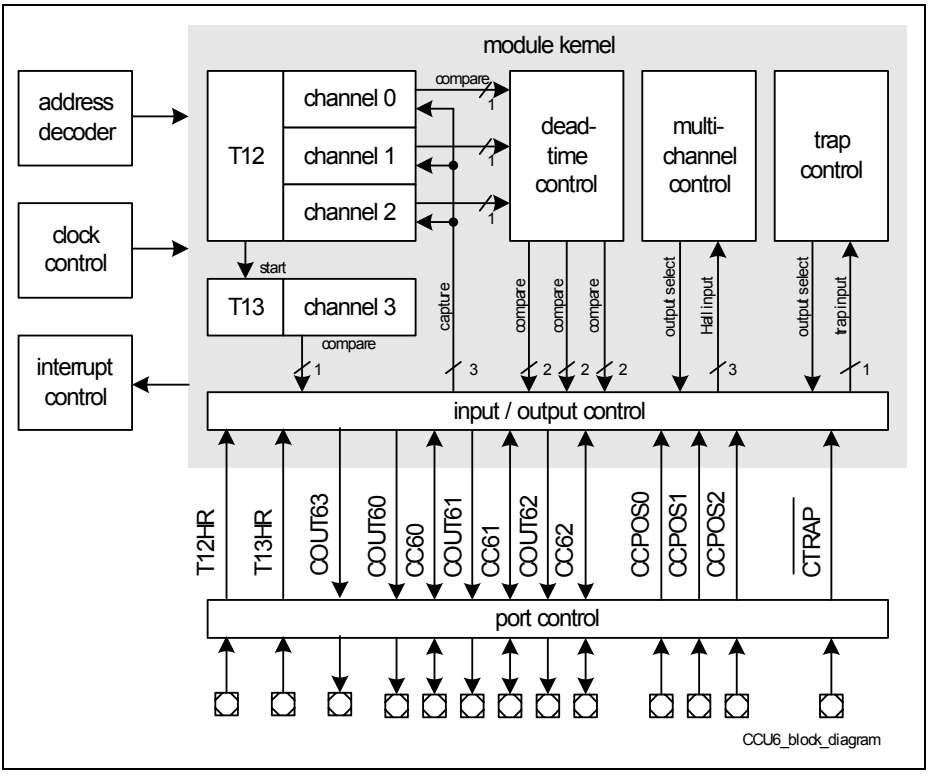


Figure 32 CCU6 Block Diagram

4 Electrical Parameters

Chapter 4 provides the characteristics of the electrical parameters which are implementation-specific for the XC866.

Note: The electrical parameters are valid for the XC866-4FR and XC866-2FR. The electrical parameters for the ROM variants and XC866-1FR are preliminary, differences from XC866-4FR and XC866-2FR are stated explicitly.

4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 4.2** and **Section 4.3**.

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC866 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC866 and must be regarded for a system design.
- **SR**
  These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC866 is designed in.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when VDDP is powered off.

4.3.5 JTAG Timing

Table 44 TCK Clock Timing (Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
TCK clock period	t_{TCK}	SR	50	–	ns
TCK high time	t_1	SR	20	–	ns
TCK low time	t_2	SR	20	–	ns
TCK clock rise time	t_3	SR	–	4	ns
TCK clock fall time	t_4	SR	–	4	ns

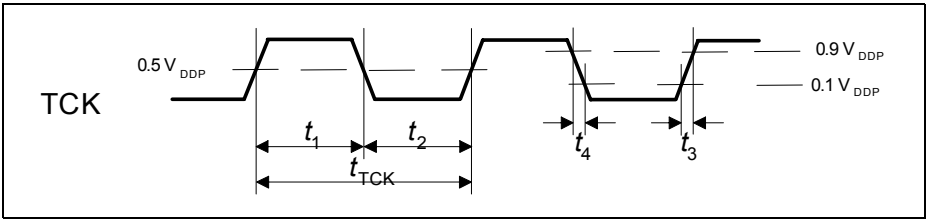


Figure 43 TCK Clock Timing

4.3.6 SSC Master Mode Timing

Table 46 SSC Master Mode Timing (Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit Values		Unit
			min.	max.	
SCLK clock period	t_0	CC	2*T_{SSC} [1]	–	ns
MTSR delay from SCLK ↓	t_1	CC	0	8	ns
MRST setup to SCLK ↑	t_2	SR	22	–	ns
MRST hold from SCLK ↑	t_3	SR	0	–	ns

[1] T_{SSCmin} = T_{CPU} = 1/f_{CPU}. When f_{CPU} = 26.7MHz, t_0 = 74.9ns. T_{CPU} is the CPU clock period.

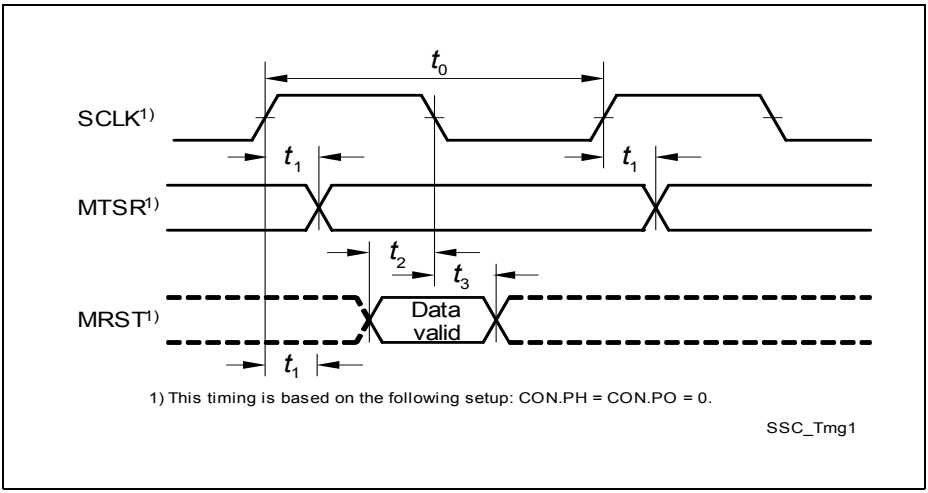


Figure 45 SSC Master Mode Timing