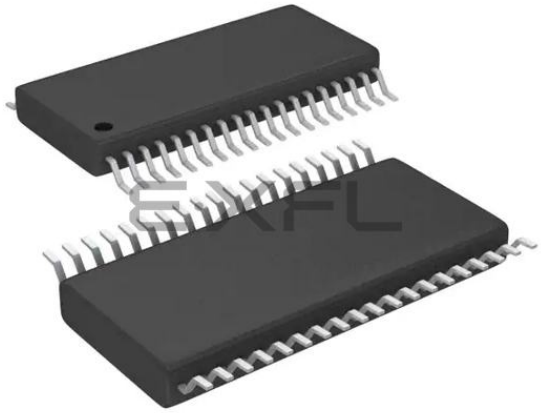

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | XC800 |
| Core Size | 8-Bit |
| Speed | 86MHz |
| Connectivity | LINbus, SSI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 19 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 768 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 38-TFSOP (0.173", 4.40mm Width) |
| Supplier Device Package | PG-TSSOP-38 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc866l-2fra-be |

**XC866 Data Sheet**
**Revision History: 2007-10** V1.2

Previous Version: V 0.1, 2005-01
V1.0, 2006-02
V1.1, 2006-12

| Page | Subjects (major changes since last revision) |
|---|---|
| 3 | Device summary table is updated for Flash 4-Kb and ROM variants. |
| 13 | Footnote is added to MBC pin; description of $V_{DDP}$ pin is updated. |
| 25 | Section on bit protection scheme and access type of register bit field PASSWD.PASS are updated. |
| 26 | Access type of PAGE bits of all module page registers are corrected to rwh. |
| 29 | Access type of Px_DIR register bits are corrected to rwh |
| 38 | New bullet point on Flash delivery state is added to the feature list. |
| 88 | Digital power supply voltage are differentiated for 5V and 3.3V variants. |
| 89 | New parameters on XTAL1 hysteresis and Voltage on GPIO pins during $V_{DDP}$ power-off condition are added. |
| 104 | Figure on Power-on reset timing is updated. |
| | |

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## 2.2 Logic Symbol

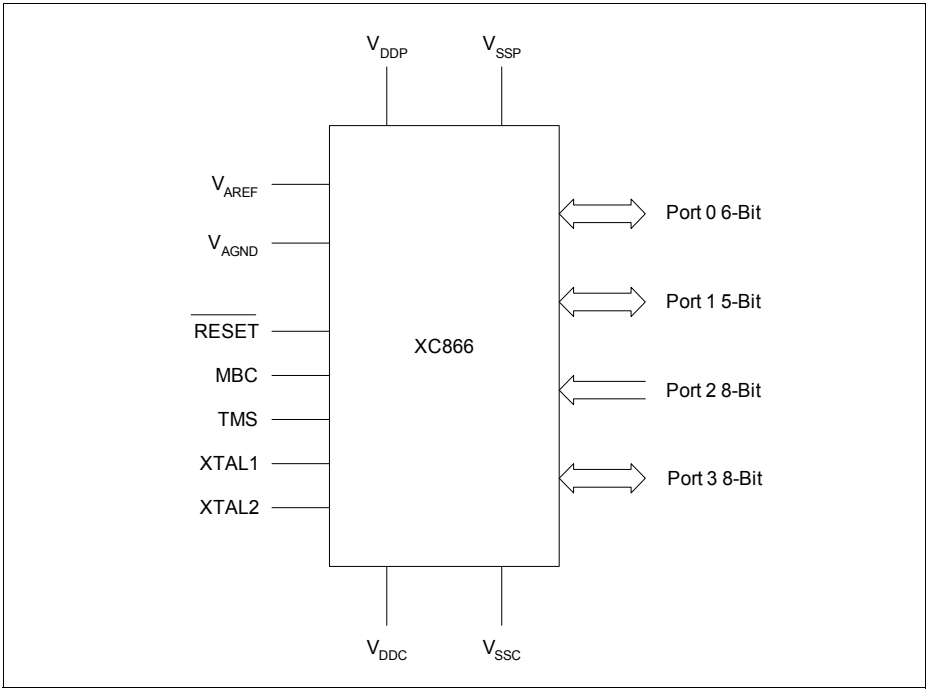



**Figure 3 XC866 Logic Symbol**

## 2.3 Pin Configuration

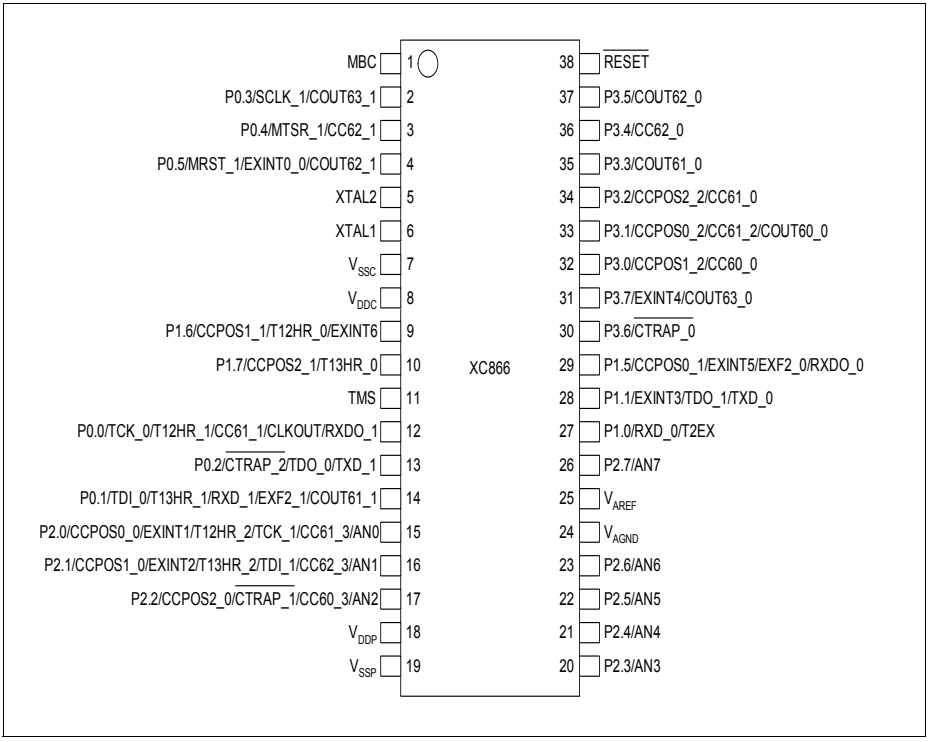



**Figure 4 XC866 Pin Configuration, PG-TSSOP-38 Package** (top view)

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|---|---|---|---|---|
| **P3** | | I | | **Port 3**<br>Port 3 is a bidirectional general purpose I/O port. It can be used as alternate functions for the CCU6. |
| P3.0 | 32 | | Hi-Z | CCPOS1_2 CCU6 Hall Input 1<br>CC60_0 Input/Output of Capture/Compare channel 0 |
| P3.1 | 33 | | Hi-Z | CCPOS0_2 CCU6 Hall Input 0<br>CC61_2 Input/Output of Capture/Compare channel 1<br>COUT60_0 Output of Capture/Compare channel 0 |
| P3.2 | 34 | | Hi-Z | CCPOS2_2 CCU6 Hall Input 2<br>CC61_0 Input/Output of Capture/Compare channel 1 |
| P3.3 | 35 | | Hi-Z | COUT61_0 Output of Capture/Compare channel 1 |
| P3.4 | 36 | | Hi-Z | CC62_0 Input/Output of Capture/Compare channel 2 |
| P3.5 | 37 | | Hi-Z | COUT62_0 Output of Capture/Compare channel 2 |
| P3.6 | 30 | | PD | $\overline{\text{CTRAP\_0}}$ CCU6 Trap Input |
| P3.7 | 31 | | Hi-Z | EXINT4 External Interrupt Input 4<br>COUT63_0 Output of Capture/Compare channel 3 |

**Figure 7** illustrates the memory address spaces of the XC866-4RR device.

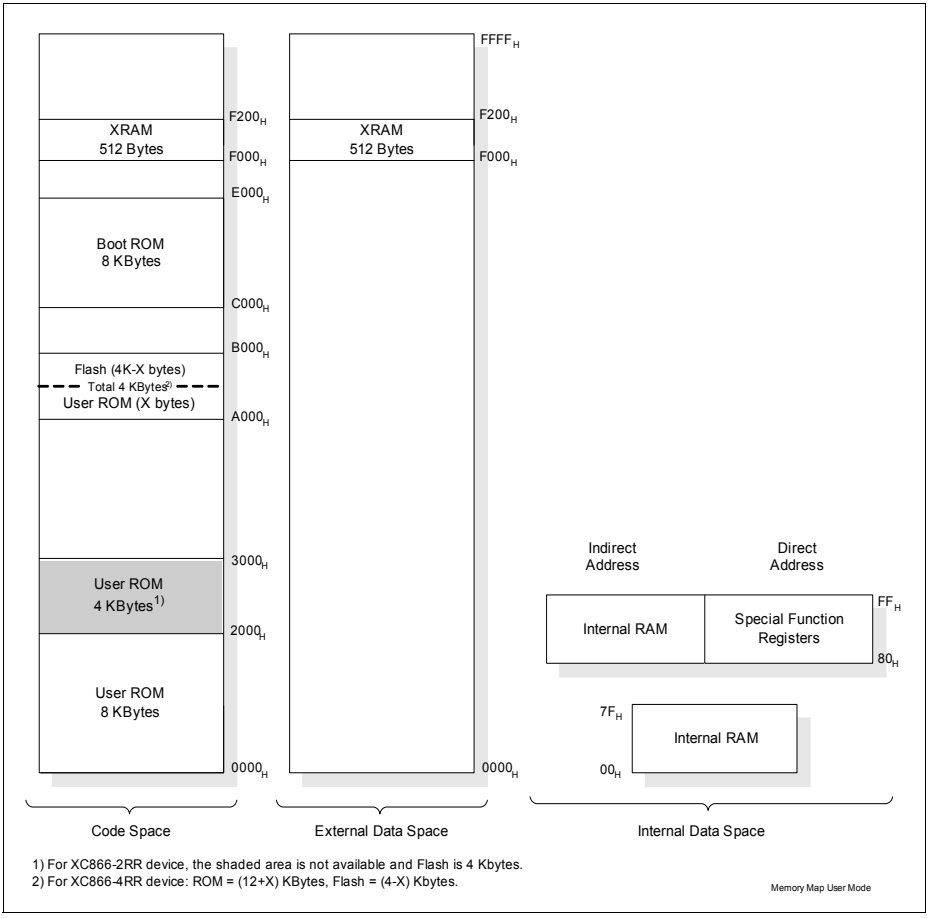



**Figure 7 Memory Map of XC866 ROM Devices**

### 3.2.4 XC866 Register Overview

The SFRs of the XC866 are organized into groups according to their functional units. The contents (bits) of the SFRs are summarized in **Table 7** to **Table 15**, with the addresses of the bitaddressable SFRs appearing in bold typeface.

The CPU SFRs can be accessed in both the standard and mapped memory areas (RMAP = 0 or 1).

**Table 7 CPU Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 0 or 1 | | | | | | | | | | |
| $81_H$ | **SP** **Reset: $07_H$**<br>Stack Pointer Register | Bit Field | SP | | | | | | | |
| | | Type | rw | | | | | | | |
| $82_H$ | **DPL** **Reset: $00_H$**<br>Data Pointer Register Low | Bit Field | DPL7 | DPL6 | DPL5 | DPL4 | DPL3 | DPL2 | DPL1 | DPL0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $83_H$ | **DPH** **Reset: $00_H$**<br>Data Pointer Register High | Bit Field | DPH7 | DPH6 | DPH5 | DPH4 | DPH3 | DPH2 | DPH1 | DPH0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $87_H$ | **PCON** **Reset: $00_H$**<br>Power Control Register | Bit Field | SMOD | 0 | | | GF1 | GF0 | 0 | IDLE |
| | | Type | rw | r | | | rw | rw | r | rw |
| **$88_H$** | **TCON** **Reset: $00_H$**<br>Timer Control Register | Bit Field | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
| | | Type | rwh | rw | rwh | rw | rwh | rw | rwh | rw |
| $89_H$ | **TMOD** **Reset: $00_H$**<br>Timer Mode Register | Bit Field | GATE1 | 0 | T1M | | GATE0 | 0 | T0M | |
| | | Type | rw | r | rw | | rw | r | rw | |
| $8A_H$ | **TL0** **Reset: $00_H$**<br>Timer 0 Register Low | Bit Field | VAL | | | | | | | |
| | | Type | rwh | | | | | | | |
| $8B_H$ | **TL1** **Reset: $00_H$**<br>Timer 1 Register Low | Bit Field | VAL | | | | | | | |
| | | Type | rwh | | | | | | | |
| $8C_H$ | **TH0** **Reset: $00_H$**<br>Timer 0 Register High | Bit Field | VAL | | | | | | | |
| | | Type | rwh | | | | | | | |
| $8D_H$ | **TH1** **Reset: $00_H$**<br>Timer 1 Register High | Bit Field | VAL | | | | | | | |
| | | Type | rwh | | | | | | | |
| **$98_H$** | **SCON** **Reset: $00_H$**<br>Serial Channel Control Register | Bit Field | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |
| | | Type | rw | rw | rw | rw | rw | rwh | rwh | rwh |
| $99_H$ | **SBUF** **Reset: $00_H$**<br>Serial Data Buffer Register | Bit Field | VAL | | | | | | | |
| | | Type | rwh | | | | | | | |
| $A2_H$ | **EO** **Reset: $00_H$**<br>Extended Operation Register | Bit Field | 0 | | | TRAP_EN | 0 | | | DPSEL0 |
| | | Type | r | | | rw | r | | | rw |
| **$A8_H$** | **IEN0** **Reset: $00_H$**<br>Interrupt Enable Register 0 | Bit Field | EA | 0 | ET2 | ES | ET1 | EX1 | ET0 | EX0 |
| | | Type | rw | r | rw | rw | rw | rw | rw | rw |
| **$B8_H$** | **IP** **Reset: $00_H$**<br>Interrupt Priority Register | Bit Field | 0 | | PT2 | PS | PT1 | PX1 | PT0 | PX0 |
| | | Type | r | | rw | rw | rw | rw | rw | rw |
| $B9_H$ | **IPH** **Reset: $00_H$**<br>Interrupt Priority Register High | Bit Field | 0 | | PT2H | PSH | PT1H | PX1H | PT0H | PX0H |
| | | Type | r | | rw | rw | rw | rw | rw | rw |
| **$D0_H$** | **PSW** **Reset: $00_H$**<br>Program Status Word Register | Bit Field | CY | AC | F0 | RS1 | RS0 | OV | F1 | P |
| | | Type | rw | rwh | rwh | rw | rw | rwh | rwh | rh |
| **$E0_H$** | **ACC** **Reset: $00_H$**<br>Accumulator Register | Bit Field | ACC7 | ACC6 | ACC5 | ACC4 | ACC3 | ACC2 | ACC1 | ACC0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| **$E8_H$** | **IEN1** **Reset: $00_H$**<br>Interrupt Enable Register 1 | Bit Field | ECCIP3 | ECCIP2 | ECCIP1 | ECCIP0 | EXM | EX2 | ESSC | EADC |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |

**Table 11 ADC Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $CA_H$ | **ADC_RESR0L** **Reset: $00_H$**<br>Result Register 0 Low | Bit Field | RESULT[1:0] | | 0 | VF | DRC | CHNR | | |
| | | Type | rh | | r | rh | rh | rh | | |
| $CB_H$ | **ADC_RESR0H** **Reset: $00_H$**<br>Result Register 0 High | Bit Field | RESULT[9:2] | | | | | | | |
| | | Type | rh | | | | | | | |
| $CC_H$ | **ADC_RESR1L** **Reset: $00_H$**<br>Result Register 1 Low | Bit Field | RESULT[1:0] | | 0 | VF | DRC | CHNR | | |
| | | Type | rh | | r | rh | rh | rh | | |
| $CD_H$ | **ADC_RESR1H** **Reset: $00_H$**<br>Result Register 1 High | Bit Field | RESULT[9:2] | | | | | | | |
| | | Type | rh | | | | | | | |
| $CE_H$ | **ADC_RESR2L** **Reset: $00_H$**<br>Result Register 2 Low | Bit Field | RESULT[1:0] | | 0 | VF | DRC | CHNR | | |
| | | Type | rh | | r | rh | rh | rh | | |
| $CF_H$ | **ADC_RESR2H** **Reset: $00_H$**<br>Result Register 2 High | Bit Field | RESULT[9:2] | | | | | | | |
| | | Type | rh | | | | | | | |
| $D2_H$ | **ADC_RESR3L** **Reset: $00_H$**<br>Result Register 3 Low | Bit Field | RESULT[1:0] | | 0 | VF | DRC | CHNR | | |
| | | Type | rh | | r | rh | rh | rh | | |
| $D3_H$ | **ADC_RESR3H** **Reset: $00_H$**<br>Result Register 3 High | Bit Field | RESULT[9:2] | | | | | | | |
| | | Type | rh | | | | | | | |
| RMAP = 0, Page 3 | | | | | | | | | | |
| $CA_H$ | **ADC_RESRA0L** **Reset: $00_H$**<br>Result Register 0, View A Low | Bit Field | RESULT[2:0] | | | VF | DRC | CHNR | | |
| | | Type | rh | | | rh | rh | rh | | |
| $CB_H$ | **ADC_RESRA0H** **Reset: $00_H$**<br>Result Register 0, View A High | Bit Field | RESULT[10:3] | | | | | | | |
| | | Type | rh | | | | | | | |
| $CC_H$ | **ADC_RESRA1L** **Reset: $00_H$**<br>Result Register 1, View A Low | Bit Field | RESULT[2:0] | | | VF | DRC | CHNR | | |
| | | Type | rh | | | rh | rh | rh | | |
| $CD_H$ | **ADC_RESRA1H** **Reset: $00_H$**<br>Result Register 1, View A High | Bit Field | RESULT[10:3] | | | | | | | |
| | | Type | rh | | | | | | | |
| $CE_H$ | **ADC_RESRA2L** **Reset: $00_H$**<br>Result Register 2, View A Low | Bit Field | RESULT[2:0] | | | VF | DRC | CHNR | | |
| | | Type | rh | | | rh | rh | rh | | |
| $CF_H$ | **ADC_RESRA2H** **Reset: $00_H$**<br>Result Register 2, View A High | Bit Field | RESULT[10:3] | | | | | | | |
| | | Type | rh | | | | | | | |
| $D2_H$ | **ADC_RESRA3L** **Reset: $00_H$**<br>Result Register 3, View A Low | Bit Field | RESULT[2:0] | | | VF | DRC | CHNR | | |
| | | Type | rh | | | rh | rh | rh | | |
| $D3_H$ | **ADC_RESRA3H** **Reset: $00_H$**<br>Result Register 3, View A High | Bit Field | RESULT[10:3] | | | | | | | |
| | | Type | rh | | | | | | | |
| RMAP = 0, Page 4 | | | | | | | | | | |
| $CA_H$ | **ADC_RCR0** **Reset: $00_H$**<br>Result Control Register 0 | Bit Field | VFCTR | WFR | 0 | IEN | 0 | | | DRCTR |
| | | Type | rw | rw | r | rw | r | | | rw |
| $CB_H$ | **ADC_RCR1** **Reset: $00_H$**<br>Result Control Register 1 | Bit Field | VFCTR | WFR | 0 | IEN | 0 | | | DRCTR |
| | | Type | rw | rw | r | rw | r | | | rw |
| $CC_H$ | **ADC_RCR2** **Reset: $00_H$**<br>Result Control Register 2 | Bit Field | VFCTR | WFR | 0 | IEN | 0 | | | DRCTR |
| | | Type | rw | rw | r | rw | r | | | rw |
| $CD_H$ | **ADC_RCR3** **Reset: $00_H$**<br>Result Control Register 3 | Bit Field | VFCTR | WFR | 0 | IEN | 0 | | | DRCTR |
| | | Type | rw | rw | r | rw | r | | | rw |
| $CE_H$ | **ADC_VFCR** **Reset: $00_H$**<br>Valid Flag Clear Register | Bit Field | 0 | | | | VFC3 | VFC2 | VFC1 | VFC0 |
| | | Type | r | | | | w | w | w | w |
| RMAP = 0, Page 5 | | | | | | | | | | |

**Table 21 System frequency ($f_{sys}$ = 80 MHz)**

| Oscillator | fosc | N | P | K | fsys |
|---|---|---|---|---|---|
| On-chip | 10 MHz | 16 | 1 | 2 | 80 MHz |
| External | 10 MHz | 16 | 1 | 2 | 80 MHz |
| | 8 MHz | 20 | 1 | 2 | 80 MHz |
| | 5 MHz | 32 | 1 | 2 | 80 MHz |

Table 22 shows the VCO range for the XC866.

**Table 22 VCO Range**

| $f_{VCOmin}$ | $f_{VCOmax}$ | $f_{VCOFREEmin}$ | $f_{VCOFREEmax}$ | Unit |
|---|---|---|---|---|
| 150 | 200 | 20 | 80 | MHz |
| 100 | 150 | 10 | 80 | MHz |

### 3.8.1 Recommended External Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 4 MHz to 12 MHz. Additionally, it is necessary to have two load capacitances $C_{X1}$ and $C_{X2}$, and depending on the crystal type, a series resistor $R_{X2}$, to limit the current. A test resistor $R_Q$ may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. $R_Q$ values are typically specified by the crystal vendor. The $C_{X1}$ and $C_{X2}$ values shown in Figure 24 can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the crystal vendor using the negative resistance method. Oscillation measurement with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal system.

When using an external clock signal, the signal must be connected to XTAL1. XTAL2 is left open (unconnected).

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must also be verified by the resonator vendor.

Figure 24 shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode.

## 3.9 Power Saving Modes

The power saving modes of the XC866 provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see **Figure 26**) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode

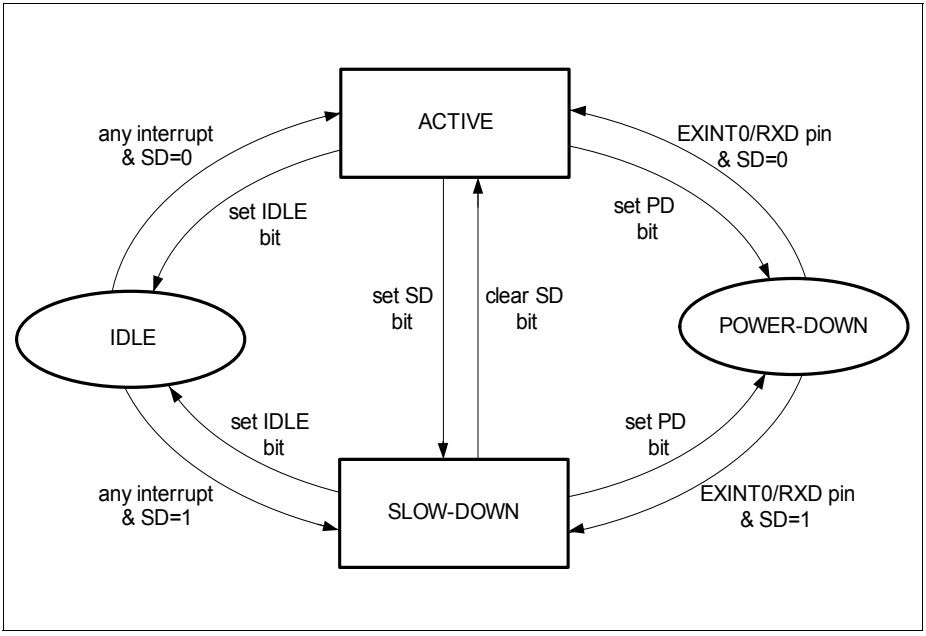



**Figure 26 Transition between Power Saving Modes**

If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert WDTTO) and the reset prewarning is entered. The prewarning period lasts for $30_H$ count, after which the system is reset (assert WDTRST).

The WDT has a “programmable window boundary” which disallows any refresh during the WDT’s count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from $0000_H$ to the value obtained from the concatenation of WDTWINB and $00_H$.

After being serviced, the WDT continues counting up from the value (<WDTREL> * $2^8$). The time period for an overflow of the WDT is programmable in two ways:

- the input frequency to the WDT can be selected to be either $f_{PCLK}/2$ or $f_{PCLK}/128$
- the reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, $P_{WDT}$, between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}}$$

If the Window-Boundary Refresh feature of the WDT is enabled, the period $P_{WDT}$ between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see **Figure 28**. This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB should not be smaller than WDTREL.

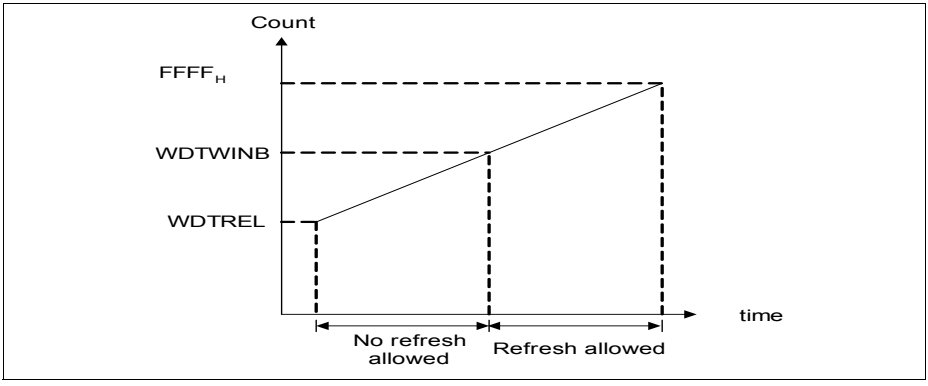



**Figure 28 WDT Timing Diagram**

## 3.13 LIN Protocol

The UART can be used to support the Local Interconnect Network (LIN) protocol for both master and slave operations. The LIN baud rate detection feature provides the capability to detect the baud rate within LIN protocol using Timer 2. This allows the UART to be synchronized to the LIN baud rate for data transmission and reception.

LIN is a holistic communication concept for local interconnected networks in vehicles. The communication is based on the SCI (UART) data format, a single-master/multiple-slave concept, a clock synchronization for nodes without stabilized time base. An attractive feature of LIN is self-synchronization of the slave nodes without a crystal or ceramic resonator, which significantly reduces the cost of hardware platform. Hence, the baud rate must be calculated and returned with every message frame.

The structure of a LIN frame is shown in **Figure 30**. The frame consists of the:

- header, which comprises a Break (13-bit time low), Synch Byte ($55_H$), and ID field
- response time
- data bytes (according to UART protocol)
- checksum

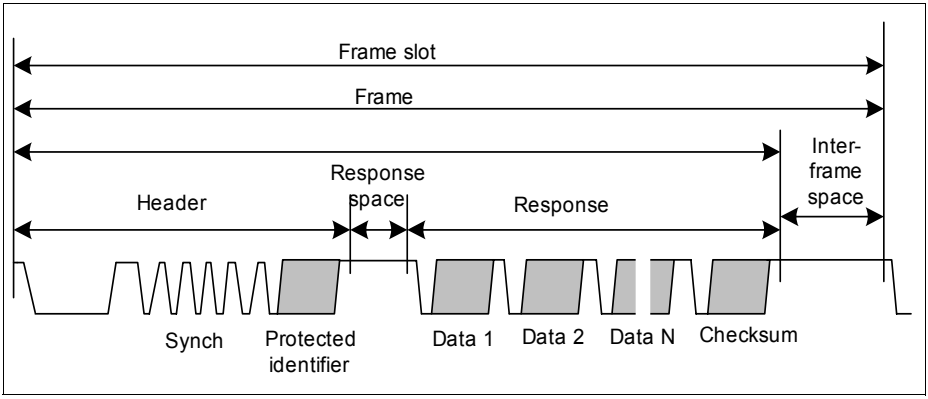



**Figure 30 Structure of LIN Frame**

### 3.13.1 LIN Header Transmission

LIN header transmission is only applicable in master mode. In the LIN communication, a master task decides when and which frame is to be transferred on the bus. It also identifies a slave task to provide the data transported by each frame. The information needed for the handshaking between the master and slave tasks is provided by the master task through the header portion of the frame.

The header consists of a break and synch pattern followed by an identifier. Among these three fields, only the break pattern cannot be transmitted as a normal 8-bit UART data.

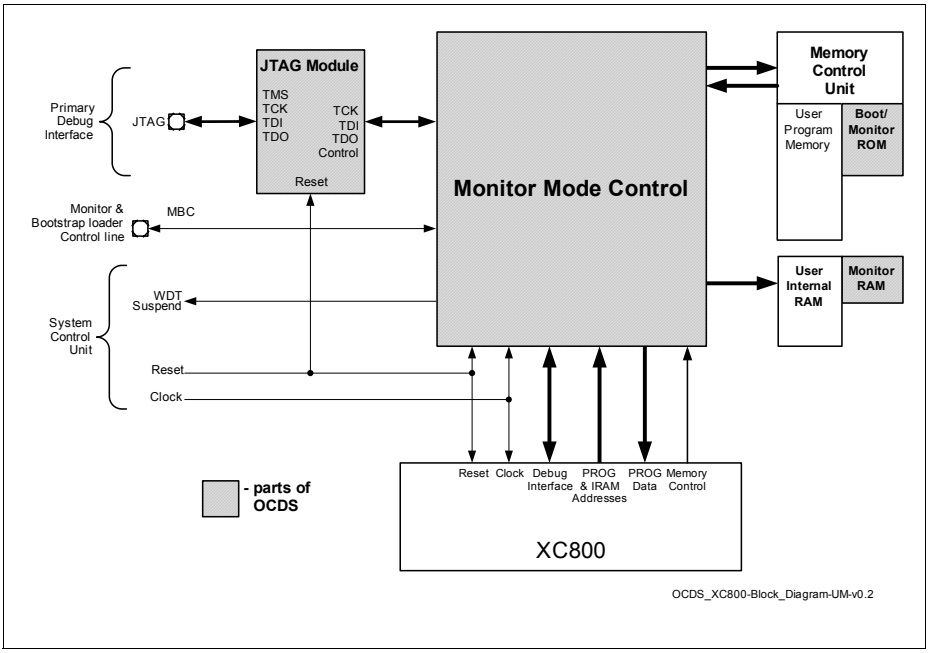



**Figure 35 OCDS Block Diagram**

### 3.19.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode $04_H$), and the same is also true immediately after reset.

The JTAG ID register contents for the XC866 devices are given in **Table 31**.

**Table 31 JTAG ID Summary**

| Device Type | Device Name | JTAG ID |
|---|---|---|
| Flash | XC866L-4FR | 1010 0083$_H$ |
| | XC866-4FR | 100F 5083$_H$ |
| | XC866L-2FR | 1010 2083$_H$ |
| | XC866-2FR | 1010 1083$_H$ |
| | XC866L-1FR | 1013 8083$_H$ |
| | XC866-1FR | 1013 8083$_H$ |

# 4 Electrical Parameters

**Chapter 4** provides the characteristics of the electrical parameters which are implementation-specific for the XC866.

*Note: The electrical parameters are valid for the XC866-4FR and XC866-2FR. The electrical parameters for the ROM variants and XC866-1FR are preliminary, differences from XC866-4FR and XC866-2FR are stated explicitly.*

## 4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 4.2** and **Section 4.3**.

### 4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC866 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC866 and must be regarded for a system design.
- **SR**
  These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC866 is designed in.

### 4.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the XC866. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

**Table 33 Operating Condition Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes/ Conditions |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Digital power supply voltage | $V_{DDP}$ | 4.5 | 5.5 | V | 5V Device |
| Digital power supply voltage | $V_{DDP}$ | 3.0 | 3.6 | V | 3.3V Device |
| Digital ground voltage | $V_{SS}$ | 0 | | V | |
| Digital core supply voltage | $V_{DDC}$ | 2.3 | 2.7 | V | |
| System Clock Frequency[1)] | $f_{SYS}$ | 74 | 86 | MHz | |
| Ambient temperature | $T_A$ | -40 | 85 | °C | SAF-XC866... |
| | | -40 | 125 | °C | SAK-XC866... |

[1)] $f_{SYS}$ is the PLL output clock. During normal operating mode, CPU clock is $f_{SYS}$ / 3. Please refer to **Figure 25** for detailed description.

### 4.2.2 Supply Threshold Characteristics

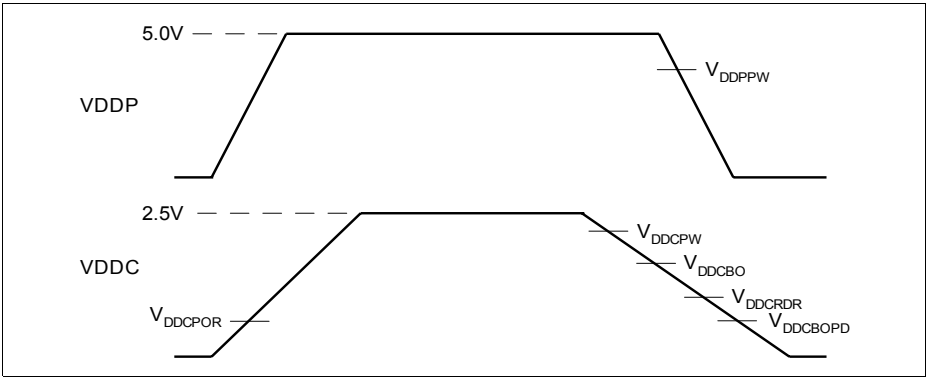



**Figure 36 Supply Threshold Parameters**

**Table 35 Supply Threshold Parameters (Operating Conditions apply)**

| Parameters | Symbol | | Limit Values | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| $V_{DDC}$ prewarning voltage[1] | $V_{DDCPW}$ | CC | 2.2 | 2.3 | 2.4 | V | |
| $V_{DDC}$ brownout voltage in active mode[1] | $V_{DDCBO}$ | CC | 2.0 | 2.1 | 2.2 | V | XC866-4FR, XC866-2FR |
| | | | 2.0 | 2.1 | 2.3 | V | XC866-1FR, ROM device |
| RAM data retention voltage | $V_{DDCRDR}$ | CC | 0.9 | 1.0 | 1.1 | V | |
| $V_{DDC}$ brownout voltage in power-down mode[2] | $V_{DDCBOPD}$ | CC | 1.3 | 1.5 | 1.7 | V | |
| $V_{DDP}$ prewarning voltage[3] | $V_{DDPPW}$ | CC | 3.4 | 4.0 | 4.6 | V | |
| Power-on reset voltage[2][4] | $V_{DDCPOR}$ | CC | 1.3 | 1.5 | 1.7 | V | |

1) Detection is disabled in power-down mode.

2) Detection is enabled in both active and power-down mode.

3) Detection is enabled for external power supply of 5.0V.
Detection must be disabled for external power supply of 3.3V.

4) The reset of EVR is extended by 300 µs typically after the VDDC reaches the power-on reset voltage.

**Table 39 Power Supply Current Parameters (Operating Conditions apply; $V_{DDP}$ = 3.3V range)**

| Parameter | Symbol | Limit Values | | Unit | Test Condition Remarks |
|---|---|---|---|---|---|
| | | typ.[1] | max.[2] | | |
| **$V_{DDP}$ = 3.3V Range** | | | | | |
| Active Mode | $I_{DDP}$ | 21.5 | 23.3 | mA | [3] |
| Idle Mode | $I_{DDP}$ | 16.4 | 18.9 | mA | XC866-4FR, XC866-2FR [4] |
| | | 11.2 | 13.5 | mA | XC866-1FR, ROM device [4] |
| Active Mode with slow-down enabled | $I_{DDP}$ | 6.8 | 8 | mA | XC866-4FR, XC866-2FR [5] |
| | | 5.4 | 7.3 | mA | XC866-1FR, ROM device [5] |
| Idle Mode with slow-down enabled | $I_{DDP}$ | 6.8 | 7.8 | mA | XC866-4FR, XC866-2FR [6] |
| | | 4.9 | 6.9 | mA | XC866-1FR, ROM device [6] |

1) The typical $I_{DDP}$ values are periodically measured at $T_A$ = + 25 °C and $V_{DDP}$ = 3.3 V.

2) The maximum $I_{DDP}$ values are measured under worst case conditions ($T_A$ = + 125 °C and $V_{DDP}$ = 3.6 V).

3) $I_{DDP}$ (active mode) is measured with: CPU clock and input clock to all peripherals running at 26.7 MHz(set by on-chip oscillator of 10 MHz and NDIV in PLL_CON to $0010_B$), $\overline{RESET}$ = $V_{DDP}$, no load on ports.

4) $I_{DDP}$ (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 26.7 MHz, $\overline{RESET}$ = $V_{DDP}$, no load on ports.

5) $I_{DDP}$ (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 833 KHz by setting CLKREL in CMCON to $0101_B$, $\overline{RESET}$ = $V_{DDP}$, no load on ports.

6) $I_{DDP}$ (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enable and running at 833 KHz by setting CLKREL in CMCON to $0101_B$,, $\overline{RESET}$ = $V_{DDP}$, no load on ports.

## 4.3 AC Parameters

### 4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 38**, **Figure 39** and **Figure 40**.

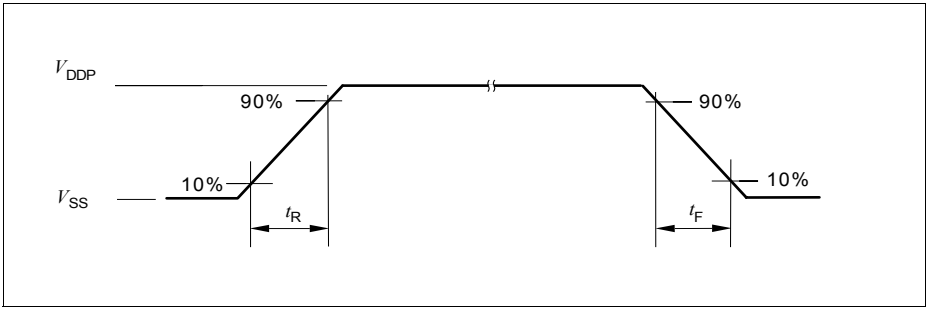



**Figure 38 Rise/Fall Time Parameters**

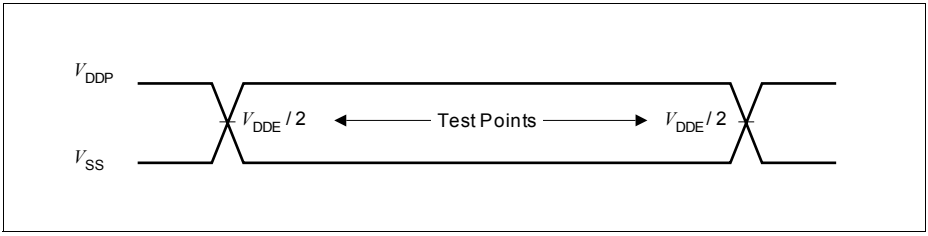



**Figure 39 Testing Waveform, Output Delay**

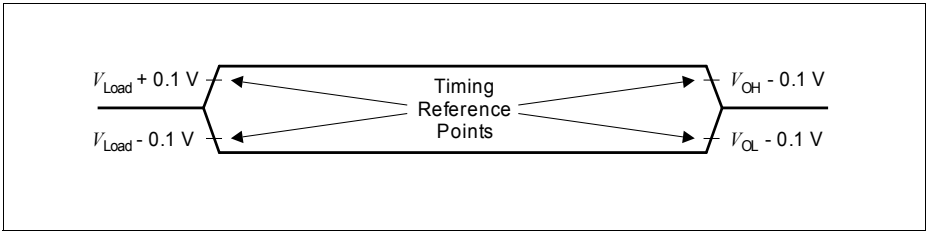



**Figure 40 Testing Waveform, Output High Impedance**

### 4.3.3 Power-on Reset and PLL Timing

**Table 42 Power-On Reset and PLL Timing (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Pad operating voltage | $V_{PAD}$ CC | 2.3 | – | – | V | |
| On-Chip Oscillator start-up time | $t_{OSCST}$ CC | – | – | 500 | ns | |
| Flash initialization time | $t_{FINIT}$ CC | – | 160 | – | µs | |
| $\overline{\text{RESET}}$ hold time[1] | $t_{RST}$ SR | – | 500 | – | µs | $V_{DDP}$ rise time (10% – 90%) ≤ 500µs |
| PLL lock-in in time | $t_{LOCK}$ CC | – | – | 200 | µs | |
| PLL accumulated jitter | $D_P$ | – | – | 0.7 | ns | 2) |

1) $\overline{\text{RESET}}$ signal has to be active (low) until $V_{DDC}$ has reached 90% of its maximum value (typ. 2.5V).

2) PLL lock at 80 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 40 and P = 1.

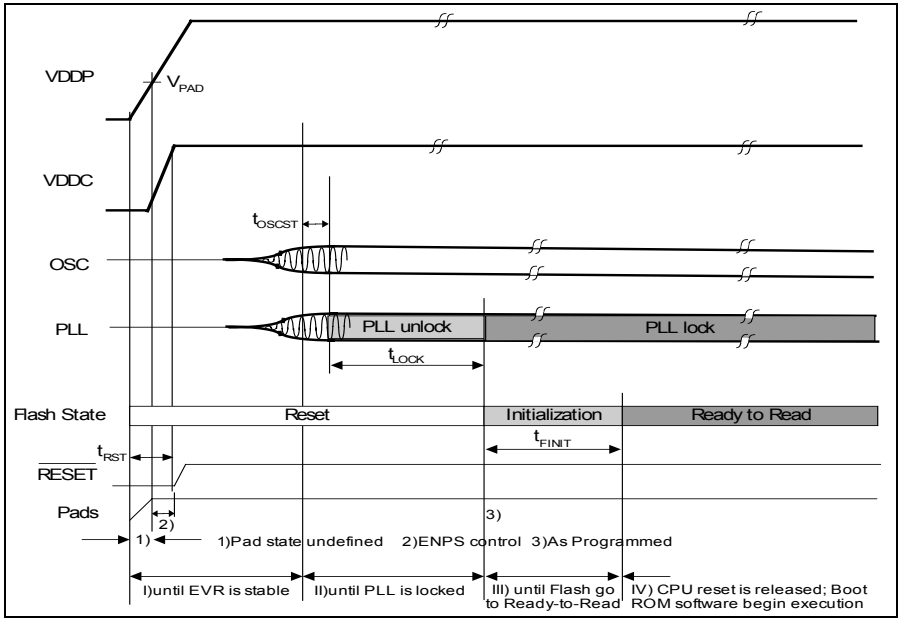



**Figure 42 Power-on Reset Timing**

**Table 45 JTAG Timing (Operating Conditions apply; $C_L$ = 50 pF)**

| Parameter | Symbol | | Limits | | Unit |
|---|---|---|---|---|---|
| | | | min | max | |
| TMS setup to TCK ↑ | $t_1$ | SR | 8.0 | – | ns |
| TMS hold to TCK ↑ | $t_2$ | SR | 5.0 | – | ns |
| TDI setup to TCK ↑ | $t_1$ | SR | 11.0 | – | ns |
| TDI hold to TCK ↑ | $t_2$ | SR | 6.0 | – | ns |
| TDO valid output from TCK ↓ | $t_3$ | CC | – | 23 | ns |
| TDO high impedance to valid output from TCK ↓ | $t_4$ | CC | – | 26 | ns |
| TDO valid output to high impedance from TCK ↓ | $t_5$ | CC | – | 18 | ns |

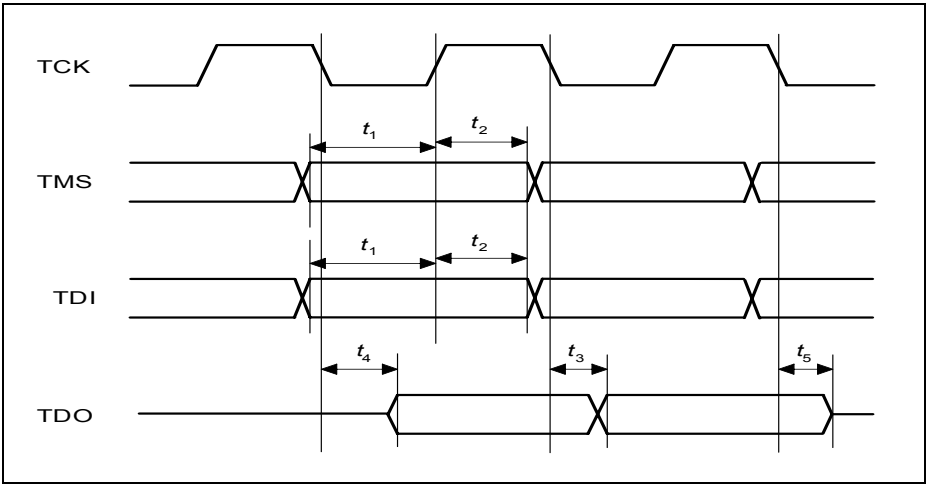
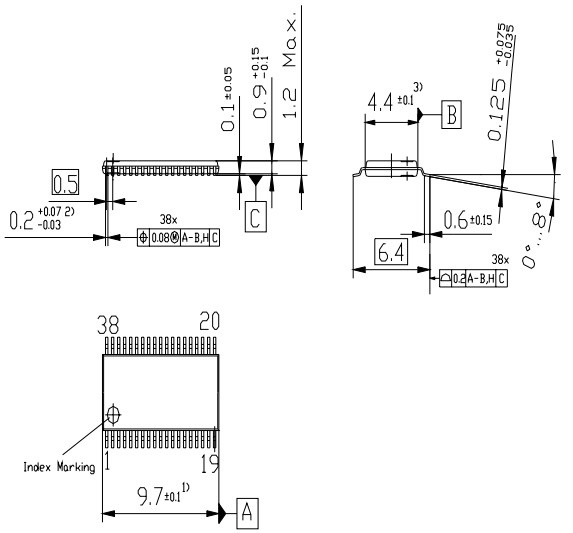



**Figure 44 JTAG Timing**

## 5.2 Package Outline




1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.15 MAX. PER SIDE

2) DOES NOT INCLUDE DAMBAR PROTRUSION OF 0.08 MAX. PER SIDE

3) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.25 MAX. PER SIDE

**Figure 46 PG-TSSOP-38-4 Package Outline**