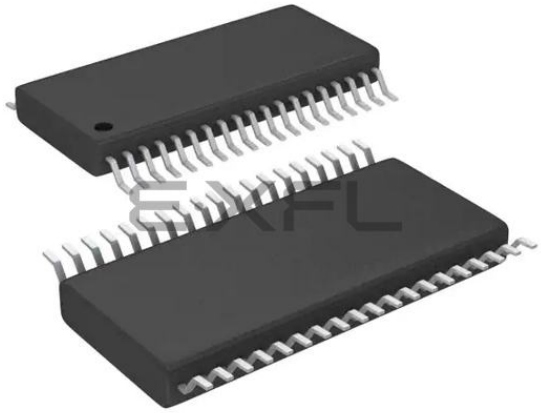

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	86MHz
Connectivity	LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	19
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc866l-2fri-bc

XC866 Variant Devices

The XC866 product family features devices with different configurations and program memory sizes, temperature and quality profiles (Automotive or Industrial), offering cost-effective solution for different application requirements.

The configuration of LIN BSL for XC866 devices are summarized in **Table 1**.

Table 1 Device Configuration for LIN BSL

Device Name	LIN BSL Support
XC866	No
XC866L	Yes

The list of XC866 devices and their differences are summarized in **Table 2**.

Table 2 Device Summary

Device Type	Device Name	Power Supply (V)	P-Flash Size (Kbytes)	D-Flash Size (Kbytes)	ROM Size (Kbytes)	Quality Profile[1)]
Flash[2)]	SAK-XC866*-4FRA	5.0	12	4	–	Automotive
	SAK-XC866*-4FRI	5.0	12	4	–	Industrial
	SAK-XC866*-2FRA	5.0	4	4	–	Automotive
	SAK-XC866*-2FRI	5.0	4	4	–	Industrial
	SAK-XC866*-1FRA	5.0	–	4	–	Automotive
	SAK-XC866*-1FRI	5.0	–	4	–	Industrial
	SAF-XC866*-4FRA	5.0	12	4	–	Automotive
	SAF-XC866*-4FRI	5.0	12	4	–	Industrial
	SAF-XC866*-2FRA	5.0	4	4	–	Automotive
	SAF-XC866*-2FRI	5.0	4	4	–	Industrial
	SAF-XC866*-1FRA	5.0	–	4	–	Automotive
	SAF-XC866*-1FRI	5.0	–	4	–	Industrial
	SAK-XC866*-4FRA 3V	3.3	12	4	–	Automotive
	SAK-XC866*-4FRI 3V	3.3	12	4	–	Industrial
	SAK-XC866*-2FRA 3V	3.3	4	4	–	Automotive
	SAK-XC866*-2FRI 3V	3.3	4	4	–	Industrial
	SAK-XC866*-1FRA 3V	3.3	–	4	–	Automotive

Table 2 Device Summary

	SAK-XC866*-1FRI 3V	3.3	–	4	–	Industrial
	SAF-XC866*-4FRA 3V	3.3	12	4	–	Automotive
	SAF-XC866*-4FRI 3V	3.3	12	4	–	Industrial
	SAF-XC866*-2FRA 3V	3.3	4	4	–	Automotive
	SAF-XC866*-2FRI 3V	3.3	4	4	–	Industrial
	SAF-XC866*-1FRA 3V	3.3	–	4	–	Automotive
	SAF-XC866*-1FRI 3V	3.3	–	4	–	Industrial
ROM	SAK-XC866*-4RRA	5.0	–	4	16	Automotive
	SAK-XC866*-4RRI	5.0	–	4	16	Industrial
	SAK-XC866*-2RRA	5.0	–	4	8	Automotive
	SAK-XC866*-2RRI	5.0	–	4	8	Industrial
	SAF-XC866*-4RRA	5.0	–	4	16	Automotive
	SAF-XC866*-4RRI	5.0	–	4	16	Industrial
	SAF-XC866*-2RRA	5.0	–	4	8	Automotive
	SAF-XC866*-2RRI	5.0	–	4	8	Industrial
	SAK-XC866*-4RRA 3V	3.3	–	4	16	Automotive
	SAK-XC866*-4RRI 3V	3.3	–	4	16	Industrial
	SAK-XC866*-2RRA 3V	3.3	–	4	8	Automotive
	SAK-XC866*-2RRI 3V	3.3	–	4	8	Industrial
	SAF-XC866*-4RRA 3V	3.3	–	4	16	Automotive
	SAF-XC866*-4RRI 3V	3.3	–	4	16	Industrial
	SAF-XC866*-2RRA 3V	3.3	–	4	8	Automotive
	SAF-XC866*-2RRI 3V	3.3	–	4	8	Industrial

1) Industrial is not for Automotive usage

2) The flash memory (P-Flash and D-Flash) can be used for code or data.

*Note: The asterisk (*) above denotes the device configuration letters from **Table 1**.*

2 General Device Information

2.1 Block Diagram

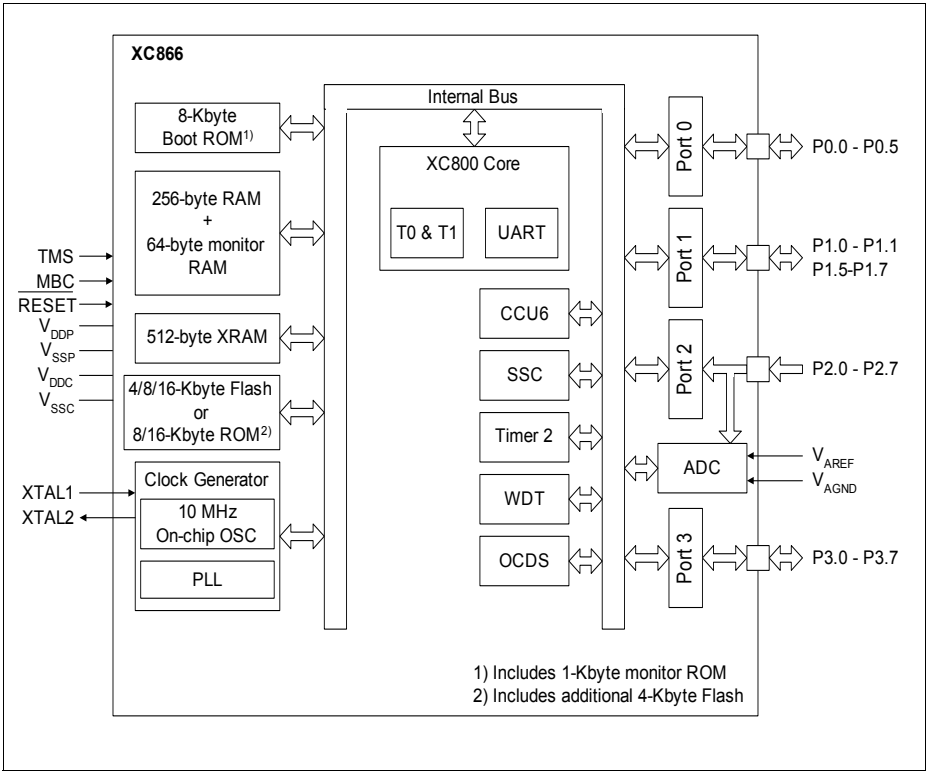

Figure 2 XC866 Block Diagram

2.3 Pin Configuration

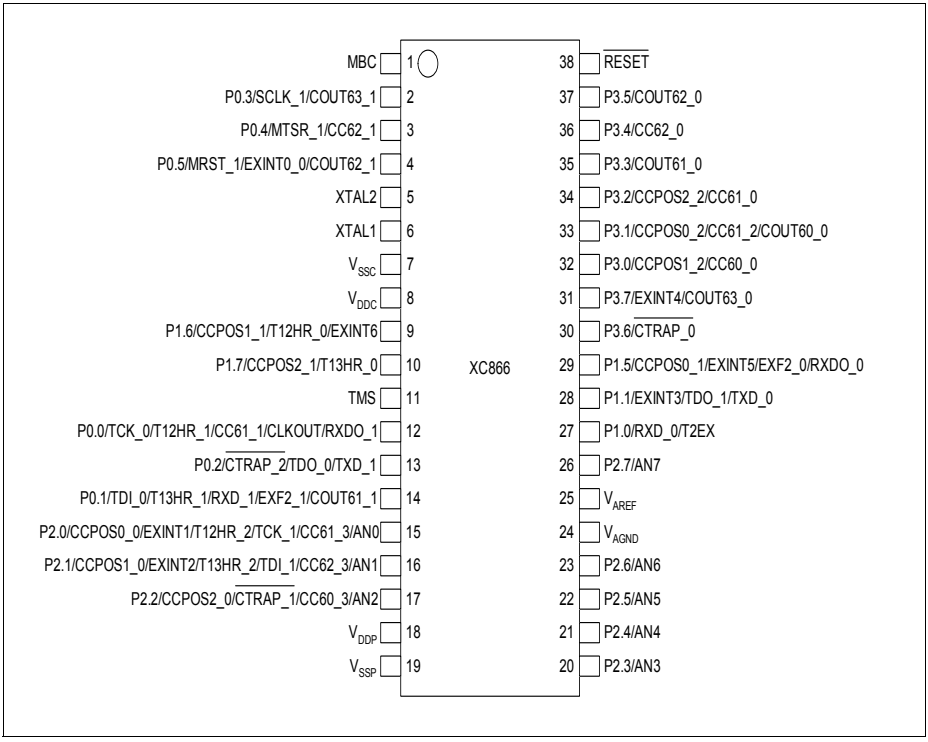

Figure 4 XC866 Pin Configuration, PG-TSSOP-38 Package (top view)

Field	Bits	Type	Description
OP	[7:6]	w	**Operation** 0X Manual page mode. The value of STNR is ignored and PAGE is directly written. 10 New page programming with automatic page saving. The value written to the bit positions of PAGE is stored. In parallel, the previous contents of PAGE are saved in the storage bit field STx indicated by STNR. 11 Automatic restore page action. The value written to the bit positions PAGE is ignored and instead, PAGE is overwritten by the contents of the storage bit field STx indicated by STNR.
0	3	r	**Reserved** Returns 0 if read; should be written with 0.

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$B2_H$	**PORT_PAGE** **Reset: 00_H** Page Register for PORT	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, Page 0										
80_H	**P0_DATA** **Reset: 00_H** P0 Data Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rwh	rwh	rwh	rwh	rwh	rwh
86_H	**P0_DIR** **Reset: 00_H** P0 Direction Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
90_H	**P1_DATA** **Reset: 00_H** P1 Data Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rwh	rwh	rwh	r			rwh	rwh
91_H	**P1_DIR** **Reset: 00_H** P1 Direction Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
$A0_H$	**P2_DATA** **Reset: 00_H** P2 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$A1_H$	**P2_DIR** **Reset: 00_H** P2 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B0_H$	**P3_DATA** **Reset: 00_H** P3 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$B1_H$	**P3_DIR** **Reset: 00_H** P3 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, Page 1										
80_H	**P0_PUDSEL** **Reset: FF_H** P0 Pull-Up/Pull-Down Select Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
86_H	**P0_PUDEN** **Reset: $C4_H$** P0 Pull-Up/Pull-Down Enable Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
90_H	**P1_PUDSEL** **Reset: FF_H** P1 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
91_H	**P1_PUDEN** **Reset: FF_H** P1 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
$A0_H$	**P2_PUDSEL** **Reset: FF_H** P2 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A1_H$	**P2_PUDEN** **Reset: 00_H** P2 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B0_H$	**P3_PUDSEL** **Reset: BF_H** P3 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B1_H$	**P3_PUDEN** **Reset: 40_H** P3 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, Page 2										
80_H	**P0_ALTSEL0** **Reset: 00_H** P0 Alternate Select 0 Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
86_H	**P0_ALTSEL1** **Reset: 00_H** P0 Alternate Select 1 Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
90_H	**P1_ALTSEL0** **Reset: 00_H** P1 Alternate Select 0 Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
91_H	**P1_ALTSEL1** **Reset: 00_H** P1 Alternate Select 1 Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
$B0_H$	**P3_ALTSEL0** **Reset: 00_H** P3 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CA_H	**ADC_RESR0L** **Reset: 00_H** Result Register 0 Low	Bit Field	RESULT[1:0]		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CB_H	**ADC_RESR0H** **Reset: 00_H** Result Register 0 High	Bit Field	RESULT[9:2]							
		Type	rh							
CC_H	**ADC_RESR1L** **Reset: 00_H** Result Register 1 Low	Bit Field	RESULT[1:0]		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CD_H	**ADC_RESR1H** **Reset: 00_H** Result Register 1 High	Bit Field	RESULT[9:2]							
		Type	rh							
CE_H	**ADC_RESR2L** **Reset: 00_H** Result Register 2 Low	Bit Field	RESULT[1:0]		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CF_H	**ADC_RESR2H** **Reset: 00_H** Result Register 2 High	Bit Field	RESULT[9:2]							
		Type	rh							
$D2_H$	**ADC_RESR3L** **Reset: 00_H** Result Register 3 Low	Bit Field	RESULT[1:0]		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
$D3_H$	**ADC_RESR3H** **Reset: 00_H** Result Register 3 High	Bit Field	RESULT[9:2]							
		Type	rh							
RMAP = 0, Page 3										
CA_H	**ADC_RESRA0L** **Reset: 00_H** Result Register 0, View A Low	Bit Field	RESULT[2:0]			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CB_H	**ADC_RESRA0H** **Reset: 00_H** Result Register 0, View A High	Bit Field	RESULT[10:3]							
		Type	rh							
CC_H	**ADC_RESRA1L** **Reset: 00_H** Result Register 1, View A Low	Bit Field	RESULT[2:0]			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CD_H	**ADC_RESRA1H** **Reset: 00_H** Result Register 1, View A High	Bit Field	RESULT[10:3]							
		Type	rh							
CE_H	**ADC_RESRA2L** **Reset: 00_H** Result Register 2, View A Low	Bit Field	RESULT[2:0]			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CF_H	**ADC_RESRA2H** **Reset: 00_H** Result Register 2, View A High	Bit Field	RESULT[10:3]							
		Type	rh							
$D2_H$	**ADC_RESRA3L** **Reset: 00_H** Result Register 3, View A Low	Bit Field	RESULT[2:0]			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
$D3_H$	**ADC_RESRA3H** **Reset: 00_H** Result Register 3, View A High	Bit Field	RESULT[10:3]							
		Type	rh							
RMAP = 0, Page 4										
CA_H	**ADC_RCR0** **Reset: 00_H** Result Control Register 0	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CB_H	**ADC_RCR1** **Reset: 00_H** Result Control Register 1	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CC_H	**ADC_RCR2** **Reset: 00_H** Result Control Register 2	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CD_H	**ADC_RCR3** **Reset: 00_H** Result Control Register 3	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CE_H	**ADC_VFCR** **Reset: 00_H** Valid Flag Clear Register	Bit Field	0				VFC3	VFC2	VFC1	VFC0
		Type	r				w	w	w	w
RMAP = 0, Page 5										

Table 14 SSC Register Overview

AB_H	**SSC_CONH** **Reset: 00_H** Control Register High *Programming Mode*	Bit Field	EN	MS	0	AREN	BEN	PEN	REN	TEN
		Type	rw	rw	r	rw	rw	rw	rw	rw
	Operating Mode	Bit Field	EN	MS	0	BSY	BE	PE	RE	TE
		Type	rw	rw	r	rh	rwh	rwh	rwh	rwh
AC_H	**SSC_TBL** **Reset: 00_H** Transmitter Buffer Register Low	Bit Field	TB_VALUE							
		Type	rw							
AD_H	**SSC_RBL** **Reset: 00_H** Receiver Buffer Register Low	Bit Field	RB_VALUE							
		Type	rh							
AE_H	**SSC_BRL** **Reset: 00_H** Baudrate Timer Reload Register Low	Bit Field	BR_VALUE[7:0]							
		Type	rw							
AF_H	**SSC_BRH** **Reset: 00_H** Baudrate Timer Reload Register High	Bit Field	BR_VALUE[15:8]							
		Type	rw							

The OCDS SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 15 OCDS Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$E9_H$	**MMCR2** **Reset: $0U_H$** Monitor Mode Control Register 2	Bit Field	EXBC_P	EXBC	MBCON_P	MBCON	MMEP_P	MMEP	MMODE	JENA
		Type	w	rw	w	rwh	w	rwh	rh	rh
$F1_H$	**MMCR** **Reset: 00_H** Monitor Mode Control Register	Bit Field	MEXIT_P	MEXIT	MSTEP_P	MSTEP	MRAMS_P	MRAMS	TRF	RRF
		Type	w	rwh	w	rw	w	rwh	rh	rh
$F2_H$	**MMSR** **Reset: 00_H** Monitor Mode Status Register	Bit Field	MBCAM	MBCIN	EXBF	SWBF	HWB3F	HWB2F	HWB1F	HWB0F
		Type	rw	rh	rwh	rwh	rwh	rwh	rwh	rwh
$F3_H$	**MMBPCR** **Reset: 00_H** BreakPoints Control Register	Bit Field	SWBC	HWB3C		HWB2C		HWB1C	HWB0C	
		Type	rw	rw		rw		rw	rw	
$F4_H$	**MMICR** **Reset: 00_H** Monitor Mode Interrupt Control Register	Bit Field	DVECT	DRETR	0		MMUIE_P	MMUIE	RRIE_P	RRIE
		Type	rwh	rwh	r		w	rw	w	rw
$F5_H$	**MMDR** **Reset: 00_H** Monitor Mode Data Register *Receive*	Bit Field	MMRR							
		Type	rh							
	Transmit	Bit Field	MMTR							
		Type	w							
$F6_H$	**HWBPSR** **Reset: 00_H** Hardware Breakpoints Select Register	Bit Field	0			BPSEL_P	BPSEL			
		Type	r			w	rw			
$F7_H$	**HWBPDR** **Reset: 00_H** Hardware Breakpoints Data Register	Bit Field	HWBPxx							
		Type	rw							

3.3 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 2.5 V supply from the Embedded Voltage Regulator (EVR) and does not require additional programming or erasing voltage. The sectorization of the Flash memory allows each sector to be erased independently.

Features

- In-System Programming (ISP) via UART
- In-Application Programming (IAP)
- Error Correction Code (ECC) for dynamic correction of single-bit errors
- Background program and erase operations for CPU load minimization
- Support for aborting erase operation
- Minimum program width[1] of 32-byte for D-Flash and 32-byte for P-Flash
- 1-sector minimum erase width
- 1-byte read access
- Flash is delivered in erased state (read all zeros)
- Operating supply voltage: 2.5 V ± 7.5 %
- Read access time: 3 × t_{CCLK} = 112.5 ns[2]
- Program time: 209440 / f_{SYS} = 2.6 ms[3]
- Erase time: 8175360 / f_{SYS} = 102 ms[3]

1) P-Flash: 32-byte wordline can only be programmed once, i.e., one gate disturb allowed.
D-Flash: 32-byte wordline can be programmed twice, i.e., two gate disturbs allowed.

2) f_{sys} = 80 MHz ± 7.5% (f_{CCLK} = 26.7 MHz ± 7.5 %) is the maximum frequency range for Flash read access.

3) f_{sys} = 80 MHz ± 7.5% is the only frequency range for Flash programming and erasing. f_{sysmin} is used for obtaining the worst case timing.

Table 16 shows the Flash data retention and endurance targets.

Table 16 Flash Data Retention and Endurance (Operating Conditions apply)

Retention	Endurance[1)]	Size	Remarks
Program Flash			
20 years	1,000 cycles	up to 16 Kbytes[2)]	for 16-Kbyte Variant
20 years	1,000 cycles	up to 8 Kbytes[2)]	for 8-Kbyte Variant
20 years	1,000 cycles	up to 4 Kbytes[2)]	for 4-Kbyte Variant
Data Flash			
20 years	1,000 cycles	4 Kbytes	
5 years	10,000 cycles	1 Kbyte	
2 years	70,000 cycles	512 bytes	
2 years	100,000 cycles	128 bytes	

1) One cycle refers to the programming of all wordlines in a sector and erasing of sector. The Flash endurance data specified in **Table 16** is valid only if the following conditions are fulfilled:
- the maximum number of erase cycles per Flash sector must not exceed 100,000 cycles.
- the maximum number of erase cycles per Flash bank must not exceed 300,000 cycles.
- the maximum number of program cycles per Flash bank must not exceed 2,500,000 cycles.

2) If no Flash is used for data, the Program Flash size can be up to the maximum Flash size available in the device variant. Having more Data Flash will mean less Flash is available for Program Flash.

3.3.1 Flash Bank Sectorization

The XC866 product family offers four Flash devices with either 8 Kbytes or 16 Kbytes of embedded Flash memory. These Flash memory sizes are made up of two or four 4-Kbyte Flash banks, respectively. Each Flash device consists of Program Flash (P-Flash) bank(s) and a single Data Flash (D-Flash) bank with different sectorization shown in **Figure 11**. Both types can be used for code and data storage. The label “Data” neither implies that the D-Flash is mapped to the data memory region, nor that it can only be used for data storage. It is used to distinguish the different Flash bank sectorizations. The XC866 ROM devices offer a single 4-Kbyte D-Flash bank.

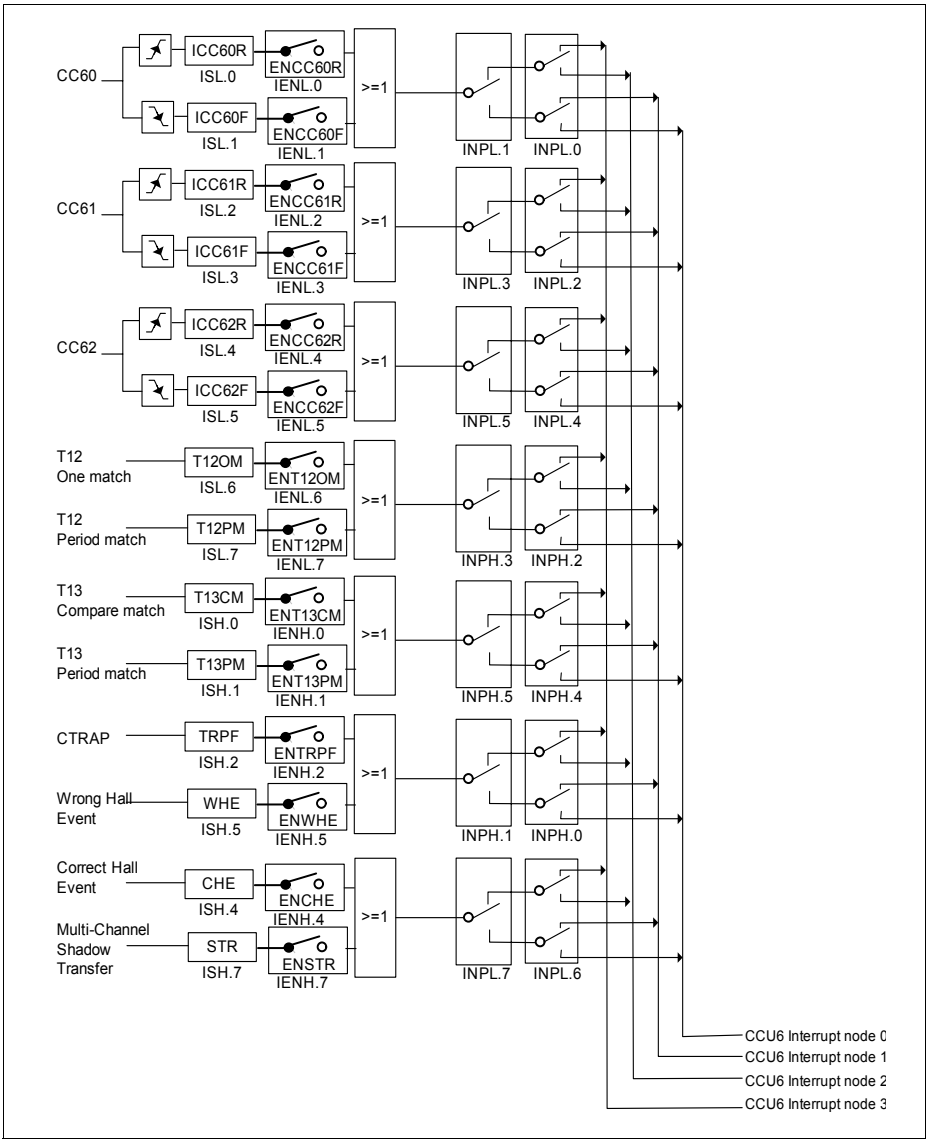

Figure 17 Interrupt Request Sources (Part 4)

3.4.2 Interrupt Source and Vector

Each interrupt source has an associated interrupt vector address. This vector is accessed to service the corresponding interrupt source request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC866 interrupt sources to the interrupt vector addresses and the corresponding interrupt source enable bits are summarized in **Table 17**.

Table 17 Interrupt Vector Addresses

Interrupt Source	Vector Address	Assignment for XC866	Enable Bit	SFR
NMI	0073_H	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		Flash NMI	NMIFLASH	
		VDDC Prewarning NMI	NMIVDD	
		VDDP Prewarning NMI	NMIVDDP	
		Flash ECC NMI	NMIECC	
XINTR0	0003_H	External Interrupt 0	EX0	IEN0
XINTR1	$000B_H$	Timer 0	ET0	
XINTR2	0013_H	External Interrupt 1	EX1	
XINTR3	$001B_H$	Timer 1	ET1	
XINTR4	0023_H	UART	ES	
XINTR5	$002B_H$	T2	ET2	
		Fractional Divider (Normal Divider Overflow)		
		LIN		

Table 17 Interrupt Vector Addresses (cont'd)

XINTR6	0033_H	ADC	EADC	IEN1
XINTR7	$003B_H$	SSC	ESSC	
XINTR8	0043_H	External Interrupt 2	EX2	
XINTR9	$004B_H$	External Interrupt 3	EXM	
		External Interrupt 4		
		External Interrupt 5		
		External Interrupt 6		
XINTR10	0053_H	CCU6 INP0	ECCIP0	
XINTR11	$005B_H$	CCU6 INP1	ECCIP1	
XINTR12	0063_H	CCU6 INP2	ECCIP2	
XINTR13	$006B_H$	CCU6 INP3	ECCIP3	

3.10 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC866 system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC866 will be aborted in a user-specified time period. In debug mode, the WDT is suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

Features:

- 16-bit Watchdog Timer
- Programmable reload value for upper 8 bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$
- Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access. **Figure 27** shows the block diagram of the WDT unit.

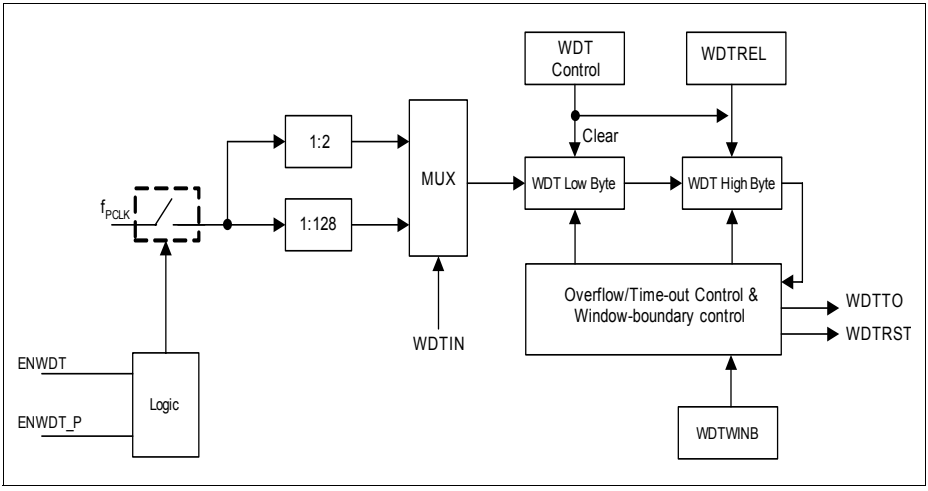

Figure 27 WDT Block Diagram

If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert WDTTO) and the reset prewarning is entered. The prewarning period lasts for 30_H count, after which the system is reset (assert WDTRST).

The WDT has a “programmable window boundary” which disallows any refresh during the WDT’s count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from 0000_H to the value obtained from the concatenation of WDTWINB and 00_H.

After being serviced, the WDT continues counting up from the value (<WDTREL> * 2^8). The time period for an overflow of the WDT is programmable in two ways:

- the input frequency to the WDT can be selected to be either $f_{PCLK}/2$ or $f_{PCLK}/128$
- the reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, P_{WDT}, between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}}$$

If the Window-Boundary Refresh feature of the WDT is enabled, the period P_{WDT} between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see **Figure 28**. This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB should not be smaller than WDTREL.

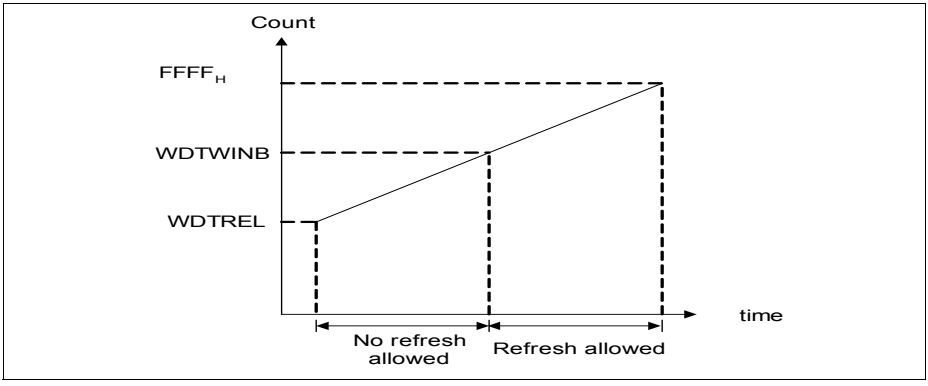

Figure 28 WDT Timing Diagram

3.14 High-Speed Synchronous Serial Interface

The High-Speed Synchronous Serial Interface (SSC) supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Features:

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format
  - Programmable number of data bits: 2 to 8 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)

Table 31 JTAG ID Summary

ROM	XC866L-4RR	1013 9083_H
	XC866-4RR	1013 9083_H
	XC866L-2RR	1013 9083_H
	XC866-2RR	1013 9083_H

3.20 Identification Register

The XC866 identity register is located at Page 1 of address $B3_H$.

ID
Identity Register **Reset Value: 0000 0010_B**

7	6	5	4	3	2	1	0
PRODID					VERID		
r					r		

Field	Bits	Type	Description
VERID	[2:0]	r	**Version ID** 010_B
PRODID	[7:3]	r	**Product ID** 00000_B

Table 36 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol	Limit Values			Unit	Test Conditions/ Remarks
		min.	typ .	max.		
Switched capacitance at the analog voltage inputs	C_{AINSW} CC	–	5	7	pF	2)4)
Input resistance of the reference input	R_{AREF}CC	–	1	2	kΩ	2)
Input resistance of the selected analog channel	R_{AIN} CC	–	1	1.5	kΩ	2)

1) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V , V_{DDP} = 5.0 V.

2) Not subject to production test, verified by design/characterization.

3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

4) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than V_{AREF}/2.

4.3.3 Power-on Reset and PLL Timing

Table 42 Power-On Reset and PLL Timing (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Pad operating voltage	V_{PAD} CC	2.3	–	–	V	
On-Chip Oscillator start-up time	t_{OSCST} CC	–	–	500	ns	
Flash initialization time	t_{FINIT} CC	–	160	–	µs	
$\overline{RESET}$ hold time[1]	t_{RST} SR	–	500	–	µs	V_{DDP} rise time (10% – 90%) ≤ 500µs
PLL lock-in in time	t_{LOCK} CC	–	–	200	µs	
PLL accumulated jitter	D_P	–	–	0.7	ns	2)

1) $\overline{RESET}$ signal has to be active (low) until V_{DDC} has reached 90% of its maximum value (typ. 2.5V).

2) PLL lock at 80 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 40 and P = 1.

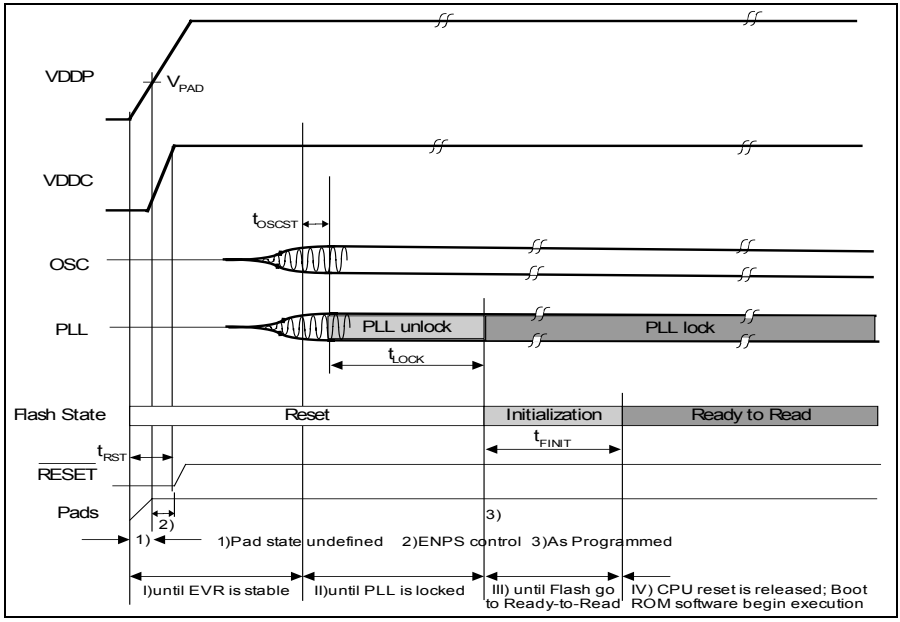

Figure 42 Power-on Reset Timing

Table 45 JTAG Timing (Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
TMS setup to TCK ↑	t_1	SR	8.0	–	ns
TMS hold to TCK ↑	t_2	SR	5.0	–	ns
TDI setup to TCK ↑	t_1	SR	11.0	–	ns
TDI hold to TCK ↑	t_2	SR	6.0	–	ns
TDO valid output from TCK ↓	t_3	CC	–	23	ns
TDO high impedance to valid output from TCK ↓	t_4	CC	–	26	ns
TDO valid output to high impedance from TCK ↓	t_5	CC	–	18	ns

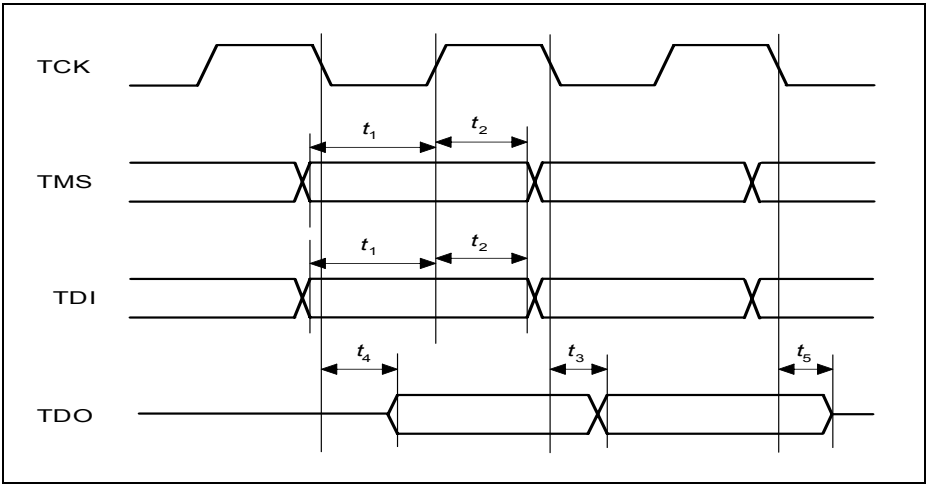

Figure 44 JTAG Timing