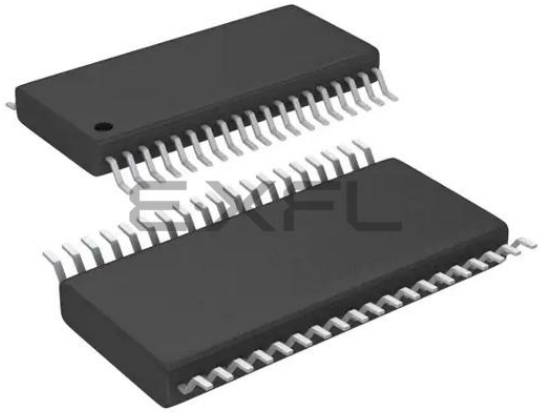

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	86MHz
Connectivity	LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc866l-4fri-be

XC866 Data Sheet
Revision History: 2007-10 V1.2

Previous Version: V 0.1, 2005-01
V1.0, 2006-02
V1.1, 2006-12

Page	Subjects (major changes since last revision)
3	Device summary table is updated for Flash 4-Kb and ROM variants.
13	Footnote is added to MBC pin; description of V_{DDP} pin is updated.
25	Section on bit protection scheme and access type of register bit field PASSWD.PASS are updated.
26	Access type of PAGE bits of all module page registers are corrected to rwh.
29	Access type of Px_DIR register bits are corrected to rwh
38	New bullet point on Flash delivery state is added to the feature list.
88	Digital power supply voltage are differentiated for 5V and 3.3V variants.
89	New parameters on XTAL1 hysteresis and Voltage on GPIO pins during V_{DDP} power-off condition are added.
104	Figure on Power-on reset timing is updated.

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Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery

For the available ordering codes for the XC866, please refer to your responsible sales representative or your local distributor.

As this document refers to all the derivatives, some descriptions may not apply to a specific product. For simplicity all versions are referred to by the term XC866 throughout this document.

2.2 Logic Symbol

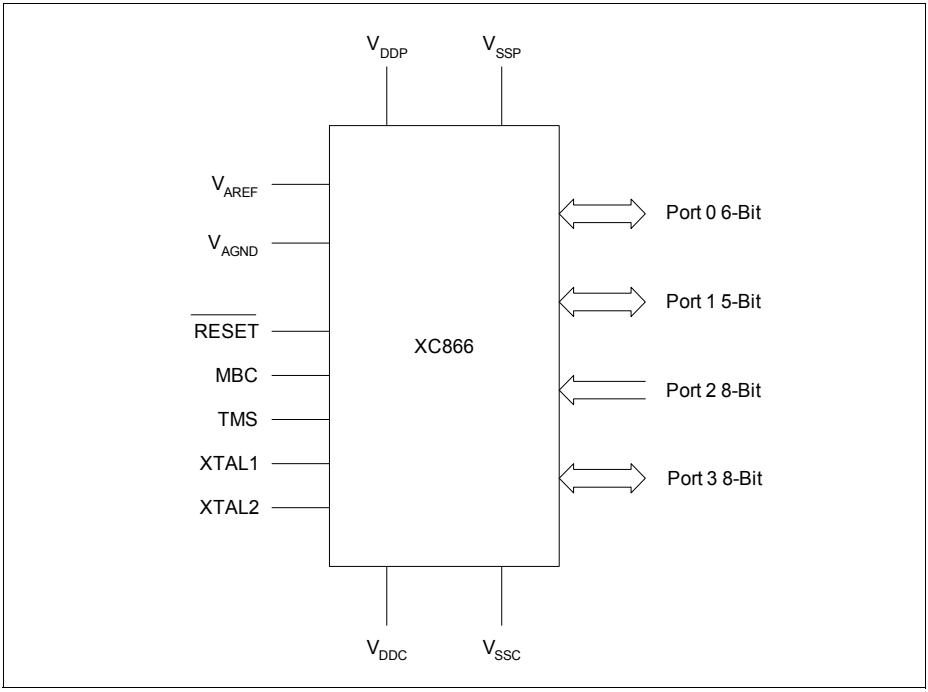


Figure 3 XC866 Logic Symbol

3.2 Memory Organization

The XC866 CPU operates in the following five address spaces:

- 8 Kbytes of Boot ROM program memory
- 256 bytes of internal RAM data memory
- 512 bytes of XRAM memory
  (XRAM can be read/written as program memory or external data memory)
- a 128-byte Special Function Register area
- 4/8/16 Kbytes of Flash program memory (Flash devices); or
  8/16 Kbytes of ROM program memory, with additional 4 Kbytes of Flash
  (ROM devices)

Figure 6 illustrates the memory address spaces of the XC866-4FR device.

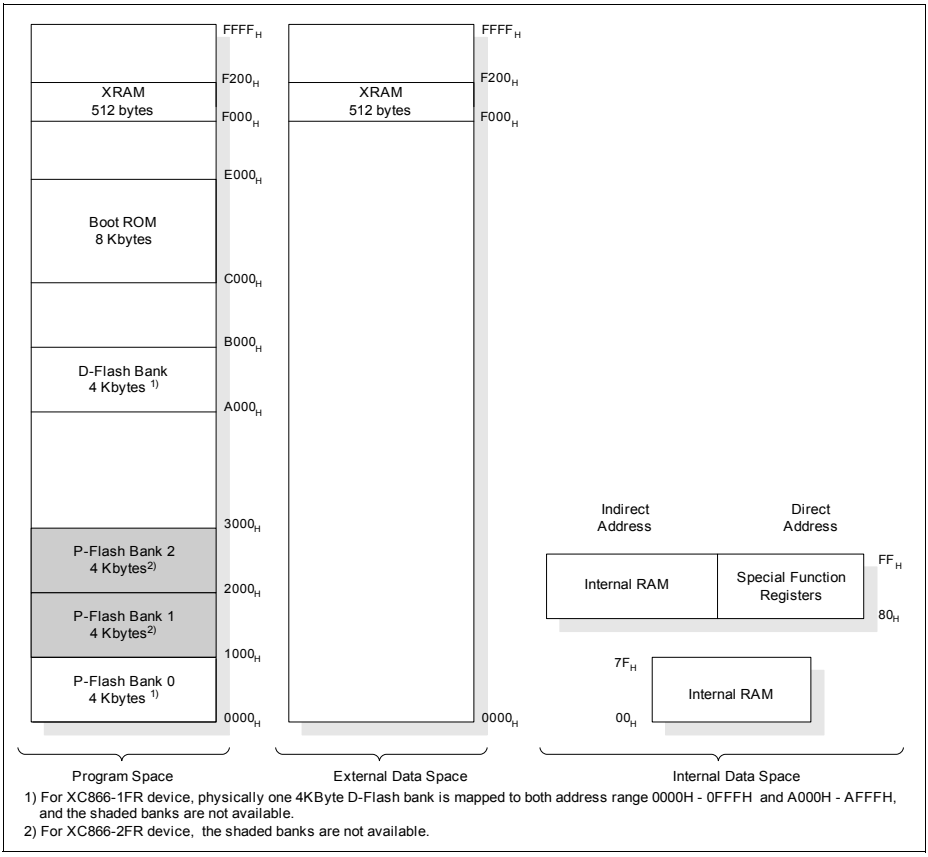
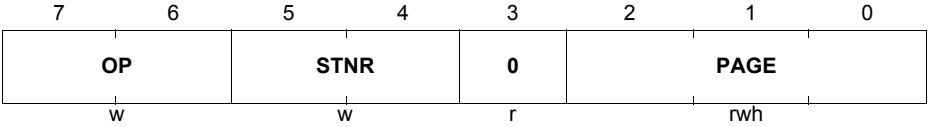


Figure 6 Memory Map of XC866 Flash Devices

The page register has the following definition:

MOD_PAGE
Page Register for module MOD **Reset Value: 00_H**



Field	Bits	Type	Description
PAGE	[2:0]	rwh	**Page Bits** When written, the value indicates the new page. When read, the value indicates the currently active page.
STNR	[5:4]	w	**Storage Number** This number indicates which storage bit field is the target of the operation defined by bit field OP. If OP = 10_B, the contents of PAGE are saved in STx before being overwritten with the new value. If OP = 11_B, the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored. 00 ST0 is selected. 01 ST1 is selected. 10 ST2 is selected. 11 ST3 is selected.

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CA_H	**ADC_CHINFR** **Reset: 00_H** Channel Interrupt Flag Register	Bit Field	CHINF 7	CHINF 6	CHINF 5	CHINF 4	CHINF 3	CHINF 2	CHINF 1	CHINF 0
		Type	rh	rh	rh	rh	rh	rh	rh	rh
CB_H	**ADC_CHINCR** **Reset: 00_H** Channel Interrupt Clear Register	Bit Field	CHINC 7	CHINC 6	CHINC 5	CHINC 4	CHINC 3	CHINC 2	CHINC 1	CHINC 0
		Type	w	w	w	w	w	w	w	w
CC_H	**ADC_CHINSR** **Reset: 00_H** Channel Interrupt Set Register	Bit Field	CHINS 7	CHINS 6	CHINS 5	CHINS 4	CHINS 3	CHINS 2	CHINS 1	CHINS 0
		Type	w	w	w	w	w	w	w	w
CD_H	**ADC_CHINPR** **Reset: 00_H** Channel Interrupt Node Pointer Register	Bit Field	CHINP 7	CHINP 6	CHINP 5	CHINP 4	CHINP 3	CHINP 2	CHINP 1	CHINP 0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
CE_H	**ADC_EVINFR** **Reset: 00_H** Event Interrupt Flag Register	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4	0		EVINF 1	EVINF 0
		Type	rh	rh	rh	rh	r		rh	rh
CF_H	**ADC_EVINCR** **Reset: 00_H** Event Interrupt Clear Flag Register	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4	0		EVINC 1	EVINC 0
		Type	w	w	w	w	r		w	w
$D2_H$	**ADC_EVINSR** **Reset: 00_H** Event Interrupt Set Flag Register	Bit Field	EVINS 7	EVINS 6	EVINS 5	EVINS 4	0		EVINS 1	EVINS 0
		Type	w	w	w	w	r		w	w
$D3_H$	**ADC_EVINPR** **Reset: 00_H** Event Interrupt Node Pointer Register	Bit Field	EVINP 7	EVINP 6	EVINP 5	EVINP 4	0		EVINP 1	EVINP 0
		Type	rw	rw	rw	rw	r		rw	rw
RMAP = 0, Page 6										
CA_H	**ADC_CRCR1** **Reset: 00_H** Conversion Request Control Register 1	Bit Field	CH7	CH6	CH5	CH4	0			
		Type	rwh	rwh	rwh	rwh	r			
CB_H	**ADC_CRPR1** **Reset: 00_H** Conversion Request Pending Register 1	Bit Field	CHP7	CHP6	CHP5	CHP4	0			
		Type	rwh	rwh	rwh	rwh	r			
CC_H	**ADC_CRMR1** **Reset: 00_H** Conversion Request Mode Register 1	Bit Field	Rsv	LDEV	CLR PND	SCAN	ENSI	ENTR	ENGT	
		Type	r	w	w	rw	rw	rw	rw	
CD_H	**ADC_QMR0** **Reset: 00_H** Queue Mode Register 0	Bit Field	CEV	TREV	FLUSH	CLRV	TRMD	ENTR	ENGT	
		Type	w	w	w	w	rw	rw	rw	
CE_H	**ADC_QSR0** **Reset: 20_H** Queue Status Register 0	Bit Field	Rsv	0	EMPTY	EV	0			
		Type	r	r	rh	rh	r			
CF_H	**ADC_Q0R0** **Reset: 00_H** Queue 0 Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
$D2_H$	**ADC_QBUR0** **Reset: 00_H** Queue Backup Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
$D2_H$	**ADC_QINR0** **Reset: 00_H** Queue Input Register 0	Bit Field	EXTR	ENSI	RF	0		REQCHNR		
		Type	w	w	w	r		w		

The Timer 2 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12 Timer 2 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$C0_H$	**T2_T2CON** **Reset: 00_H** Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN2	TR2	0	$\overline{CP/RL2}$
		Type	rwh	rwh	r		rw	rwh	r	rw

Table 13 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FD_H	**CCU6_CC61RH** **Reset: 00_H** Capture/Compare Register for Channel CC61 High	Bit Field	CC61VH							
		Type	rh							
FE_H	**CCU6_CC62RL** **Reset: 00_H** Capture/Compare Register for Channel CC62 Low	Bit Field	CC62VL							
		Type	rh							
FF_H	**CCU6_CC62RH** **Reset: 00_H** Capture/Compare Register for Channel CC62 High	Bit Field	CC62VH							
		Type	rh							
RMAP = 0, Page 2										
$9A_H$	**CCU6_T12MSELL** **Reset: 00_H** T12 Capture/Compare Mode Select Register Low	Bit Field	MSEL61				MSEL60			
		Type	rw				rw			
$9B_H$	**CCU6_T12MSELH** **Reset: 00_H** T12 Capture/Compare Mode Select Register High	Bit Field	DBYP	HSYNC			MSEL62			
		Type	rw	rw			rw			
$9C_H$	**CCU6_IENL** **Reset: 00_H** Capture/Compare Interrupt Enable Register Low	Bit Field	ENT12PM	ENT12OM	ENCC62F	ENCC62R	ENCC61F	ENCC61R	ENCC60F	ENCC60R
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$9D_H$	**CCU6_IENH** **Reset: 00_H** Capture/Compare Interrupt Enable Register High	Bit Field	ENSTR	EN IDLE	EN WHE	EN CHE	0	EN TRPF	ENT13PM	ENT13CM
		Type	rw	rw	rw	rw	r	rw	rw	rw
$9E_H$	**CCU6_INPL** **Reset: 40_H** Capture/Compare Interrupt Node Pointer Register Low	Bit Field	INPCHE		INPCC62		INPCC61		INPCC60	
		Type	rw		rw		rw		rw	
$9F_H$	**CCU6_INPH** **Reset: 39_H** Capture/Compare Interrupt Node Pointer Register High	Bit Field	0		INPT13		INPT12		INPERR	
		Type	r		rw		rw		rw	
$A4_H$	**CCU6_ISSL** **Reset: 00_H** Capture/Compare Interrupt Status Set Register Low	Bit Field	ST12PM	ST12OM	SCC62F	SCC62R	SCC61F	SCC61R	SCC60F	SCC60R
		Type	w	w	w	w	w	w	w	w
$A5_H$	**CCU6_ISSH** **Reset: 00_H** Capture/Compare Interrupt Status Set Register High	Bit Field	SSTR	SIDLE	SWHE	SCHE	SWHC	STRPF	ST13PM	ST13CM
		Type	w	w	w	w	w	w	w	w
$A6_H$	**CCU6_PSLR** **Reset: 00_H** Passive State Level Register	Bit Field	PSL63	0	PSL					
		Type	rwh	r	rwh					
$A7_H$	**CCU6_MCMCTR** **Reset: 00_H** Multi-Channel Mode Control Register	Bit Field	0		SWSYN		0	SWSEL		
		Type	r		rw		r	rw		
FA_H	**CCU6_TCTR2L** **Reset: 00_H** Timer Control Register 2 Low	Bit Field	0	T13TED		T13TEC			T13SSC	T12SSC
		Type	r	rw		rw			rw	rw
FB_H	**CCU6_TCTR2H** **Reset: 00_H** Timer Control Register 2 High	Bit Field	0				T13RSEL		T12RSEL	
		Type	r				rw		rw	
FC_H	**CCU6_MODCTRL** **Reset: 00_H** Modulation Control Register Low	Bit Field	MCMEN	0	T12MODEN					
		Type	rw	r	rw					
FD_H	**CCU6_MODCTRH** **Reset: 00_H** Modulation Control Register High	Bit Field	ECT13O	0	T13MODEN					
		Type	rw	r	rw					
FE_H	**CCU6_TRPCTRL** **Reset: 00_H** Trap Control Register Low	Bit Field	0					TRPM2	TRPM1	TRPM0
		Type	r					rw	rw	rw

Table 13 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FF_H	**CCU6_TRPCTRH** **Reset: 00_H** Trap Control Register High	Bit Field	TRPPEN	TRPEN13	TRPEN					
		Type	rw	rw	rw					
RMAP = 0, Page 3										
$9A_H$	**CCU6_MCMOUTL** **Reset: 00_H** Multi-Channel Mode Output Register Low	Bit Field	0	R	MCMP					
		Type	r	rh	rh					
$9B_H$	**CCU6_MCMOUTH** **Reset: 00_H** Multi-Channel Mode Output Register High	Bit Field	0		CURH			EXPH		
		Type	r		rh			rh		
$9C_H$	**CCU6_ISL** **Reset: 00_H** Capture/Compare Interrupt Status Register Low	Bit Field	T12PM	T12OM	ICC62F	ICC62R	ICC61F	ICC61R	ICC60F	ICC60R
		Type	rh	rh	rh	rh	rh	rh	rh	rh
$9D_H$	**CCU6_ISH** **Reset: 00_H** Capture/Compare Interrupt Status Register High	Bit Field	STR	IDLE	WHE	CHE	TRPS	TRPF	T13PM	T13CM
		Type	rh	rh	rh	rh	rh	rh	rh	rh
$9E_H$	**CCU6_PISEL0L** **Reset: 00_H** Port Input Select Register 0 Low	Bit Field	ISTRP		ISCC62		ISCC61		ISCC60	
		Type	rw		rw		rw		rw	
$9F_H$	**CCU6_PISEL0H** **Reset: 00_H** Port Input Select Register 0 High	Bit Field	IST12HR		ISPOS2		ISPOS1		ISPOS0	
		Type	rw		rw		rw		rw	
$A4_H$	**CCU6_PISEL2** **Reset: 00_H** Port Input Select Register 2	Bit Field	0						IST13HR	
		Type	r						rw	
FA_H	**CCU6_T12L** **Reset: 00_H** Timer T12 Counter Register Low	Bit Field	T12CVL							
		Type	rwh							
FB_H	**CCU6_T12H** **Reset: 00_H** Timer T12 Counter Register High	Bit Field	T12CVH							
		Type	rwh							
FC_H	**CCU6_T13L** **Reset: 00_H** Timer T13 Counter Register Low	Bit Field	T13CVL							
		Type	rwh							
FD_H	**CCU6_T13H** **Reset: 00_H** Timer T13 Counter Register High	Bit Field	T13CVH							
		Type	rwh							
FE_H	**CCU6_CMPSTATL** **Reset: 00_H** Compare State Register Low	Bit Field	0	CC63ST	CCPOS2	CCPOS1	CCPOS0	CC62ST	CC61ST	CC60ST
		Type	r	rh	rh	rh	rh	rh	rh	rh
FF_H	**CCU6_CMPSTATH** **Reset: 00_H** Compare State Register High	Bit Field	T13IM	COUT63PS	COUT62PS	CC62PS	COUT61PS	CC61PS	COUT60PS	CC60PS
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 14 SSC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$A9_H$	**SSC_PISEL** **Reset: 00_H** Port Input Select Register	Bit Field	0					CIS	SIS	MIS
		Type	r					rw	rw	rw
AA_H	**SSC_CONL** **Reset: 00_H** Control Register Low *Programming Mode*	Bit Field	LB	PO	PH	HB	BM			
		Type	rw	rw	rw	rw	rw			
	Operating Mode	Bit Field	0				BC			
		Type	r				rh			

3.3 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 2.5 V supply from the Embedded Voltage Regulator (EVR) and does not require additional programming or erasing voltage. The sectorization of the Flash memory allows each sector to be erased independently.

Features

- In-System Programming (ISP) via UART
- In-Application Programming (IAP)
- Error Correction Code (ECC) for dynamic correction of single-bit errors
- Background program and erase operations for CPU load minimization
- Support for aborting erase operation
- Minimum program width[1] of 32-byte for D-Flash and 32-byte for P-Flash
- 1-sector minimum erase width
- 1-byte read access
- Flash is delivered in erased state (read all zeros)
- Operating supply voltage: 2.5 V ± 7.5 %
- Read access time: 3 × t_{CCLK} = 112.5 ns[2]
- Program time: 209440 / f_{SYS} = 2.6 ms[3]
- Erase time: 8175360 / f_{SYS} = 102 ms[3]

1) P-Flash: 32-byte wordline can only be programmed once, i.e., one gate disturb allowed.
D-Flash: 32-byte wordline can be programmed twice, i.e., two gate disturbs allowed.

2) f_{sys} = 80 MHz ± 7.5% (f_{CCLK} = 26.7 MHz ± 7.5 %) is the maximum frequency range for Flash read access.

3) f_{sys} = 80 MHz ± 7.5% is the only frequency range for Flash programming and erasing. f_{sysmin} is used for obtaining the worst case timing.

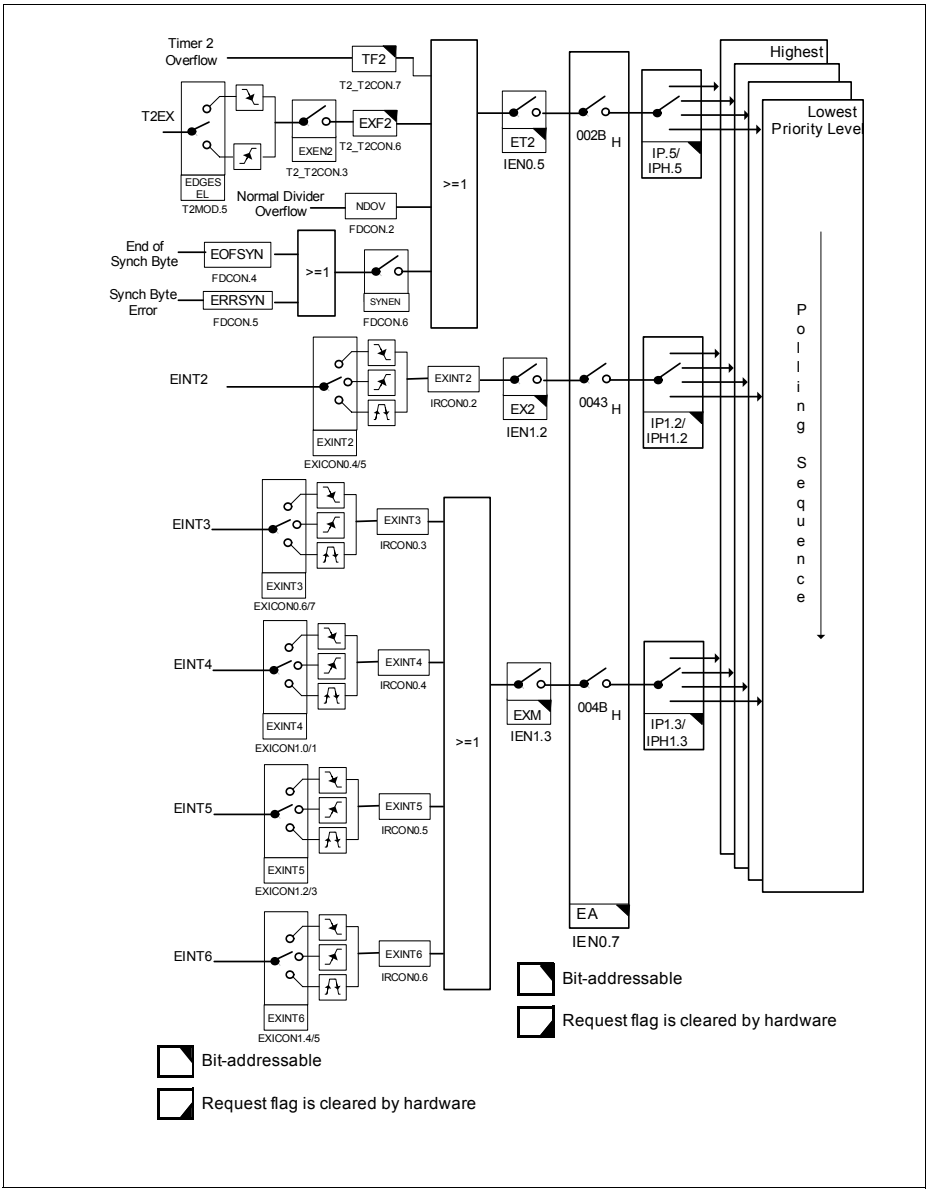


Figure 15 Interrupt Request Sources (Part 2)

115.2 kHz, using different module clock frequencies. The fractional divider is enabled (fractional divider mode) and the corresponding parameter settings are shown.

Table 27 Deviation Error for UART with Fractional Divider enabled

f_{PCLK}	Prescaling Factor (2^{BRPRE})	Reload Value (BR_VALUE + 1)	STEP	Deviation Error
26.67 MHz	1	10 (A_H)	177 ($B1_H$)	+0.03 %
13.33 MHz	1	7 (7_H)	248 ($F8_H$)	+0.11 %
6.67 MHz	1	3 (3_H)	212 ($D4_H$)	-0.16 %

3.18 Analog-to-Digital Converter

The XC866 includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at Port 2.

Features:

- Successive approximation
- 8-bit or 10-bit resolution
  (TUE of ± 1 LSB and ± 2 LSB, respectively)
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access
  (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter
  (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

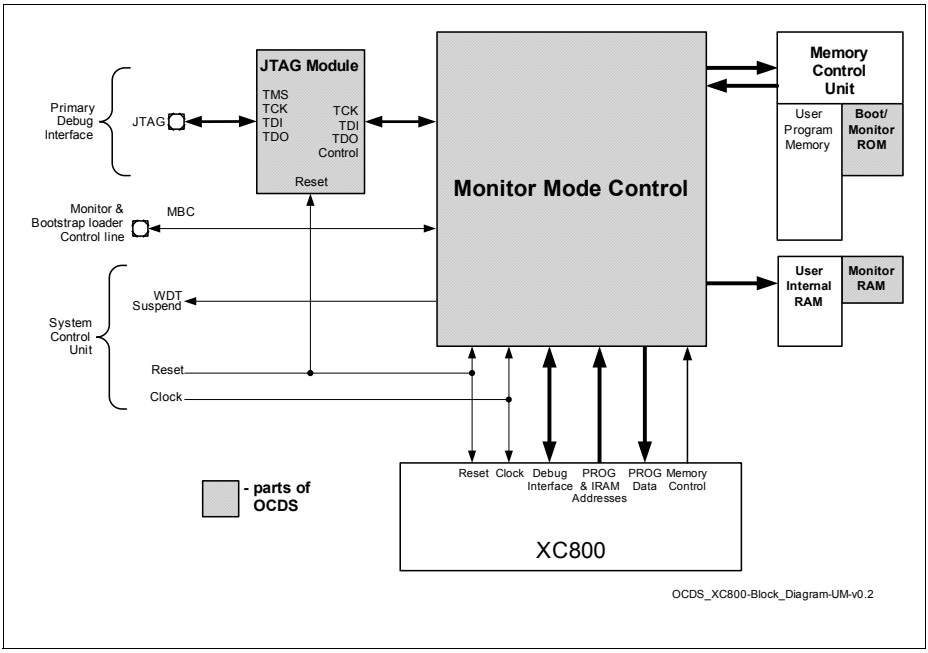


Figure 35 OCDS Block Diagram

3.19.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC866 devices are given in **Table 31**.

Table 31 JTAG ID Summary

Device Type	Device Name	JTAG ID
Flash	XC866L-4FR	1010 0083$_H$
	XC866-4FR	100F 5083$_H$
	XC866L-2FR	1010 2083$_H$
	XC866-2FR	1010 1083$_H$
	XC866L-1FR	1013 8083$_H$
	XC866-1FR	1013 8083$_H$

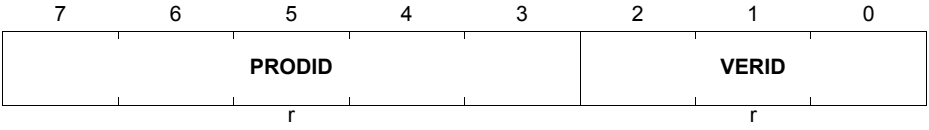
Table 31 JTAG ID Summary

ROM	XC866L-4RR	1013 9083$_H$
	XC866-4RR	1013 9083$_H$
	XC866L-2RR	1013 9083$_H$
	XC866-2RR	1013 9083$_H$

3.20 Identification Register

The XC866 identity register is located at Page 1 of address B3$_H$.

ID
Identity Register **Reset Value: 0000 0010$_B$**



Field	Bits	Type	Description
VERID	[2:0]	r	**Version ID** 010$_B$
PRODID	[7:3]	r	**Product ID** 00000$_B$

Table 34 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions Remarks
			min.	max.		
Input low voltage at XTAL1	V_{ILX}	SR	V_{SS} - 0.5	0.3 × V_{DDC}	V	
Input high voltage at XTAL1	V_{IHX}	SR	0.7 × V_{DDC}	V_{DDC} + 0.5	V	
Pull-up current	I_{PU}	SR	–	-10	µA	$V_{IH,min}$
			-150	–	µA	$V_{IL,max}$
Pull-down current	I_{PD}	SR	–	10	µA	$V_{IL,max}$
			150	–	µA	$V_{IH,min}$
Input leakage current[2)]	I_{OZ1}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125°C$, XC866-4FR and XC866-2FR
			-2.5	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125°C$, XC866-1FR and ROM device
Input current at XTAL1	I_{ILX}	CC	-10	10	µA	
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	SR	–	25	mA	3)
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	4)
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M	SR	–	15	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma\|I_M\|$	SR	–	60	mA	
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	80	mA	
Maximum current out of V_{SS}	I_{MVSS}	SR	–	80	mA	

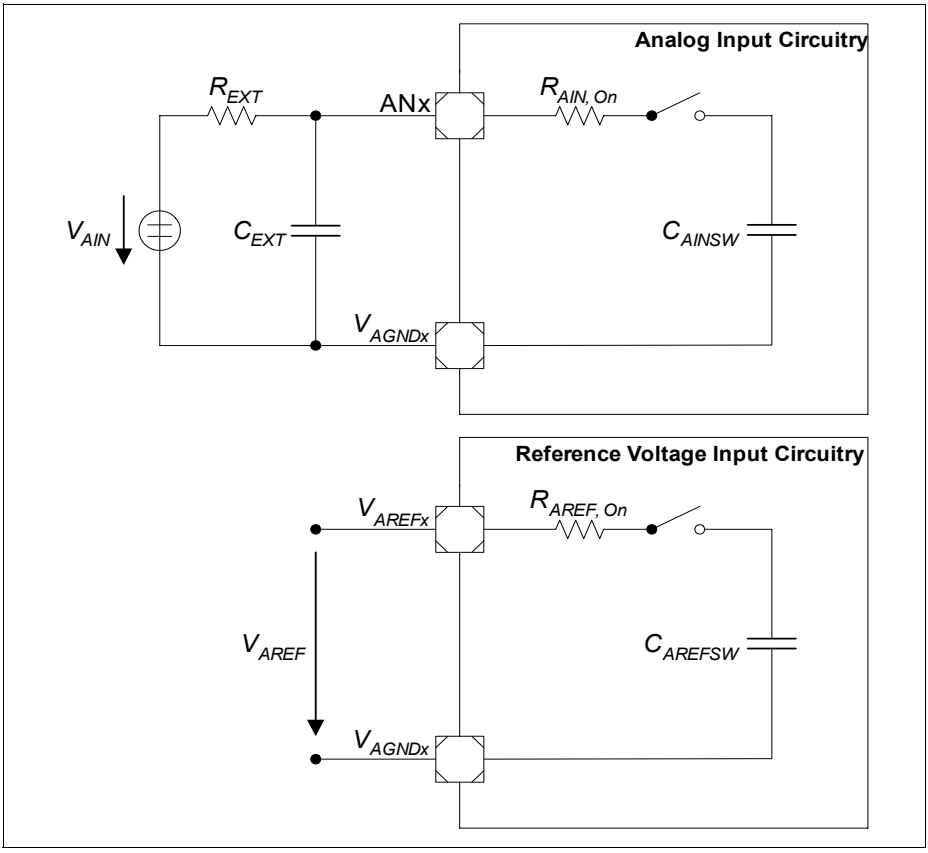


Figure 37 ADC Input Circuits

4.2.3.1 ADC Conversion Timing

Conversion time, $t_C = t_{ADC} \times (1 + r \times (3 + n + STC))$, where

r = CTC + 2 for CTC = 00_B, 01_B or 10_B,

r = 32 for CTC = 11_B,

CTC = Conversion Time Control (GLOBCTR.CTC),

STC = Sample Time Control (INPCR0.STC),

n = 8 or 10 (for 8-bit and 10-bit conversion respectively),

$t_{ADC} = 1 / f_{ADC}$

4.2.4 Power Supply Current

Table 37 Power Supply Current Parameters (Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit Values		Unit	Test Condition Remarks
		typ.[1]	max.[2]		
V_{DDP} = 5V Range					
Active Mode	I_{DDP}	22.6	24.5	mA	[3]
Idle Mode	I_{DDP}	17.2	19.7	mA	XC866-4FR, XC866-2FR [4]
		12.5	14	mA	XC866-1FR, ROM device[4]
Active Mode with slow-down enabled	I_{DDP}	7.2	8.2	mA	XC866-4FR, XC866-2FR [5]
		5.6	7.5	mA	XC866-1FR, ROM device[5]
Idle Mode with slow-down enabled	I_{DDP}	7.1	8	mA	XC866-4FR, XC866-2FR [6]
		5.1	7.2	mA	XC866-1FR, ROM device[6]

1) The typical I_{DDP} values are periodically measured at T_A = + 25 °C and V_{DDP} = 5.0 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = + 125 °C and V_{DDP} = 5.5 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 26.7 MHz(set by on-chip oscillator of 10 MHz and NDIV in PLL_CON to 0010_B), $\overline{RESET}$ = V_{DDP}, no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 26.7 MHz, $\overline{RESET}$ = V_{DDP} , no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 833 KHz by setting CLKREL in CMCON to 0101_B, $\overline{RESET}$ = V_{DDP}, no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 833 KHz by setting CLKREL in CMCON to 0101_B, $\overline{RESET}$ = V_{DDP}, no load on ports.

Table 40 Power Down Current (Operating Conditions apply; V_{DDP} = 3.3V range)

Parameter	Symbol	Limit Values		Unit	Test Condition Remarks
		typ.[1]	max.[2]		
V_{DDP} = 3.3V Range					
Power-Down Mode[3]	I_{PDP}	1	10	µA	T_A = + 25 °C.[4]
		-	30	µA	T_A = + 85 °C, XC866-4FR, XC866-2FR[4][5]
		-	35	µA	T_A = + 85 °C, XC866-1FR, ROM device[4][5]

1) The typical I_{PDP} values are measured at V_{DDP} = 3.3 V.

2) The maximum I_{PDP} values are measured at V_{DDP} = 3.6 V.

3) I_{PDP} (power-down mode) has a maximum value of 200 µA at T_A = + 125 °C.

4) I_{PDP} (power-down mode) is measured with: $\overline{\text{RESET}}$ = V_{DDP}, V_{AGND}= V_{SS}, RXD/INT0= V_{DDP}; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

5) Not subject to production test, verified by design/characterization.

4.3.2 Output Rise/Fall Times

Table 41 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
V_{DDP} = 5V Range					
Rise/fall times [1] [2]	t_R, t_F	–	10	ns	20 pF. [3]
V_{DDP} = 3.3V Range					
Rise/fall times [1] [2]	t_R, t_F	–	10	ns	20 pF. [4]

[1] Rise/Fall time measurements are taken with 10% - 90% of the pad supply.

[2] Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

[3] Additional rise/fall time valid for C_L = 20pF - 100pF @ 0.125 ns/pF.

[4] Additional rise/fall time valid for C_L = 20pF - 100pF @ 0.225 ns/pF.

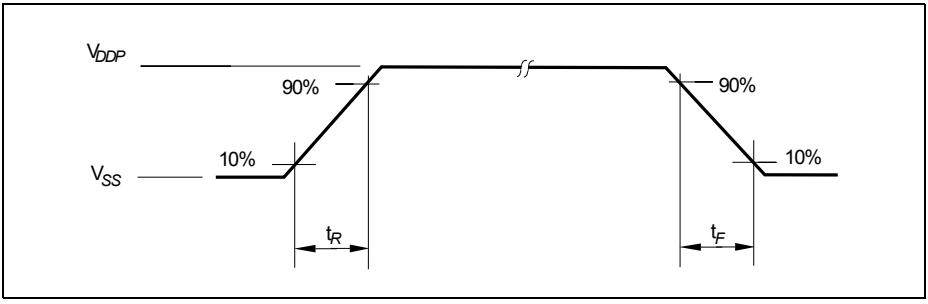


Figure 41 Rise/Fall Times Parameters

Table 45 JTAG Timing (Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
TMS setup to TCK ↑	t_1	SR	8.0	–	ns
TMS hold to TCK ↑	t_2	SR	5.0	–	ns
TDI setup to TCK ↑	t_1	SR	11.0	–	ns
TDI hold to TCK ↑	t_2	SR	6.0	–	ns
TDO valid output from TCK ↓	t_3	CC	–	23	ns
TDO high impedance to valid output from TCK ↓	t_4	CC	–	26	ns
TDO valid output to high impedance from TCK ↓	t_5	CC	–	18	ns

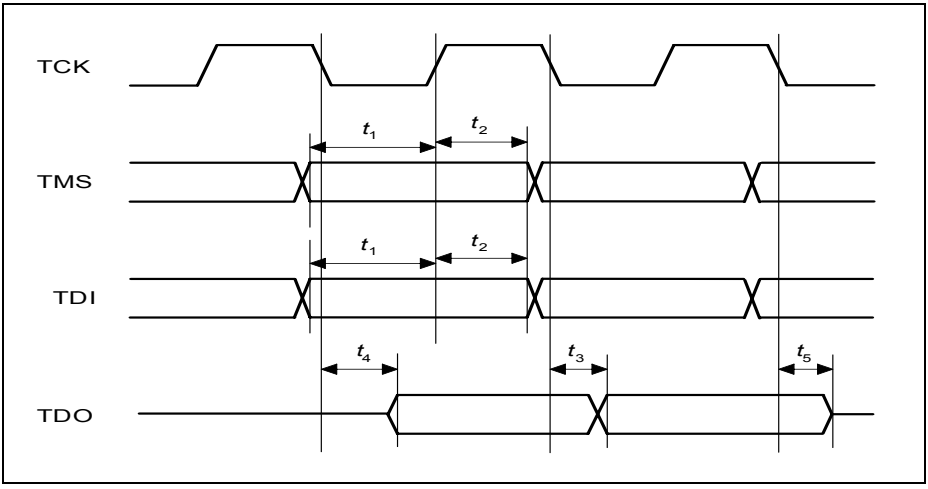


Figure 44 JTAG Timing