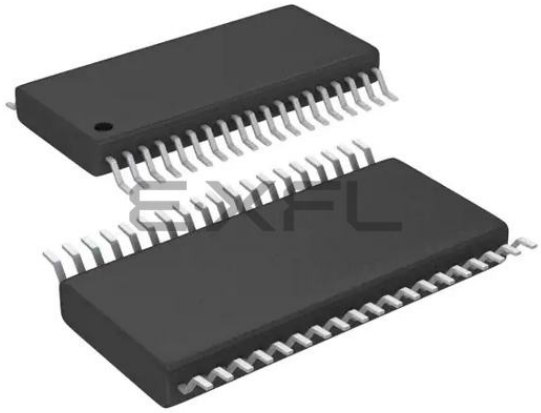

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | XC800 |
| Core Size | 8-Bit |
| Speed | 86MHz |
| Connectivity | SSI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 19 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 768 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 38-TFSOP (0.173", 4.40mm Width) |
| Supplier Device Package | PG-TSSOP-38 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xc8661friabkxuma1 |

## 2.2 Logic Symbol

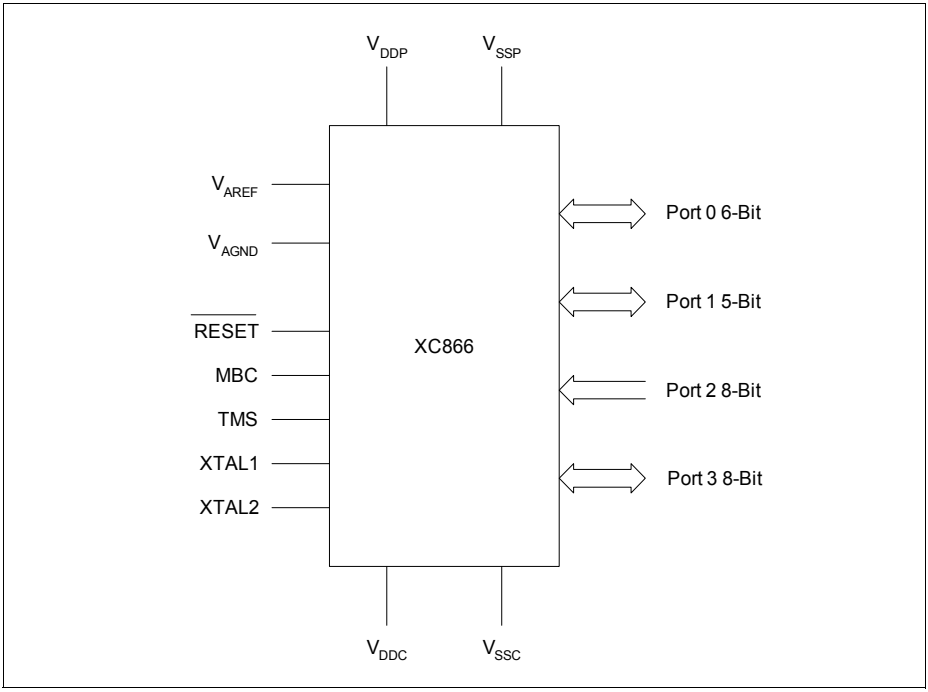



**Figure 3 XC866 Logic Symbol**

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|---|---|---|---|---|
| **P1** | | I/O | | **Port 1**<br>Port 1 is a 5-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, and the SSC. |
| P1.0 | 27 | | PU | RXD_0 UART Receive Data Input<br>T2EX Timer 2 External Trigger Input |
| P1.1 | 28 | | PU | EXINT3 External Interrupt Input 3<br>TDO_1 JTAG Serial Data Output<br>TXD_0 UART Transmit Data Output/ Clock Output |
| P1.5 | 29 | | PU | CCPOS0_1 CCU6 Hall Input 0<br>EXINT5 External Interrupt Input 5<br>EXF2_0 TImer 2 External Flag Output<br>RXDO_0 UART Transmit Data Output |
| P1.6 | 9 | | PU | CCPOS1_1 CCU6 Hall Input 1<br>T12HR_0 CCU6 Timer 12 Hardware Run Input<br>EXINT6 External Interrupt Input 6 |
| P1.7 | 10 | | PU | CCPOS2_1 CCU6 Hall Input 2<br>T13HR_0 CCU6 Timer 13 Hardware Run Input<br>P1.5 and P1.6 can be used as a software chip select output for the SSC. |

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|---|---|---|---|---|
| **P2** | | I | | **Port 2**<br>Port 2 is an 8-bit general purpose input-only port. It can be used as alternate functions for the digital inputs of the JTAG and CCU6. It is also used as the analog inputs for the ADC. |
| P2.0 | 15 | | Hi-Z | CCPOS0_0 CCU6 Hall Input 0<br>EXINT1 External Interrupt Input 1<br>T12HR_2 CCU6 Timer 12 Hardware Run Input<br>TCK_1 JTAG Clock Input<br>CC61_3 Input of Capture/Compare channel 1<br>AN0 Analog Input 0 |
| P2.1 | 16 | | Hi-Z | CCPOS1_0 CCU6 Hall Input 1<br>EXINT2 External Interrupt Input 2<br>T13HR_2 CCU6 Timer 13 Hardware Run Input<br>TDI_1 JTAG Serial Data Input<br>CC62_3 Input of Capture/Compare channel 2<br>AN1 Analog Input 1 |
| P2.2 | 17 | | Hi-Z | CCPOS2_0 CCU6 Hall Input 2<br>CTRAP_1 CCU6 Trap Input<br>CC60_3 Input of Capture/Compare channel 0<br>AN2 Analog Input 2 |
| P2.3 | 20 | | Hi-Z | AN3 Analog Input 3 |
| P2.4 | 21 | | Hi-Z | AN4 Analog Input 4 |
| P2.5 | 22 | | Hi-Z | AN5 Analog Input 5 |
| P2.6 | 23 | | Hi-Z | AN6 Analog Input 6 |
| P2.7 | 26 | | Hi-Z | AN7 Analog Input 7 |

# 3 Functional Description

## 3.1 Processor Architecture

The XC866 is based on a high-performance 8-bit Central Processing Unit (CPU) that is compatible with the standard 8051 processor. While the standard 8051 processor is designed around a 12-clock machine cycle, the XC866 CPU uses a 2-clock machine cycle. This allows fast access to ROM or RAM memories without wait state. Access to the Flash memory, however, requires an additional wait state (one machine cycle). The instruction set consists of 45% one-byte, 41% two-byte and 14% three-byte instructions.

The XC866 CPU provides a range of debugging features, including basic stop/start, single-step execution, breakpoint support and read/write access to the data memory, program memory and SFRs.

**Figure 5** shows the CPU functional blocks.

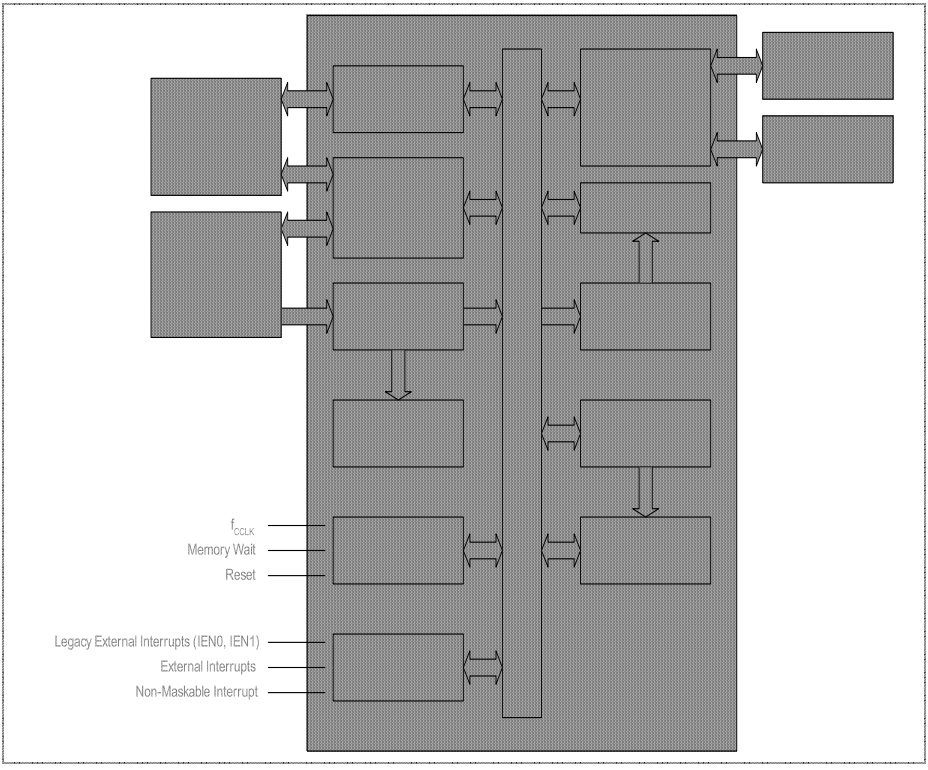



**Figure 5 CPU Block Diagram**

### 3.2.1 Memory Protection Strategy

The XC866 memory protection strategy includes:

- Read-out protection: The Flash Memory can be enabled for read-out protection and ROM memory is always protected.
- Program and erase protection: The Flash memory in all devices can be enabled for program and erase protection.

Flash memory protection is available in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in **Table 4**.

**Table 4 Flash Protection Modes**

| **Mode** | 0 | 1 |
|---|---|---|
| **Activation** | Program a valid password via BSL mode 6 | |
| **Selection** | MSB of password = 0 | MSB of password = 1 |
| **P-Flash contents can be read by** | Read instructions in the P-Flash | Read instructions in the P-Flash or D-Flash |
| **P-Flash program and erase** | Not possible | Not possible |
| **D-Flash contents can be read by** | Read instructions in any program memory | Read instructions in the P-Flash or D-Flash |
| **D-Flash program** | Possible | Not possible |
| **D-Flash erase** | Possible, on the condition that bit DFLASHEN in register MISC_CON is set to 1 prior to each erase operation | Not possible |

BSL mode 6, which is used for enabling Flash protection, can also be used for disabling Flash protection. Here, the programmed password must be provided by the user. A password match triggers an automatic erase of the read-protected Flash contents, see **Table 5** and **Table 6**, and the programmed password is erased. The Flash protection is then disabled upon the next reset.

**For XC866-2FR and XC866-4FR devices:**

The selection of protection type is summarized in **Table 5**.

### 3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range $80_H$ to $FF_H$. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

#### 3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range $80_H$ to $FF_H$, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 8**.

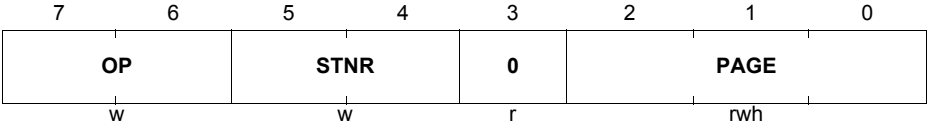
**SYSCON0**
**System Control Register 0** **Reset Value: $00_H$**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **0** | | | | | **1** | **0** | **RMAP** |
| r | | | | | rw | r | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RMAP** | 0 | rw | **Special Function Register Map Control**<br>0 The access to the standard SFR area is enabled.<br>1 The access to the mapped SFR area is enabled. |
| **1** | 2 | rw | **Reserved**<br>Returns the last value if read; should be written with 1. |
| **0** | 1,[7:3] | r | **Reserved**<br>Returns 0 if read; should be written with 0. |

The page register has the following definition:

**MOD_PAGE**
**Page Register for module MOD** **Reset Value: $00_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| **PAGE** | [2:0] | rwh | **Page Bits**<br>When written, the value indicates the new page.<br>When read, the value indicates the currently active page. |
| **STNR** | [5:4] | w | **Storage Number**<br>This number indicates which storage bit field is the target of the operation defined by bit field OP.<br>If OP = $10_B$,<br>the contents of PAGE are saved in STx before being overwritten with the new value.<br>If OP = $11_B$,<br>the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored.<br><br>00 ST0 is selected.<br>01 ST1 is selected.<br>10 ST2 is selected.<br>11 ST3 is selected. |

**Table 16** shows the Flash data retention and endurance targets.

**Table 16 Flash Data Retention and Endurance (Operating Conditions apply)**

| Retention | Endurance[1)] | Size | Remarks |
|---|---|---|---|
| **Program Flash** | | | |
| 20 years | 1,000 cycles | up to 16 Kbytes[2)] | for 16-Kbyte Variant |
| 20 years | 1,000 cycles | up to 8 Kbytes[2)] | for 8-Kbyte Variant |
| 20 years | 1,000 cycles | up to 4 Kbytes[2)] | for 4-Kbyte Variant |
| **Data Flash** | | | |
| 20 years | 1,000 cycles | 4 Kbytes | |
| 5 years | 10,000 cycles | 1 Kbyte | |
| 2 years | 70,000 cycles | 512 bytes | |
| 2 years | 100,000 cycles | 128 bytes | |

1) One cycle refers to the programming of all wordlines in a sector and erasing of sector. The Flash endurance data specified in **Table 16** is valid only if the following conditions are fulfilled:
- the maximum number of erase cycles per Flash sector must not exceed 100,000 cycles.
- the maximum number of erase cycles per Flash bank must not exceed 300,000 cycles.
- the maximum number of program cycles per Flash bank must not exceed 2,500,000 cycles.

2) If no Flash is used for data, the Program Flash size can be up to the maximum Flash size available in the device variant. Having more Data Flash will mean less Flash is available for Program Flash.

### 3.3.1 Flash Bank Sectorization

The XC866 product family offers four Flash devices with either 8 Kbytes or 16 Kbytes of embedded Flash memory. These Flash memory sizes are made up of two or four 4-Kbyte Flash banks, respectively. Each Flash device consists of Program Flash (P-Flash) bank(s) and a single Data Flash (D-Flash) bank with different sectorization shown in **Figure 11**. Both types can be used for code and data storage. The label “Data” neither implies that the D-Flash is mapped to the data memory region, nor that it can only be used for data storage. It is used to distinguish the different Flash bank sectorizations. The XC866 ROM devices offer a single 4-Kbyte D-Flash bank.

### 3.3.2 Flash Programming Width

For the P-Flash banks, a programmed wordline (WL) must be erased before it can be reprogrammed as the Flash cells can only withstand one gate disturb. This means that the entire sector containing the WL must be erased since it is impossible to erase a single WL.

For the D-Flash bank, the same WL can be programmed twice before erasing is required as the Flash cells are able to withstand two gate disturbs. Hence, it is possible to program the same WL, for example, with 16 bytes of data in two times (see **Figure 12**).

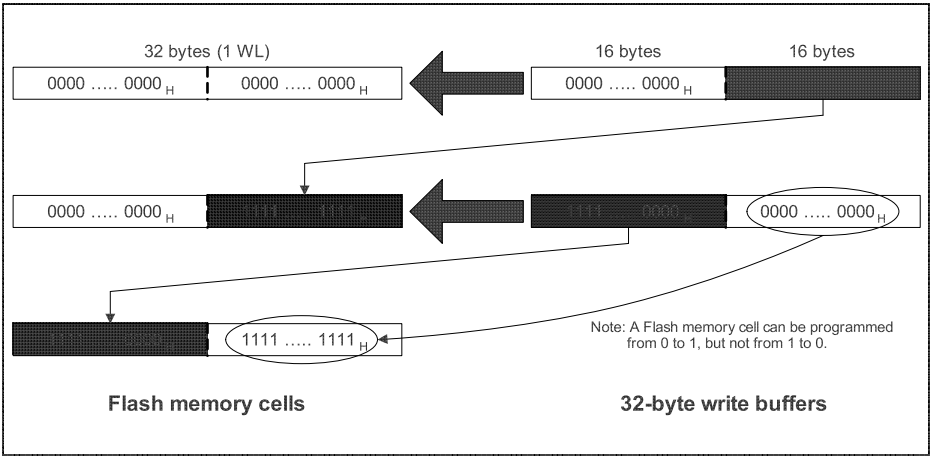



**Figure 12 D-Flash Programming**

*Note: When programming a D-Flash WL the second time, the previously programmed Flash memory cells (whether 0s or 1s) should be reprogrammed with 0s to retain its original contents and to prevent "over-programming".*

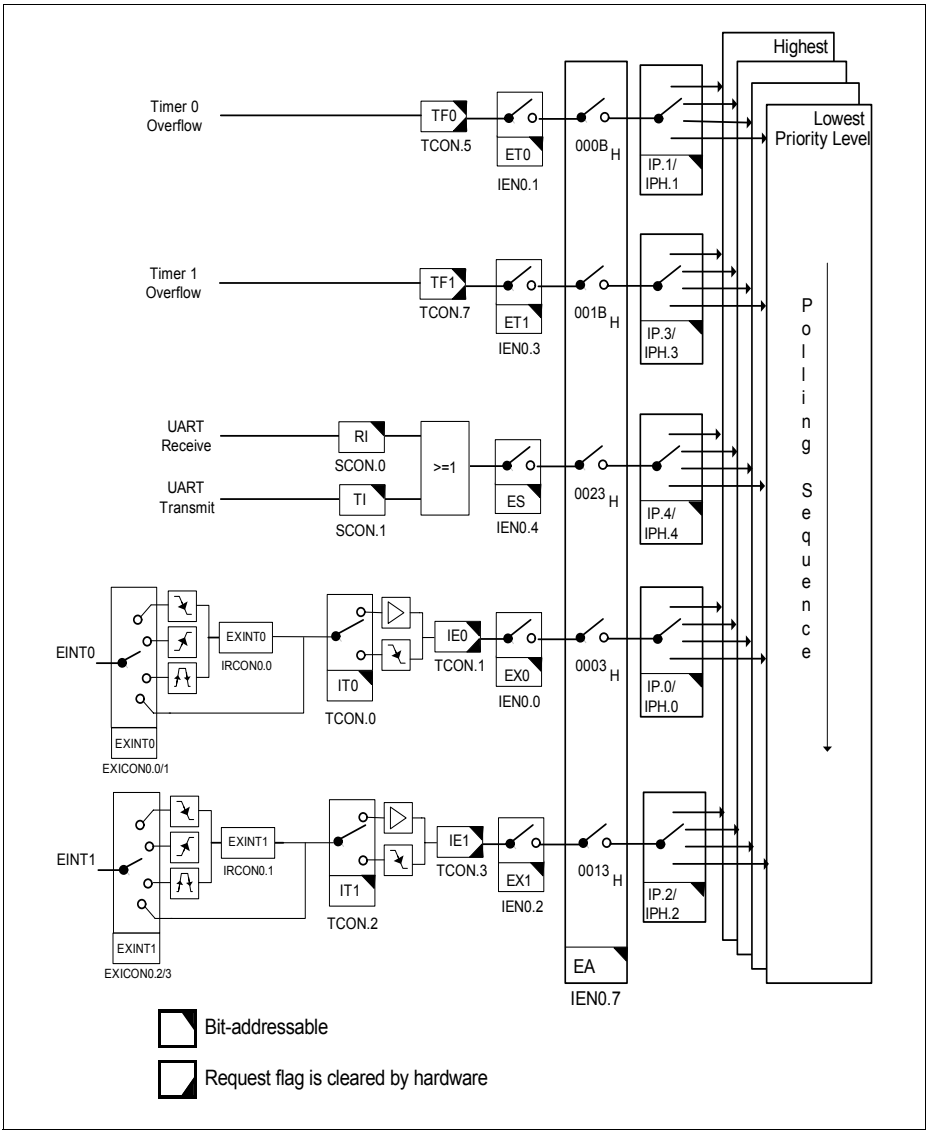



**Figure 14 Interrupt Request Sources (Part 1)**

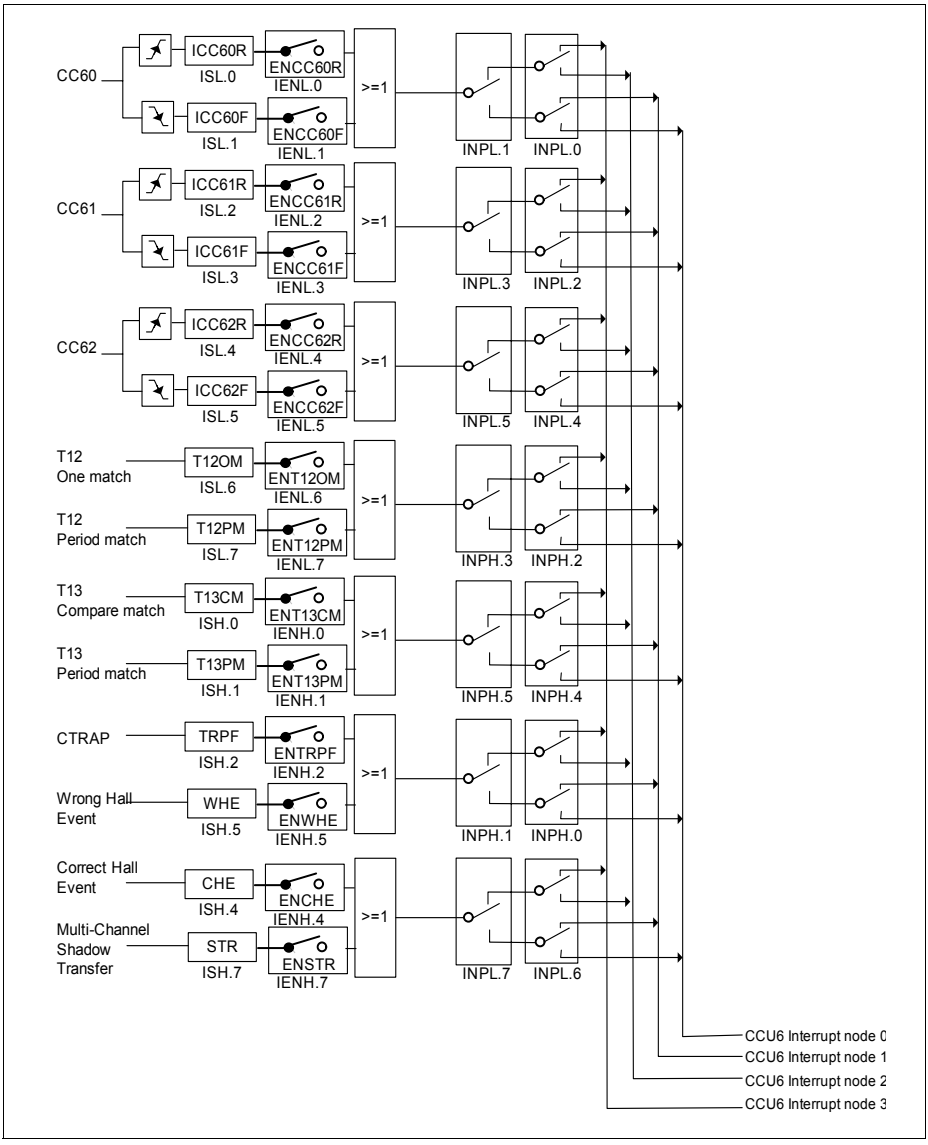



**Figure 17 Interrupt Request Sources (Part 4)**

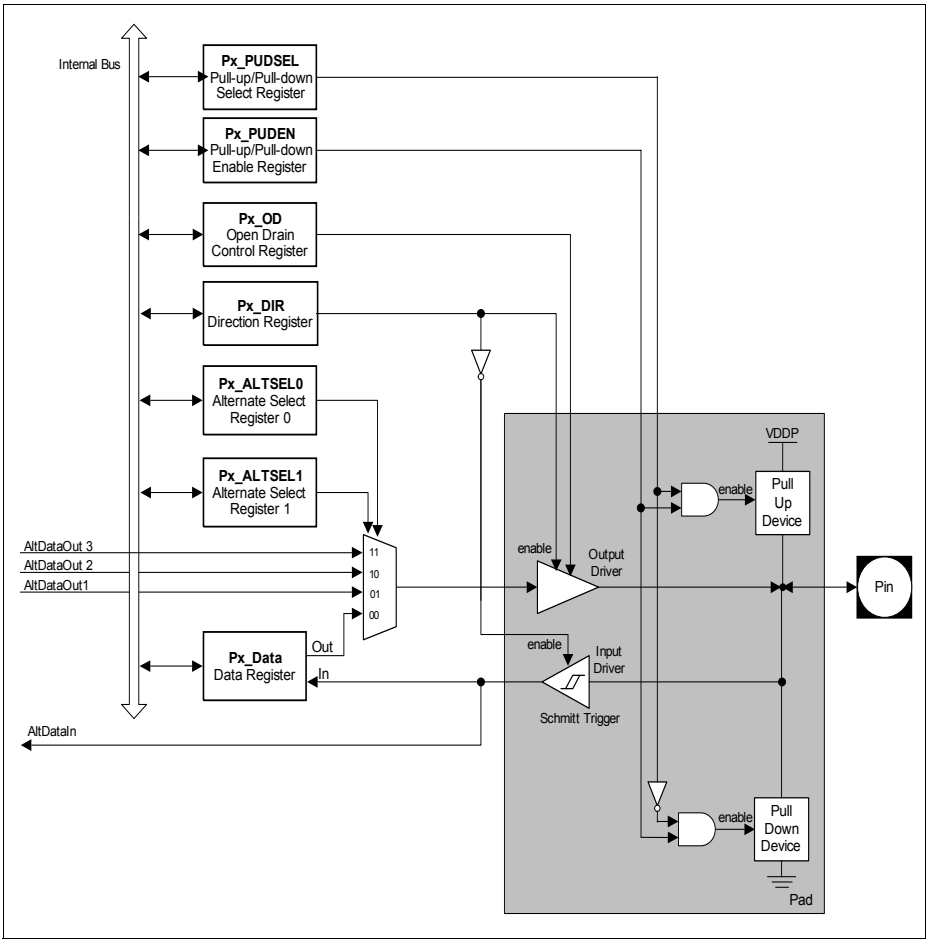



**Figure 18 General Structure of Bidirectional Port**

## 3.16 Timer 2

Timer 2 is a 16-bit general purpose timer (THL2) that has two modes of operation, a 16-bit auto-reload mode and a 16-bit one channel capture mode. If the prescalar is disabled, Timer 2 counts with an input clock of PCLK/12. Timer 2 continues counting as long as it is enabled.

**Table 29 Timer 2 Modes**

| Mode | Description |
|---|---|
| **Auto-reload** | **Up/Down Count Disabled**<br>• Count up only<br>• Start counting from 16-bit reload value, overflow at $FFFF_H$<br>• Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well<br>• Programmble reload value in register RC2<br>• Interrupt is generated with reload event |
| | **Up/Down Count Enabled**<br>• Count up or down, direction determined by level at input pin T2EX<br>• No interrupt is generated<br>• Count up<br>– Start counting from 16-bit reload value, overflow at $FFFF_H$<br>– Reload event triggered by overflow condition<br>– Programmble reload value in register RC2<br>• Count down<br>– Start counting from $FFFF_H$, underflow at value defined in register RC2<br>– Reload event triggered by underflow condition<br>– Reload value fixed at $FFFF_H$ |
| **Channel capture** | • Count up only<br>• Start counting from $0000_H$, overflow at $FFFF_H$<br>• Reload event triggered by overflow condition<br>• Reload value fixed at $0000_H$<br>• Capture event triggered by falling/rising edge at pin T2EX<br>• Captured timer value stored in register RC2<br>• Interrupt is generated with reload or capture event |

## 3.18 Analog-to-Digital Converter

The XC866 includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at Port 2.

**Features:**

- Successive approximation
- 8-bit or 10-bit resolution
  (TUE of ± 1 LSB and ± 2 LSB, respectively)
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access
  (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter
  (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

## 3.19 On-Chip Debug Support

The On-Chip Debug Support (OCDS) provides the basic functionality required for the software development and debugging of XC800-based systems.

The OCDS design is based on these principles:

- use the built-in debug functionality of the XC800 Core
- add a minimum of hardware overhead
- provide support for most of the operations by a Monitor Program
- use standard interfaces to communicate with the Host (a Debugger)

**Features:**

- Set breakpoints on instruction address and within a specified address range
- Set breakpoints on internal RAM address
- Support unlimited software breakpoints in Flash/RAM code region
- Process external breaks
- Step through the program code

The OCDS functional blocks are shown in **Figure 35**. The Monitor Mode Control (MMC) block at the center of OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals. After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work-data and Monitor-stack). The OCDS system is accessed through the JTAG[1)], which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated MBC pin is used for external configuration and debugging control.

*Note: All the debug functionality described here can normally be used only after XC866 has been started in OCDS mode.*

1) The pins of the JTAG port can be assigned to either Port 0 (primary) or Ports 1 and 2 (secondary). User must set the JTAG pins (TCK and TDI) as input during connection with the OCDS system.

**Table 38 Power Down Current (Operating Conditions apply; $V_{DDP}$ = 5V range )**

| Parameter | Symbol | Limit Values | | Unit | Test Condition Remarks |
|---|---|---|---|---|---|
| | | typ.[1] | max.[2] | | |
| **$V_{DDP}$ = 5V Range** | | | | | |
| Power-Down Mode[3] | $I_{PDP}$ | 1 | 10 | µA | $T_A$ = + 25 °C.[4] |
| | | - | 30 | µA | $T_A$ = + 85 °C, XC866-4FR, XC866-2FR [4][5] |
| | | - | 35 | µA | $T_A$ = + 85 °C, XC866-1FR, ROM device[4][5] |

1) The typical $I_{PDP}$ values are measured at $V_{DDP}$ = 5.0 V.

2) The maximum $I_{PDP}$ values are measured at $V_{DDP}$ = 5.5 V.

3) $I_{PDP}$ (power-down mode) has a maximum value of 200 µA at $T_A$ = + 125 °C.

4) $I_{PDP}$ (power-down mode) is measured with: $\overline{\text{RESET}}$ = $V_{DDP}$, $V_{AGND}$= $V_{SS}$, RXD/INT0 = $V_{DDP}$; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

5) Not subject to production test, verified by design/characterization.

**Table 39 Power Supply Current Parameters (Operating Conditions apply; $V_{DDP}$ = 3.3V range)**

| Parameter | Symbol | Limit Values | | Unit | Test Condition Remarks |
|---|---|---|---|---|---|
| | | typ.[1] | max.[2] | | |
| **$V_{DDP}$ = 3.3V Range** | | | | | |
| Active Mode | $I_{DDP}$ | 21.5 | 23.3 | mA | [3] |
| Idle Mode | $I_{DDP}$ | 16.4 | 18.9 | mA | XC866-4FR, XC866-2FR [4] |
| | | 11.2 | 13.5 | mA | XC866-1FR, ROM device [4] |
| Active Mode with slow-down enabled | $I_{DDP}$ | 6.8 | 8 | mA | XC866-4FR, XC866-2FR [5] |
| | | 5.4 | 7.3 | mA | XC866-1FR, ROM device [5] |
| Idle Mode with slow-down enabled | $I_{DDP}$ | 6.8 | 7.8 | mA | XC866-4FR, XC866-2FR [6] |
| | | 4.9 | 6.9 | mA | XC866-1FR, ROM device [6] |

1) The typical $I_{DDP}$ values are periodically measured at $T_A$ = + 25 °C and $V_{DDP}$ = 3.3 V.

2) The maximum $I_{DDP}$ values are measured under worst case conditions ($T_A$ = + 125 °C and $V_{DDP}$ = 3.6 V).

3) $I_{DDP}$ (active mode) is measured with: CPU clock and input clock to all peripherals running at 26.7 MHz(set by on-chip oscillator of 10 MHz and NDIV in PLL_CON to $0010_B$), $\overline{RESET}$ = $V_{DDP}$, no load on ports.

4) $I_{DDP}$ (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 26.7 MHz, $\overline{RESET}$ = $V_{DDP}$, no load on ports.

5) $I_{DDP}$ (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 833 KHz by setting CLKREL in CMCON to $0101_B$, $\overline{RESET}$ = $V_{DDP}$, no load on ports.

6) $I_{DDP}$ (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enable and running at 833 KHz by setting CLKREL in CMCON to $0101_B$,, $\overline{RESET}$ = $V_{DDP}$, no load on ports.

**Table 40 Power Down Current (Operating Conditions apply; $V_{DDP}$ = 3.3V range )**

| Parameter | Symbol | Limit Values | | Unit | Test Condition Remarks |
|---|---|---|---|---|---|
| | | typ.[1] | max.[2] | | |
| **$V_{DDP}$ = 3.3V Range** | | | | | |
| Power-Down Mode[3] | $I_{PDP}$ | 1 | 10 | µA | $T_A$ = + 25 °C.[4] |
| | | - | 30 | µA | $T_A$ = + 85 °C, XC866-4FR, XC866-2FR[4][5] |
| | | - | 35 | µA | $T_A$ = + 85 °C, XC866-1FR, ROM device[4][5] |

1) The typical $I_{PDP}$ values are measured at $V_{DDP}$ = 3.3 V.

2) The maximum $I_{PDP}$ values are measured at $V_{DDP}$ = 3.6 V.

3) $I_{PDP}$ (power-down mode) has a maximum value of 200 µA at $T_A$ = + 125 °C.

4) $I_{PDP}$ (power-down mode) is measured with: $\overline{\text{RESET}}$ = $V_{DDP}$, $V_{AGND}$= $V_{SS}$, RXD/INT0= $V_{DDP}$; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

5) Not subject to production test, verified by design/characterization.

### 4.3.3 Power-on Reset and PLL Timing

**Table 42 Power-On Reset and PLL Timing (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Pad operating voltage | $V_{PAD}$ CC | 2.3 | – | – | V | |
| On-Chip Oscillator start-up time | $t_{OSCST}$ CC | – | – | 500 | ns | |
| Flash initialization time | $t_{FINIT}$ CC | – | 160 | – | µs | |
| $\overline{RESET}$ hold time[1] | $t_{RST}$ SR | – | 500 | – | µs | $V_{DDP}$ rise time (10% – 90%) ≤ 500µs |
| PLL lock-in in time | $t_{LOCK}$ CC | – | – | 200 | µs | |
| PLL accumulated jitter | $D_P$ | – | – | 0.7 | ns | 2) |

1) $\overline{RESET}$ signal has to be active (low) until $V_{DDC}$ has reached 90% of its maximum value (typ. 2.5V).

2) PLL lock at 80 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 40 and P = 1.

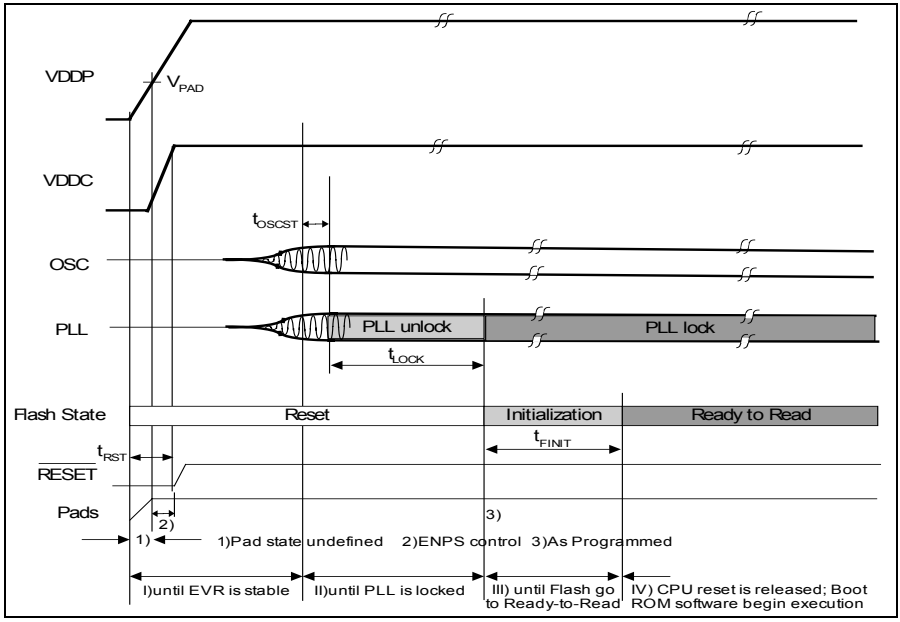
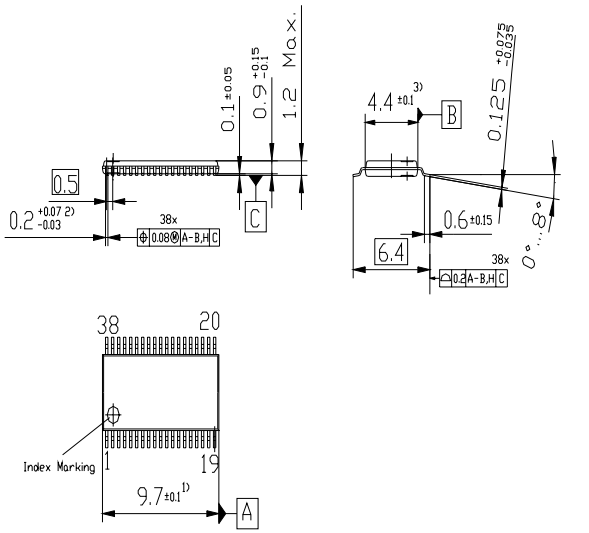



**Figure 42 Power-on Reset Timing**

## 5.2 Package Outline




1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.15 MAX. PER SIDE

2) DOES NOT INCLUDE DAMBAR PROTRUSION OF 0.08 MAX. PER SIDE

3) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.25 MAX. PER SIDE

**Figure 46 PG-TSSOP-38-4 Package Outline**